DATA HANDBOOK

Liquid Crystal Displays and Driver ICs for LCD

BOOK LCD01 1991

Philips Components

PHILIPS

LIQUID CRYSTAL DISPLAYS

CONTENTS

page

PREFACE

This data handbook incorporates information about LCD cells, LCD modules and driver ICs for LCD.

LCD cells are versatile displays with a large number of superior features. These include low power consumption, high legibility (even in bright sunlight), thin outline and flexibility in pattern design, making them very suitable for customization.

Modules are the incorporation of LCD cells and IC drivers into one unit. The thin outline of the cells enable the module to remain compact and easy to mount in a variety of applications. We offer both Full dot graphic and character display modules in twisted nematic (TN, character) and supertwisted nematic (STN, full dot graphic) liquid crystal technologies (see the chapter 'User Guide').

With the advent of STN technology, the application areas of LCDs have expanded enormously. STN creates the possibility of high information density displays with far better viewing angles and contrast than those possible in TN technology (see the section 'Derived technologies' of the chapter 'User Guide').

Driver ICs for LCD can be both dedicated or non-dedicated microcontrollers or microprocessors. Full data for the dedicated devices is contained in this handbook. For data on the non-dedicated devices please refer to the IC data handbook series.

As LCD's can be custom designed the handbook contains a 'Custom Design Guide'.

For more information about the principles of LCD refer to the chapter 'User Guide'. Standard cell data is contained in the chapter 'LCD data' and module data is contained in the chapter 'LCD Module Data'. Data for the dedicated driver ICs is contained in the chapter 'Driver ICs for LCD'.

Type number survey

Liquid Crystal Displays — Type number survey

Type number survey - LCD cells

BASIC TYPE NUMBER	DESCRIPTION*	DRIVE**	DIMENSIONS (mm) EXCLUDING PINS		PAGE
			WIDTH	HEIGHT	
LHA142	1-character	DD	50.8	80.0	80
LTA141	5 x 7 dot matrix	DD	50.8	80.0	86
LTA331	16-character, 1-line	1:16	69.0	23.0	89
LTA332	16-character, 2-line	1:16	69.0	24.7	94
LTA341	20-character, 2-line	1:16	93.6	34.6	99
LTA342	24-character, 2-line	1:16	93.6	34.6	104
LTA343	40-character, 2-line	1:16	160.0	27.4	109
LTD101	3 1/2-digit	DD	50.8	22.9	114
LTD132	3 1/2-digit	1:2	46.8	54.8	117
LTD133	3 1/2-digit clock LCD	1:2	38.6	20.8	121
LTD201	4-digit	DD	23.9	14.0	124
LTD202	2-digit	DD	27.9	30.4	126
LTD203	4-digit	DD	38.0	20.3	129
LTD211	8-digit	1:2	38.0	20.3	132
LTD221	3 1/2-digit	DD	50.8	30.4	135
LTD222	3 1/2-digit multimeter	DD	50.7	30.4	138
LTD224	3 1/2-digit multimeter	DD	50.8	30.4	141
LTD225	3 1/2-digit multimeter	DD	50.8	30.4	144
LTD226	4-digit	DD	50.8	30.4	147
LTD227	4 1/2-digit multimeter	DD	50.8	30.4	150
LTD228	5-digit	DD	50.8	30.4	153
LTD229	6-digit	DD	69.8	30.4	156
LTD231	3 1/2-digit multimeter	1:3	50.8	30.4	159
LTD232	4 1/2-digit multimeter	1:3	50.8	30.4	162
LTD233	16-digit	1:2	69.8	20.3	165
LTD234	16-digit	1:4	69.8	20.3	169
LTD235	4-digit	1:3	50.8	30.4	173
LTD241	3 1/2-digit multimeter	DD	69.8	38.0	177
LTD242	4-digit	DD	69.8	38.0	180
LTD261	1-digit	DD	76.2	101.6	183
LTD262	8-digit	DD	93.8	30.8	186
LTD263	6-digit	DD	93.8	30.8	190
LTD264	5-digit	DD	114.0	26.0	193
LTD321	bargraph	DD	69.8	30.4	197
LTD351	bargraph	1:2	26.0	114.0	200

* For more detailed visual description refer to optical selection guide.

** DD = direct drive

Liquid Crystal Displays — Type number survey

Type number survey - LCD modules

BASIC TYPE NUMBER	DESCRIPTION*	DRIVE	PAGE
LTM233	16-digit, 1-line, segment display module	1:2	204
LTN111	5 x 7 dot, 16-character, 1-line, dot matrix module	1:16	209
LTN211	5 x 7 dot, 16-character, 2-line dot matrix module	1:16	219
LTN221	5 x 7 dot, 20-character, 2-line dot matrix module	1:16	229
LTN222	5 x 7 dot, 24-character, 2-line dot matrix module	1:16	239
LTN243	5 x 7 dot, 40-character, 2-line dot matrix module	1:16	249

* For more detailed visual description refer to optical selection guide

Type number survey-EL-backlights

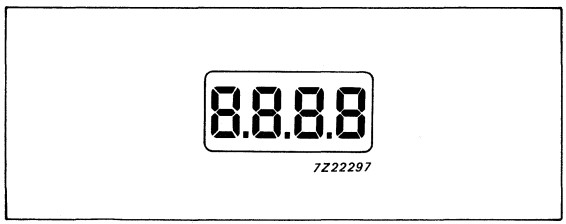
TYPE NUMBER	DESCRIPTION	PAGE
LXL111	to be used with LTN111 module, emitted colour is green	260
LXL211	to be used with LTN211 module, emitted colour is green	262
LXL221	to be used with LTN221 and LTN222 modules, emitted colour is green	264
LXL242	to be used with LTN243 module, emitted colour is green	266

Optical selection guide

Liquid Crystal Displays

Optical selection guide

LTD201



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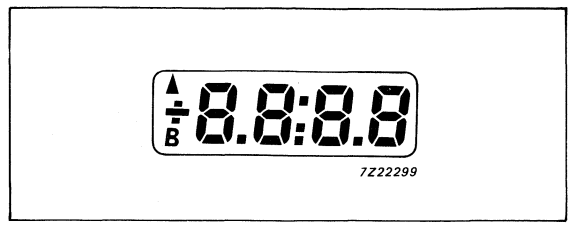

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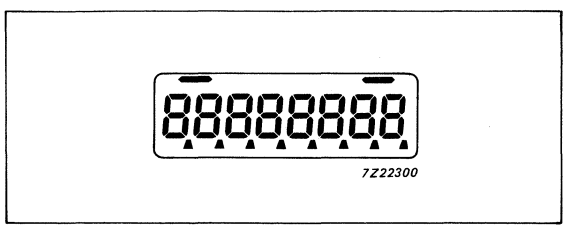

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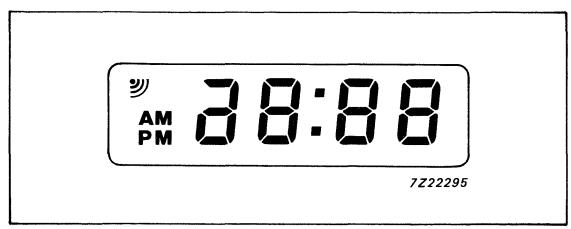

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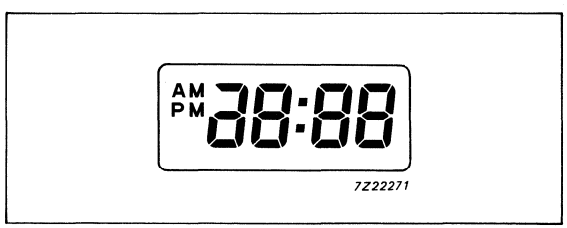

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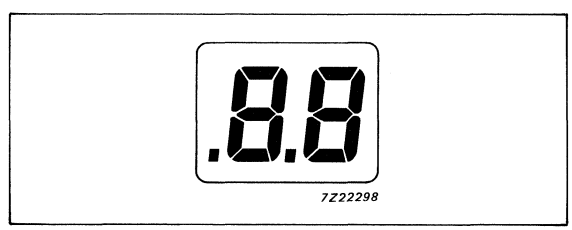

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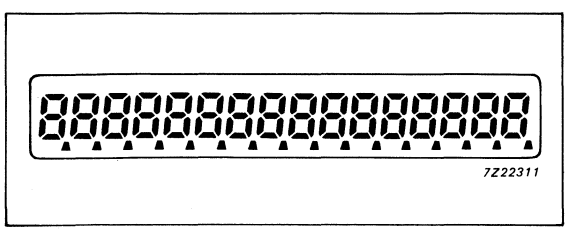

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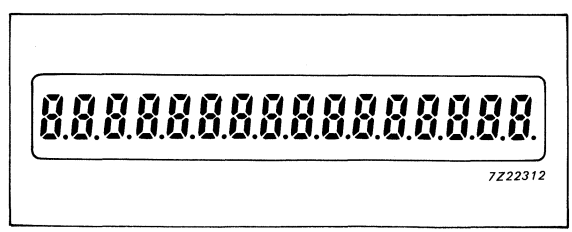

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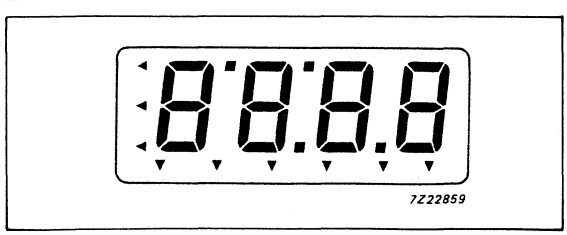
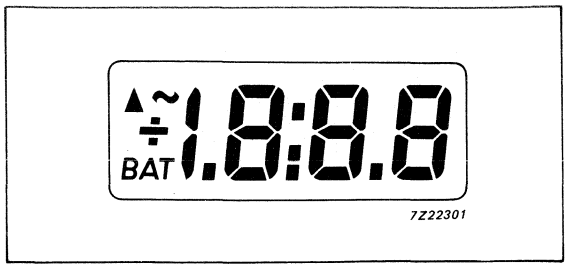


Liquid Crystal Displays

Optical selection guide

LTD221



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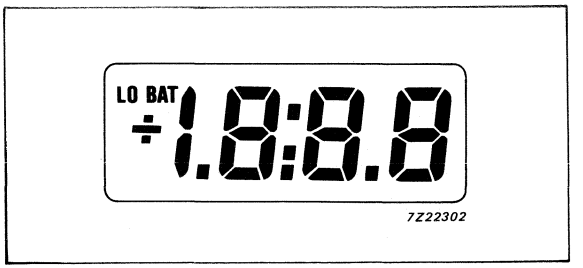

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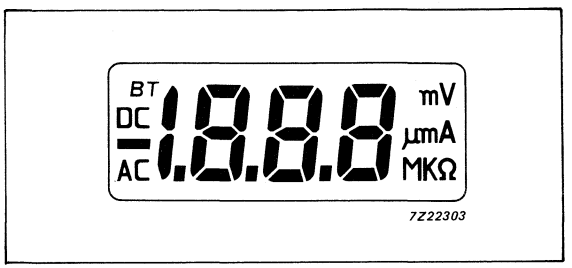

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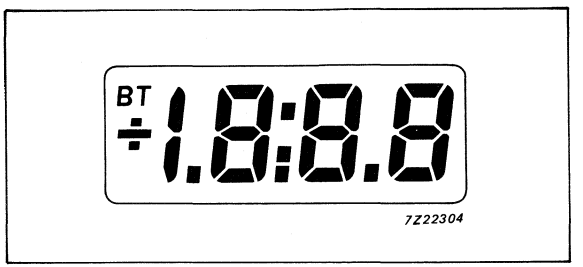

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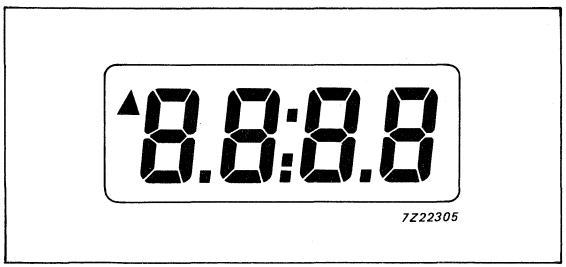

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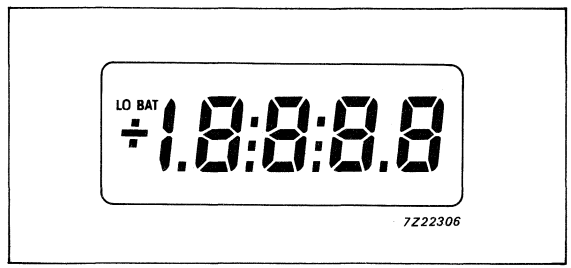

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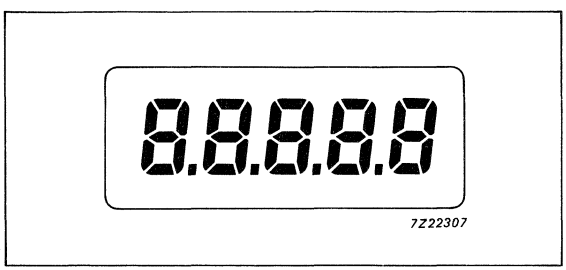

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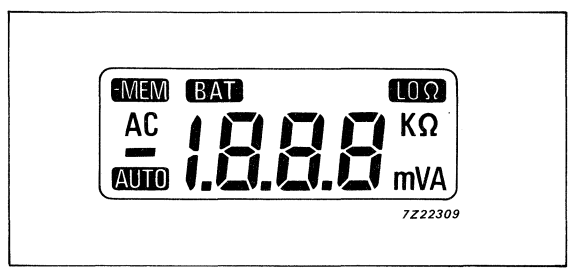

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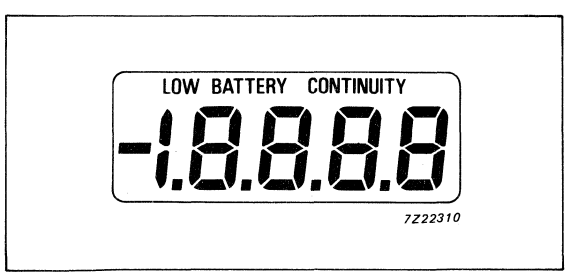

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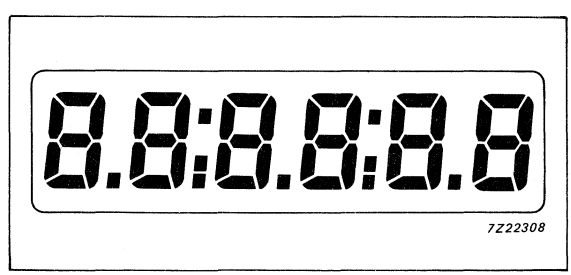

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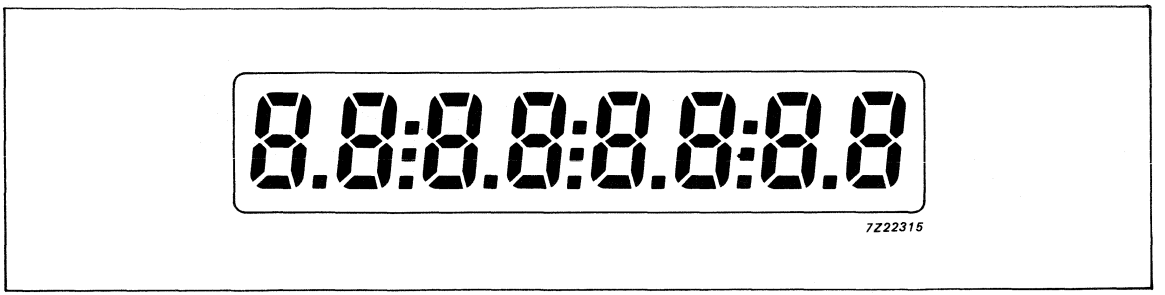

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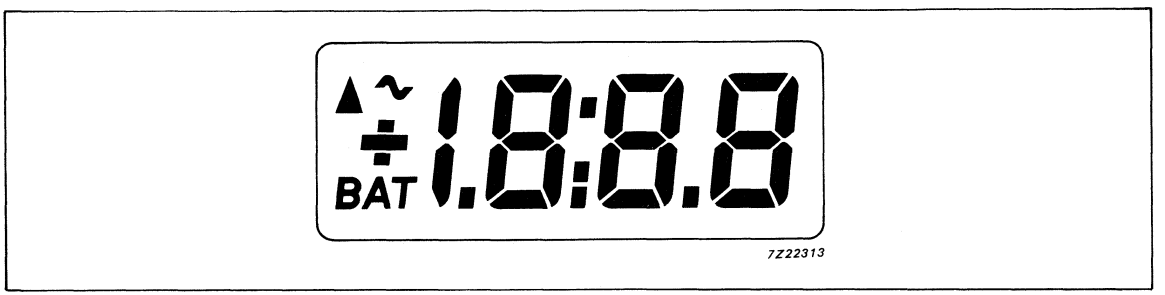

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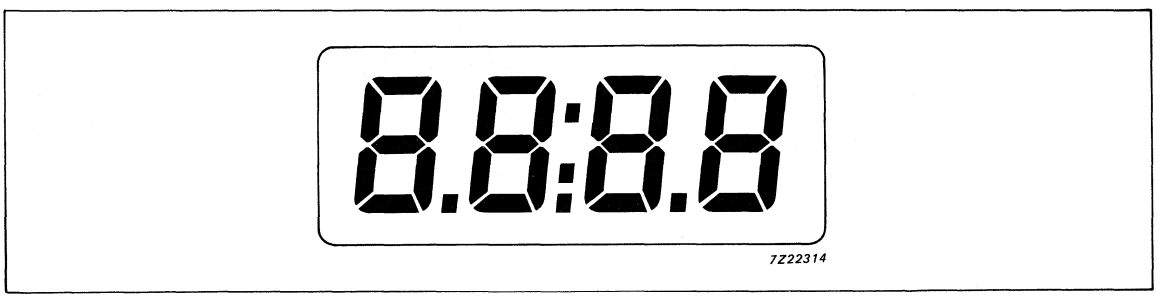

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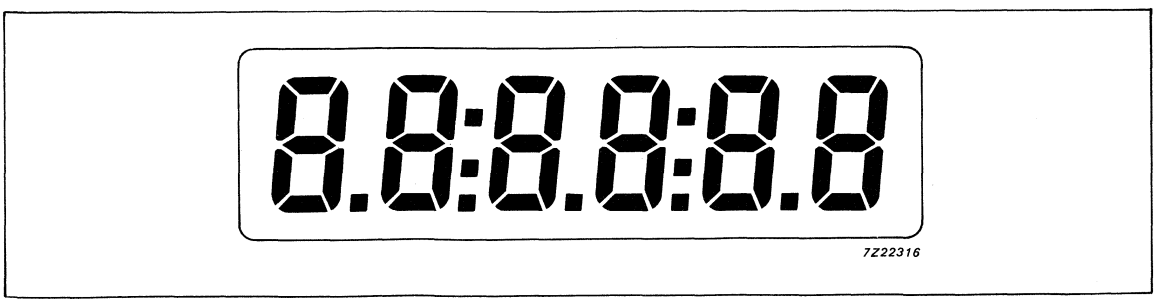

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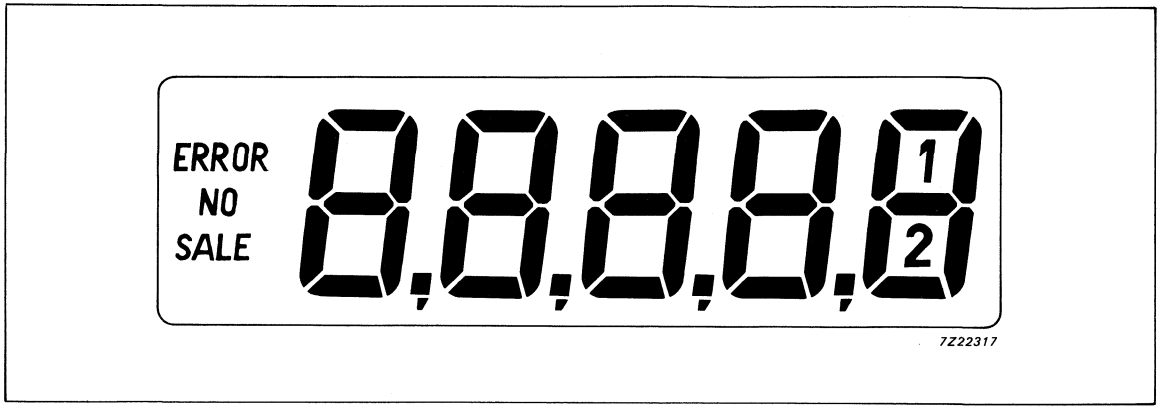

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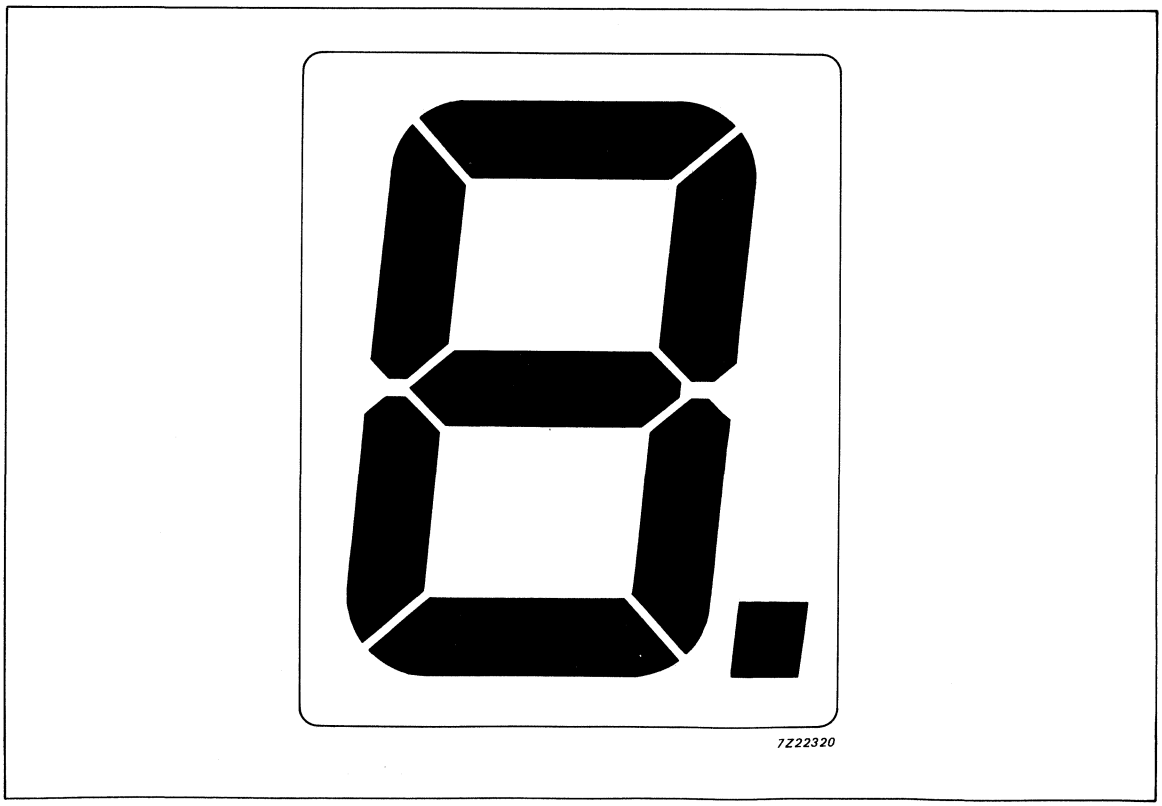

Liquid Crystal Displays — Optical selection guide

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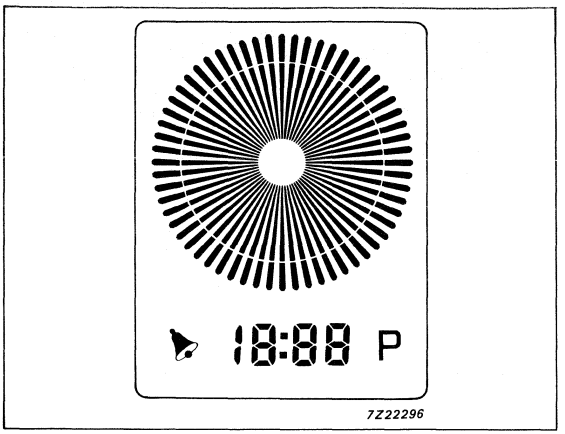

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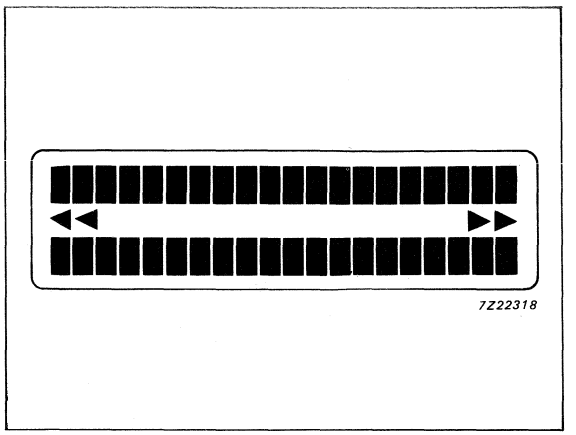

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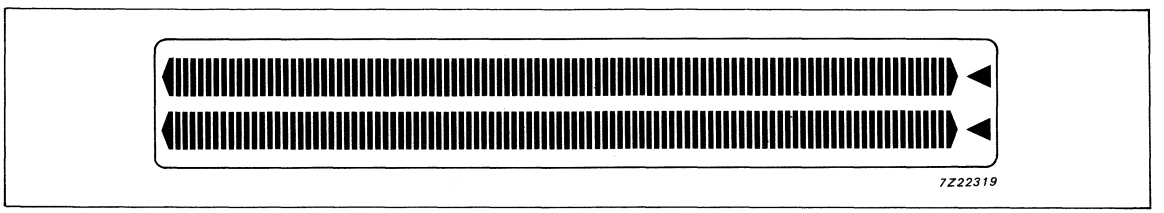

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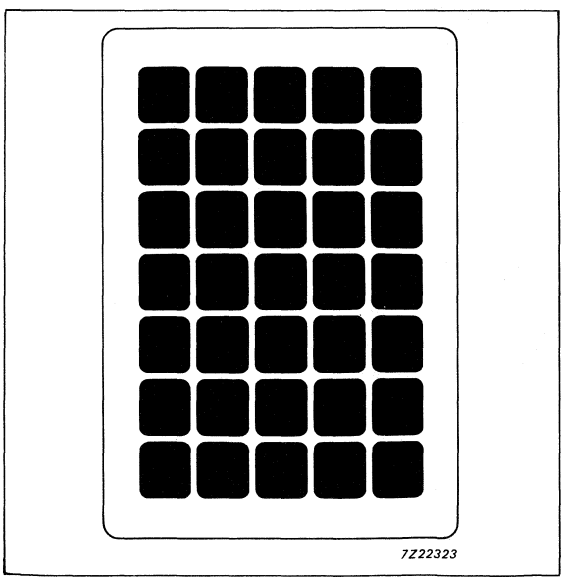

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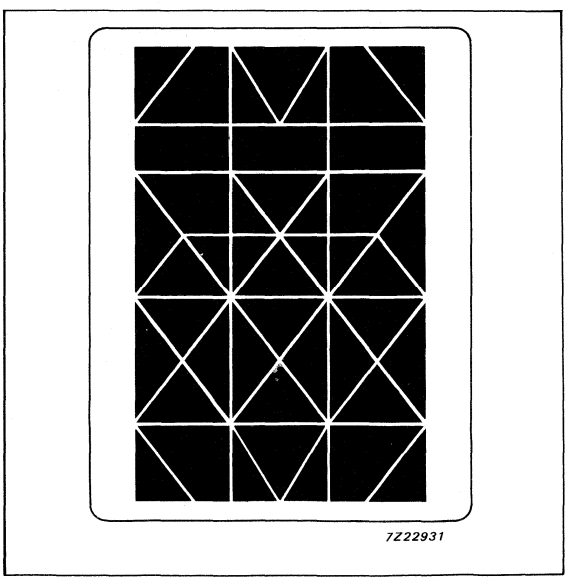

Liquid Crystal Displays — Optical selection guide

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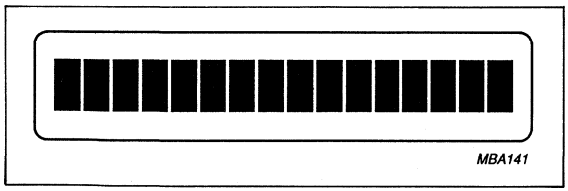

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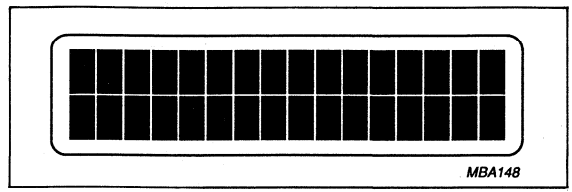

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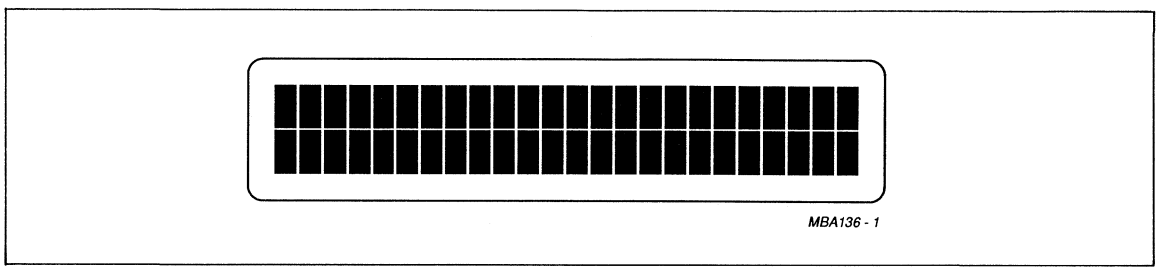

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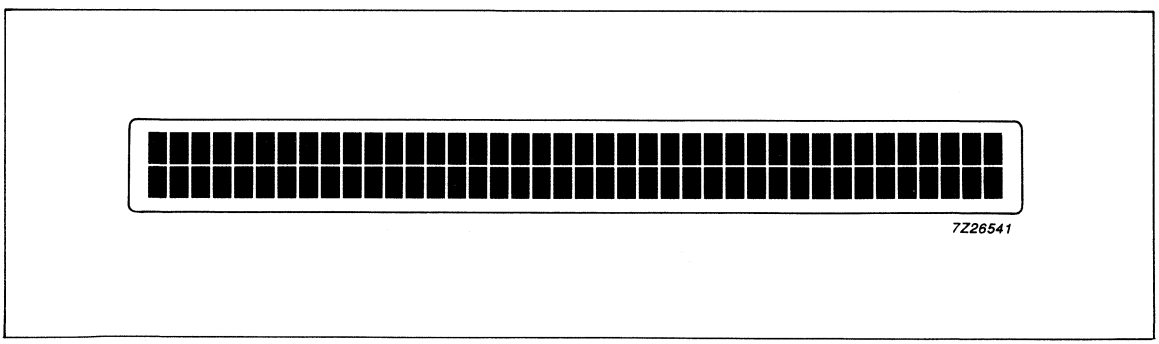

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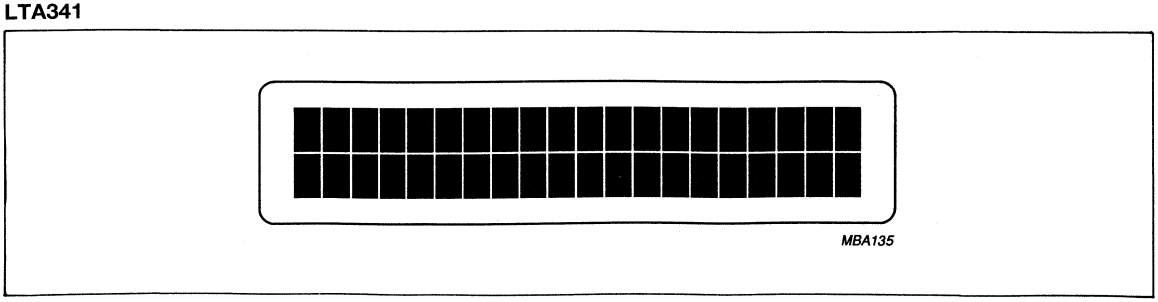

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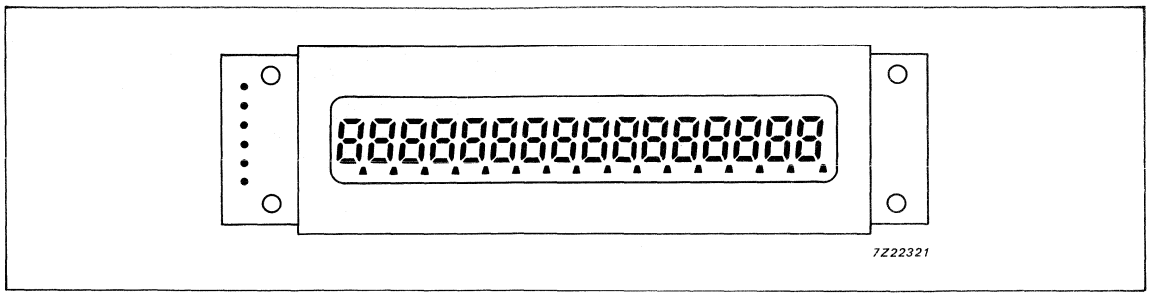

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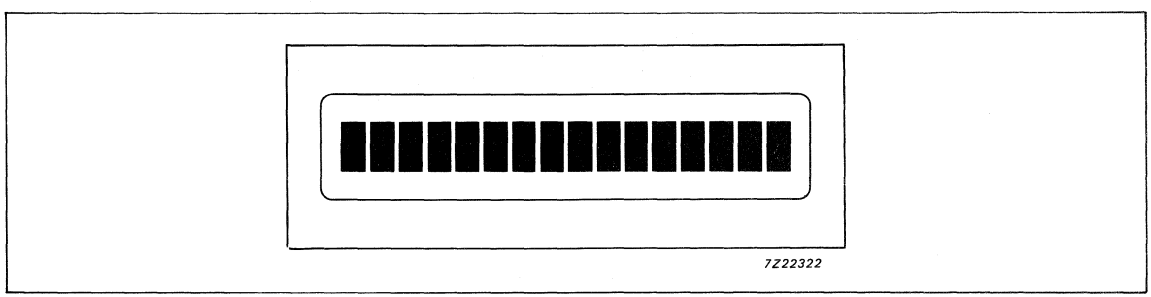

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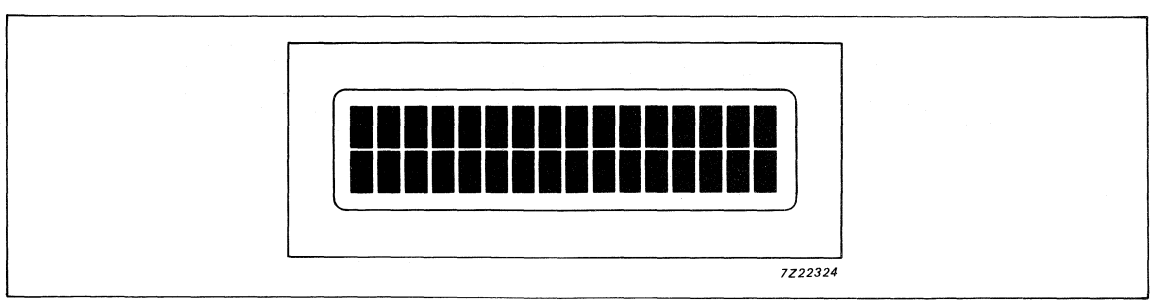

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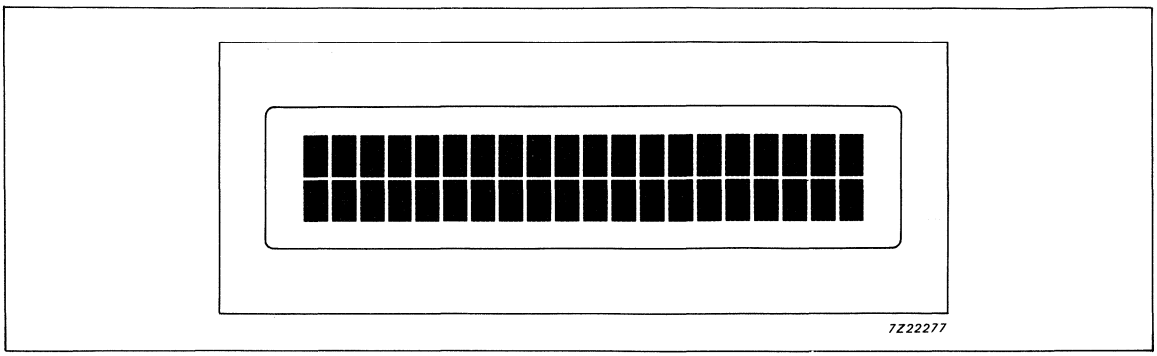

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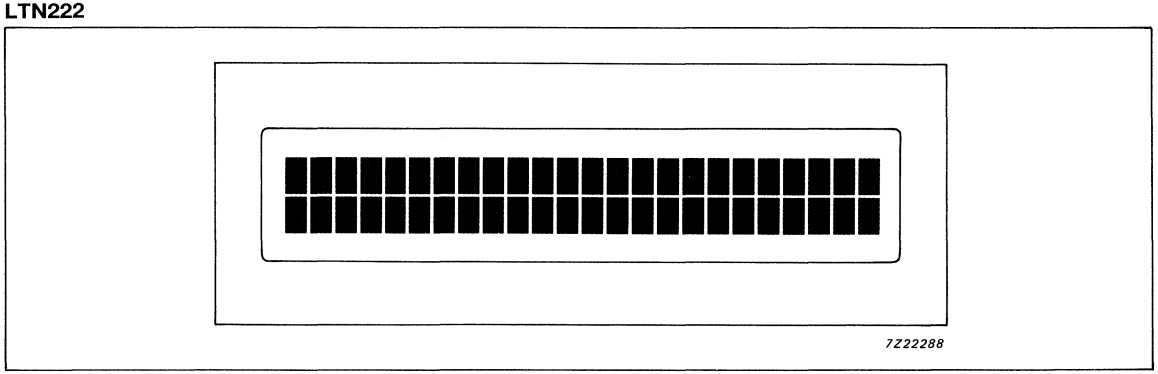
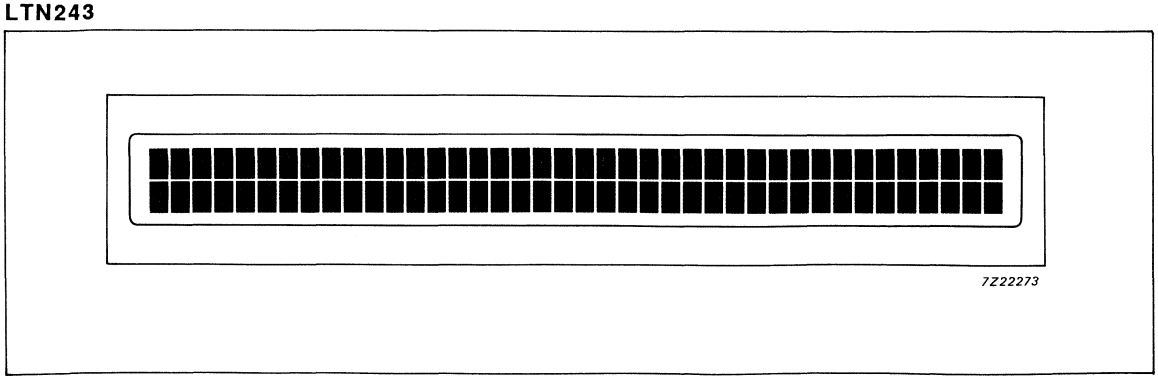


LTN243



User guide

Liquid crystal displays — User guide

Liquid crystal display — User guide

INTRODUCTION

Liquid crystals are materials which combine the properties of both liquids and crystals. Rather than a melting point they have a temperature range, known as a mesophase, within which the molecules are almost as mobile as they would be in a liquid, but are grouped together in an ordered form, similar to that of a solid crystal.

Around 1970 it was found that thin layers of a certain type of liquid crystal can be switched from transparent to opaque, or vice-versa, by the application of a voltage. This property is the fundamental operating principle of liquid crystal displays (LCDs).

The main features of LCDs are:

- **flat and compact size;** LCDs are lightweight and very thin; the thickness of the display is only a few millimeters
- **low power consumption;** low power and supply requirements mean that LCDs can easily be powered over long periods, by batteries, whilst at the same time be compatible with modern electronic circuits, for example CMOS
- **passive display;** LCDs do not generate light, and as such are comparable to printed matter; light is necessary in order to read the display and it will not fade as the ambient light increases, however, reading in dark conditions is possible with the use of back-lighting
- **reliable;** LCDs have a wide operating temperature range and a long life
- **flexible design;** a change in display size or layout is relatively simple, making LCDs ideal for customization
- **low cost;** LCDs are the most economically produced flat display system, including drive and supply aspects

Initially LCDs were used almost exclusively in watches, calculators, and measuring instruments. These were simple, usually seven segment displays, with a limited amount of numeric data. More recently, advances in technology have improved legibility, information content and the temperature range, which has led to applications in telecommunications, cars, entertainment electronics and computers.

LCDs are now the fastest growing display technology. They are currently replacing the CRT for the display of text and graphics and may eventually replace the CRT in TV applications.

STRUCTURE OF AN LCD

An LCD consists of two glass planes which are sealed together with a gap between them of about six to ten μm (Fig 1.). The inner surfaces of the glass plates are coated with transparent electrodes which define the characters, symbols, or other patterns to be displayed. The electrode material is usually indium tin oxide (ITO).

Between the electrodes and the liquid crystal there are polymeric layers which are treated in a way that induces the adjacent liquid crystal molecules to maintain a defined orientation angle. For this reason, the polymeric layers are also known as orientation, or alignment layers.

The distance between the two plates is set within narrow limits by means of glass fibre spacers or minute plastic balls.

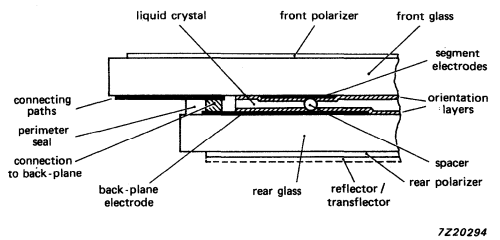


Fig.1 Construction of an LCD.

Liquid crystal

The most common type of liquid crystal used in display technology is nematic (fig. 2(a)). In nematic liquid crystal the long rod- like molecules align themselves spontaneously parallel, which gives the material anisotropic optical and electrical properties, that is, it has different properties in different directions. Other classes of liquid which have increasing significance in display technology are cholesteric (Fig. 2(b)) and smectic (Fig. 2(c)).

Liquid crystal display

User guide

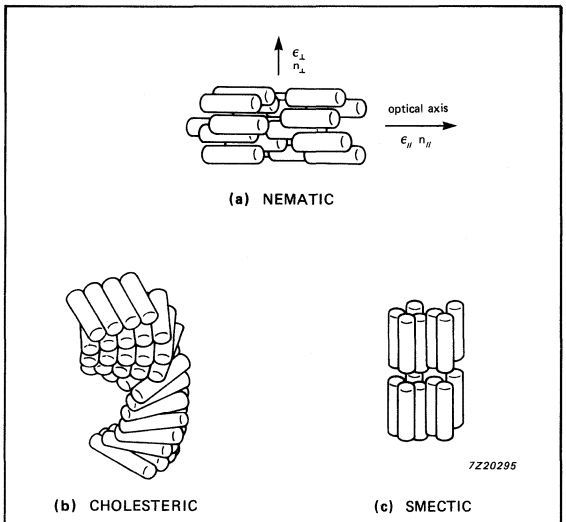


Fig.2 Molecular structure of liquid crystals (a) nematic (b) cholesteric (c) smectic.

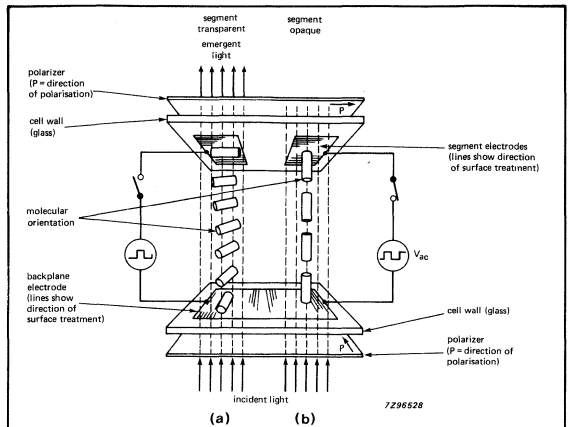


Fig.3 Principle of operation of a Twisted Nematic (TN) display (a) OFF state (b) On state.

If one polarizer is rotated through 90° the effect will be reversed and the display will appear black under no voltage field conditions and bright when a voltage is applied. This is known as a negative image display.

THE TN LCD IN OPERATION

The operating principle of Twisted Nematic (TN) LCDs is illustrated in Fig. 3. The nematic liquid crystal molecules are anchored in a fixed direction at the top and bottom plates by the orientation layer. As the orientation directions of the top and bottom polarizers differ by an angle of 90° the crystal molecules are twisted through a 90° helix. Polarizing filters are aligned with the orientation directions at the respective plates. Polarized light from the bottom polarizer is then guided by the crystal molecules through the helix to the top plate with its polarization direction rotated 90°. This property is caused by the optical anisotropy of the molecules. As such the polarization direction is aligned with the top polarizer and light passes through it to give the display a bright appearance (Fig. 3(a)). If sufficient voltage is applied across the electrodes the electrical anisotropy of the molecules will cause them to align with the electric field and the 90° twist in the optic axis will be distorted. The light will then pass through the liquid crystal, but will maintain its polarization direction and be absorbed by the top polarizer (Fig. 3(b)). On switching off the initial state is restored and the cell will again appear transparent. Under these conditions the display will appear black when ON and bright when OFF. This is known as a positive image display.

If the electrodes were to cover the top and bottom plates the LCD would act as a light shutter. A more usual arrangement is for the electrodes to be patterned in such a way that specific segments can be switched to form characters, graphics or symbols. An example of this is the basic seven segment digit shown in Fig. 4. Any number can be displayed by switching on the appropriate electrodes, that form the various segments. It should be noted that segments are only formed where the segment electrodes and the common (backplane) electrode overlap; the remaining parts of the electrodes are required for connections to the outside.

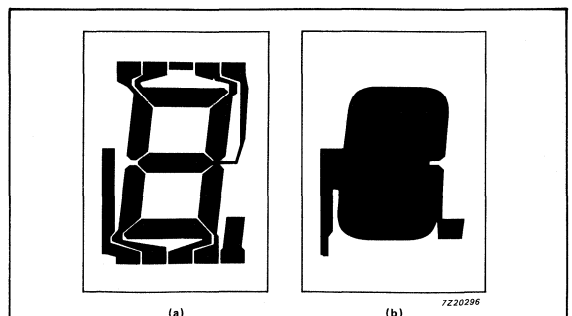


Fig.4 A seven segment plus decimal point display (a) segment electrodes (b) common electrode.

ILLUMINATION MODES

LCDs can be operated in one of three modes, depending upon the ambient light conditions:

- **reflective mode**; the LCD is covered by a diffuse metallic reflector, such as brushed aluminium foil, that reflects ambient light back through the display; this mode is best suited for positive image displays and applications with sufficient ambient light; reflective mode is especially suited to battery operated displays as no lighting power is required (Fig. 5(b))
- **transmissive mode**; the display is lit from behind; negative image displays are best suited to this mode; their appearance is similar to active displays such as Light Emitting Diodes (LEDs), Vacuum Fluorescent Displays (VFDs) etc; this type of display can be projected like a slide (Fig. 5(a))
- **transflective mode**; a combination of transmissive and reflective modes; the display is backed by a partly transmissive reflector (transflector) which reflects ambient light as well as transmitting diffused back-lighting for night use (Fig. 5(c))

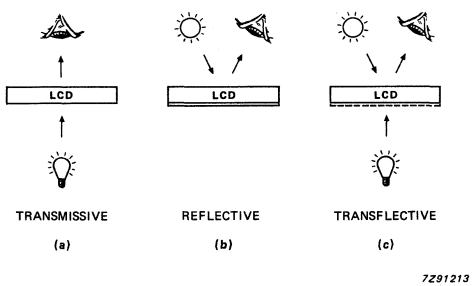


Fig.5 The three illumination modes (a) transmissive (b) reflective (c) transflective

COLOUR IN TN LCDs

Colour can be introduced into a TN display in one of three ways: colour selective polarizers, coloured filters or coloured back-lighting.
Colour selective polarizers produce coloured segments on a bright background or bright segments on a dark background. A two colour combination can be produced by using two different colour selective polarizers, for example red and green polarizers will give red segments on a green background or vice-versa.

Coloured filters may be either foil behind the display or translucent colours printed onto the display itself. They are best suited to transmissive mode LCDs with a negative image, that is coloured segments on a dark background. Coloured back-lighting produces black segments on a dark background. It is possible to change the colour of the display by using two different backlights, for example between red and green, and by using both lights, white. It should be noted that the colour effect in a transflective display will be greatly reduced under high ambient light conditions.

OPTICAL PROPERTIES

Contrast and brightness

The legibility of an LCD depends upon a variety of factors such as pattern layout, technology, driving and illumination conditions, viewing direction, viewing angle, viewing distance and operating voltage. The most important optical characteristics when defining legibility are brightness and contrast ratio.
The brightness of an LCD is expressed as the luminance of the reflected or transmitted light compared to the luminance of the incident light. For a reflective LCD an MgO surface is used as a reference for testing luminance. The brightness of a TN LCD cannot be higher than 50%, since an ideal polarizer only transmits half the incident light. A reflective display will, therefore, tend to appear rather grey. A brighter display can be obtained using back-lighting.
The contrast ratio (C_R) of an LCD is the ratio between the brightness of the light areas (B_l) and the brightness of the dark areas (B_d) of the display.

i.e., $C_R = B_l/B_d$

For a TN display the typical maximum contrast ratio can range between 5 and 50.
In a reflective display, the maximum contrast ratio that can be detected by the human eye is normally about 10 and the lower limit of good legibility about 2. For comparison the contrast ratio of this page is about 7.
A higher contrast is necessary for back illuminated displays. This is especially true of negative image displays, as the human eye can easily detect light leaking through the dark background of the display. The leakage can be reduced by matching the spectral transmission of the background and the spectral emission of the back-lighting system correctly (especially if a coloured filter is used).

Both brightness and contrast depend on the type of polarizers used. For reflective displays with a positive image, low efficiency polarizers produce brighter displays with a low contrast. High efficiency polarizers produce a high contrast but will reduce brightness considerably.

Viewing angle

A twisted nematic LCD has a preferred viewing direction (ϕ_{pref} measured in the plane of the LCD), which is built-in during the manufacturing process by treatment of the orientation layers. For most standard applications this direction is from below (6 o'clock) although other directions can be manufactured.

Fig. 6 shows a contrast versus voltage curve from three different angles α, which are referenced perpendicularly to the display. At a very low voltage the display is not visible; as the voltage is increased the pattern first appears at low elevation angles (high values of α) in the preferred viewing direction (curve 2). By further increasing the voltage the pattern becomes more visible at higher elevation angles. If the contrast is observed at a fixed drive voltage within the plane ϕ_{pref} and perpendicularly to the display the viewing angle is α_{opt} and maximum contrast occurs. At higher voltages the value of α_{opt} becomes rather small. However, $\alpha_{opt} = 0$ can never be reached and a basic asymmetry will always remain.
The voltage at which a display becomes visible (10% of maximum contrast) at a specific viewing direction and viewing angle, is known as the threshold voltage (V_{th}). The voltage at which contrast reaches 90% of its maximum value is known as the saturation voltage (V_{sat}).
Voltage and contrast characteristics will vary for different liquid crystal mixtures. Most mixtures will also have a negative temperature coefficient, that is V_{th} decreases as the temperature increases.

In a plane perpendicular to ϕ_{pref}, TN LCDs have an almost symmetrical contrast. This is shown by an isocontrast diagram, the method of illustrating the viewing cone of a display. An isocontrast diagram shows the contrast in the azimuth (ϕ) and elevation (α) viewing angles. Fig. 7 is a typical isocontrast for a TN display which has a preferred viewing direction from below (6 o'clock).

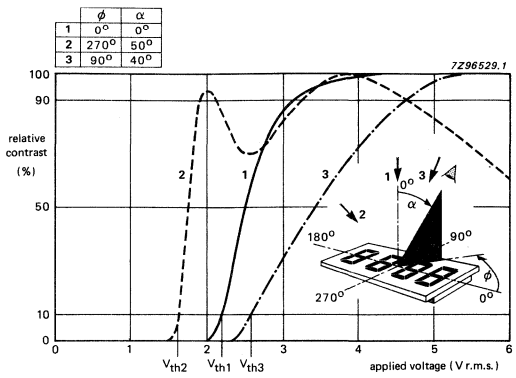


Fig.6 Relative contrast as a function of applied voltage.

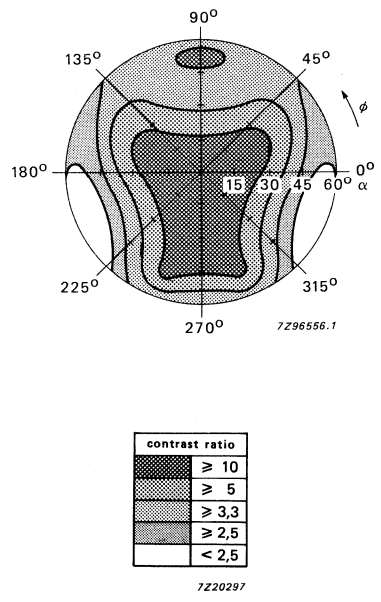


Fig.7 Typical isocontrast diagram for a direct drive, reflective, TN display, showing the variation of contrast as a function of the two components α and ϕ of the viewing angle.

Response times

Typical turn-on and turn-off times for LCDs range between 50 and 100 ms at room temperature. One of the main influences upon response times is the liquid crystal viscosity. As the viscosity increases with a decreasing temperature, the molecules become less free to move resulting in longer response times.
Response times are also affected by applied voltage, drive method and liquid crystal layer thickness.

DRIVING LCDs

Each segment of an LCD can be considered as the equivalent of an electrical capacitance with a very high parallel and low series resistance (Fig. 8). The capacitance is voltage dependent as the liquid crystal molecules have anisotropic dielectric properties. Applying a DC voltage will cause electro-chemical reactions which shorten the life of the LCD. For this reason, the drive voltage must be alternating with a maximum permissible DC component of 100 mV. The optical effect then produced in a display depends, approximately on the RMS value of the drive voltage.

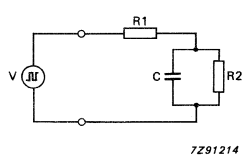


Fig.8 Simplified equivalent circuit of an LCD. R_1 is the series resistance of the electrodes. R_2 the series resistance of the liquid crystal and C the interelectrode capacitance. Typical values are R_1 = 10 kOhms, R_2 = 1 Mohm/cm^2, C = 1.5 nF/cm^2.

The frequency of the drive voltage must be at least 30 Hz to prevent display flicker. At this frequency and a drive voltage just above saturation voltage, typical current consumption is approximately 1.5 μA per square centimeter of the activated display area.The current consumption increases in direct proportion to the drive frequency. An upper frequency limit is set by coupling and relaxation effects which cause ghosting and irregular contrast in the display. These effects must be considered, especially in the layout of large and complex displays. The upper frequency limit is approximately 200 Hz.

Possible interference effects with lighting systems should also be considered when deciding on the drive frequency to be used.

Direct drive

A direct (or static) drive LCD has a separate connection and driver for each segment and one for the common back-plane.
The back-plane of a direct drive display is usually driven by a square wave having a peak-to-peak value (V_{op}) that is above the saturation voltage (V_{sat}).
To select a segment the inverse of the back-plane waveform is applied to the appropriate electrode. This produces an RMS voltage value between the back-plane and segment electrodes which is equal to V_{op}. The back-plane voltage waveform is also applied to all non-selected segments which results in a net zero voltage across them. A symmetrical square wave voltage difference results, if this was not the case undesirable DC components would be applied to the liquid crystal.
Fig. 9 illustrates a typical direct drive circuit with exclusive-OR gates controlling the voltage to the different segments. Individual segments are selected by switching the appropriate segment control line HIGH, which will invert the back-plane voltage applied to the segment. The control lines of non-selected segments are LOW and no inversion takes place.

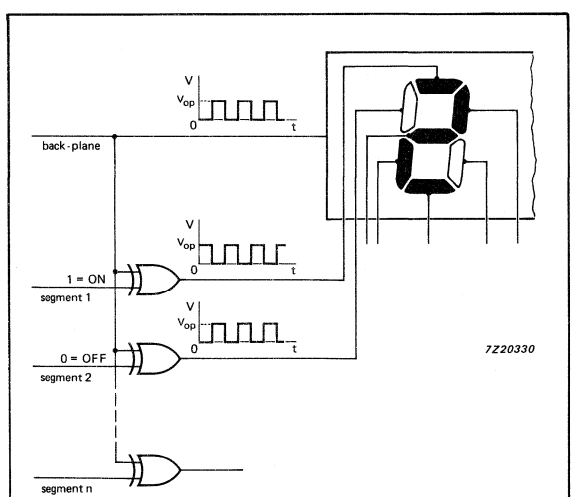


Fig.9 Phase-switching circuit for direct drive.

The advantages of direct drive are broad temperature ranges, wide viewing angles, fast response times and insensitivity to driving voltage tolerance. However, the number of connections and driving circuits needed can become very large for complex displays.

Multiplex drive

In high information density displays, such as a dot matrix, it is difficult or impossible to connect each dot or segment individually to an edge contact. The large number of contacts and drivers required could lead to low reliability and high cost. Therefore, it is necessary to use multiplex drive.

Multiplex drive electrodes are arranged in the form of a matrix. Segments are connected in groups and the back-plane is split into several commons so that every segment in a group has a different back-plane. A segment is then no longer identified by an individual external contact but by a group contact and a specific back-plane. The multiplex ratio is defined as 1:N, where N is the number of back-planes, or segments, per group.

Fig. 10 illustrates the segment to back-plane assignment for a seven segment digit, using a 1:3 multiplex drive. The number of contacts has been reduced from the nine necessary in direct drive, to six. Fig. 10(c) shows the equivalent circuit with each segment being represented by a capacitor.

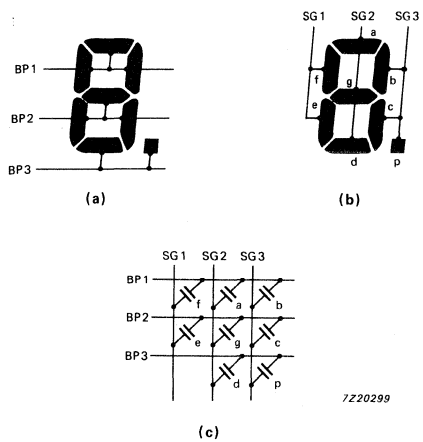


Fig.10 A single digit plus point, eight segment LCD with a 1:3 multiplex drive (a) back-plane electrodes (b) segment grouping (c) equivalent circuit.

The reduction in the number of contacts required by using multiplex drive can be dramatic. A segment display having a multiplex ratio of 1:N and a total of M segments can be addressed using as few as M/N + N connections.

For example:

- a 40-segment display requires 41 connections in direct drive but, by using a 1:4 multiplex drive the number of connections is reduced to

$40/4 + 4 = 14$

- a dot matrix display with 20 000 elements (pixels), that is 100 rows and 200 columns can be controlled with only 300 connections (number of rows + number of columns) rather than the 20 001 connections which would be necessary for direct drive.

An individual segment is selected by a combination of the back-plane and segment group signals. Fig. 11 shows a simple example of matrix waveforms. Each back-plane is selected in sequence; whether or not a segment is selected is determined by the level of the segment group voltage when the corresponding back-plane is addressed. The waveforms illustrated have net DC components which could cause electro-mechanical degradation of the liquid crystal. In practical addressing schemes, the net DC component is eliminated by alternately inverting both the back-plane and the segment group waveforms.

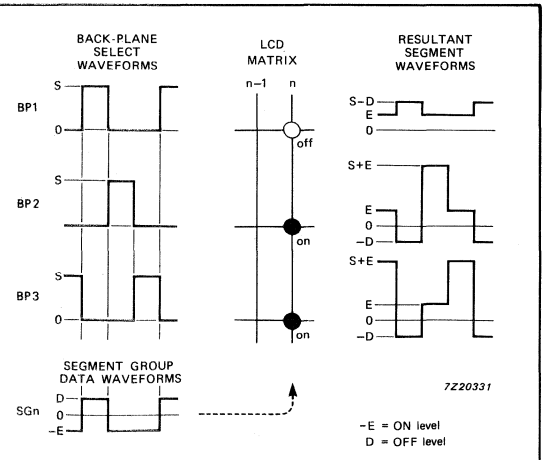


Fig.11 Row and column multiplexing waveforms for a display showing the voltage waveforms across individual elements.

Fig. 11 shows that all the elements receive a voltage, which means that the voltage at which non-selected elements remain OFF has been raised above zero. The ratio of the ON to OFF voltage (discrimination) decreases as the multiplex ratio increases (see **Table 1**) and the non-selected segments will become slightly visible. The discrimination can be optimized up to a certain limit, by increasing the number of multiplex levels.

Table 1 shows that the largest relative profit is obtained when going from direct drive to MUX 1:2. The number of connections is approximately halved, but a reasonably good discrimination is maintained (2.24). For this reason MUX 1:2 is popular for displays up to 100...150 segments (higher MUX rates would give little or no advantage, while reducing the contrast relatively fast).

Table 1 Discrimination and number of connections compared to the multiplex rate.

multiplex ratio	1:1	1:2	1:3	1:4	1:8
discrimination, $V_{on(RMS)}$ / $V_{off(RMS)}$	∞	2.24	1.92	1.73	1.45
number of connections required for a display having 120 segments	121	62	43	34	23

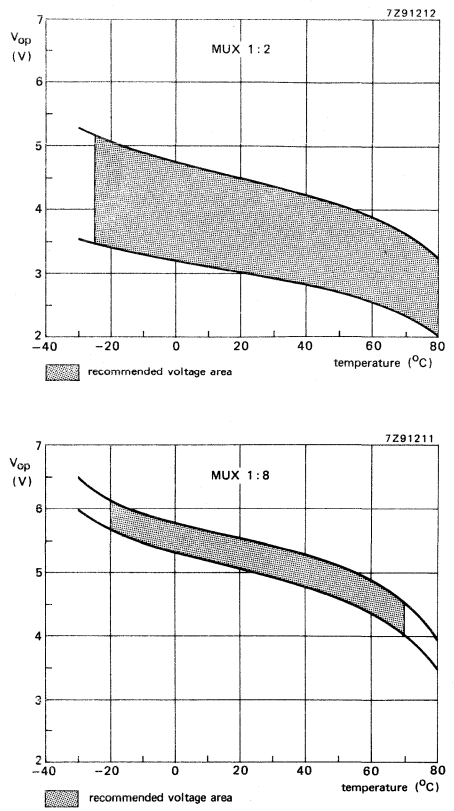


Fig.12 Typical recommended voltage areas for (a) 1:2 and (b) 1:8 MUX rates. At the lower boundary of each area the OFF segments become faintly visible at a viewing angle $\alpha = 40°$, $\phi = 270°$, while the ON elements are visible with a contrast better than 2 at $\alpha = 0°$.

ELECTRO-OPTICAL CHARACTERISTICS OF MULTIPLEXED LCDs

Most LCD applications require the OFF elements to remain invisible up to a certain viewing angle (α). In order to keep the OFF voltage below the threshold voltage (V_{th}) the value of the operating voltage (V_{op}) must not exceed a maximum criteria (Fig. 6). However, for ON elements a minimum contrast at a different viewing angle is required, which calls for a value of V_{op} that exceeds a minimum criteria. Since V_{th} is temperature dependent, both ON and OFF criteria of V_{op} vary with temperature (see Fig. 12 for MUX rates 1:2 and 1:8). The area between the ON and OFF criteria is the recommended voltage area as it represents invisible OFF segments, and ON segments with sufficient contrast.

At low multiplex ratios satisfactory operation over a wide temperature range can be obtained with a fixed value of V_{op}. However, in order to obtain a contrast viewing cone throughout the same temperature range at higher MUX ratios, V_{op} has to be temperature compensated to allow for the negative temperature coefficient of V_{th}.
As well as its effects on the operating voltage and temperature range, increased multiplexing also narrows the viewing cone (Fig. 13 and Fig. 14).

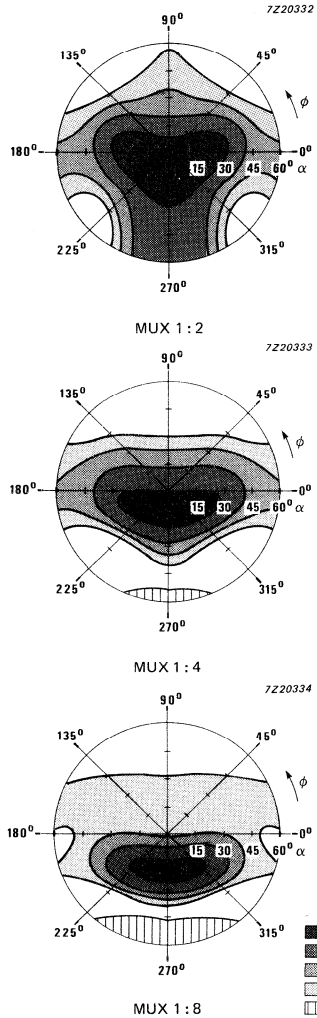


Fig.13 Isocontrast diagrams for various MUX ratios.

The effect of OFF segments being visible depends upon the type of display pattern. In a segment display incorrect information can be displayed and the MUX ratios are, therefore, normally limited to 1:8. In character or full matrix dot displays visible OFF segments can lead to a somewhat darker background. This may be disturbing but the information will remain correct and legible up to MUX rates of 1:100. Satisfactory operation at higher MUX ratios is obtained using advanced technologies such as STN.

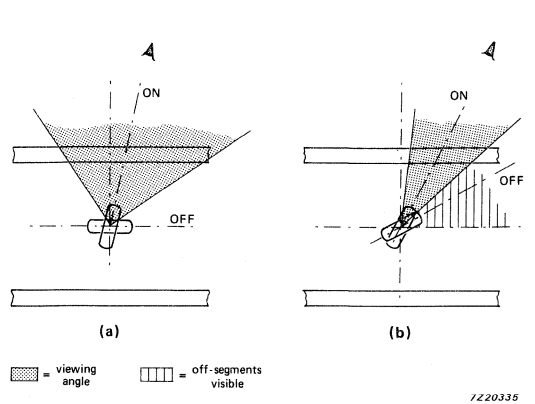


Fig.14 Angular variations of the center liquid crystal molecule (a) direct drive (b) MUX drive

DERIVED TECHNOLOGIES

Super Twisted Nematic (STN) displays

The main limiting factor in the use of multiplexed TN displays is the gradual slope of the contrast as a function of the voltage curve. It has been discovered that this curve can be made much steeper by increasing the twist angle of the liquid crystal beyond 90° to a value ranging between 180 and 270°.
The larger twist angle is achieved using a special cholesteric doped nematic liquid crystal. The cholesteric molecules have a helical screw structure (Fig. 2) which helps to ensure that all the liquid crystal molecules twist in the same direction and have the same stable state.

STN displays use birefringence effect which introduces wavelength dependence and characteristic colour into the display. With optimized polarizer angles the display will, for example, appear blue on a bright background (blue mode), or bright yellow on a yellow background (yellow mode).
STN displays can produce images with a good contrast over wide viewing angles, at MUX rates of 1:100 or higher.

Guest-Host displays (GHD)

Two problems associated with TN displays are the angular dependence of the contrast and the relatively low brightness. These are both caused by the use of two polarizers. An alternative type of display is the GHD which works with

one or no polarizers. In GHDs the molecules of a dichroic dye (guest) are dissolved into the nematic liquid crystal (host). The guest molecules always align themselves parallel to the molecules of the liquid crystal.
When there is no voltage applied the molecules are aligned parallel to the display surface (OFF-state); certain wavelengths of the incident light are absorbed by the dye and the display appears coloured. When sufficient voltage is applied the molecules will align perpendicular to the display (ON-state), the dye will no longer absorb the light and the display will appear bright (Fig. 15). Typically GHDs have bright segments on a coloured background, the colour of which depends upon the dye and may include black.

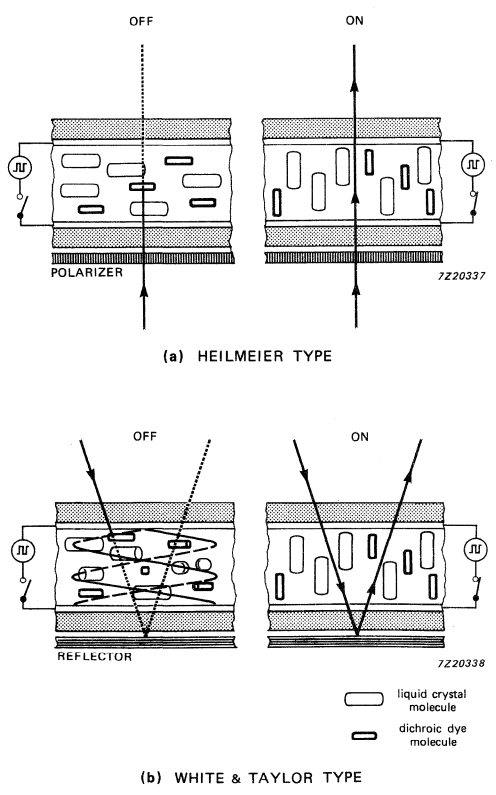


Fig.15 Operation of a GHD (a) Heilmeier (b) White and Taylor.

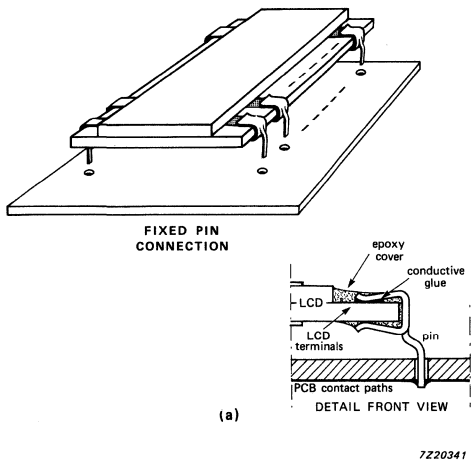
There are two main types of GHD:
- Heilmeier (Fig. 15(a)) which requires a front polarizer for good legibility and must have good back-lighting or be viewed in high ambient light conditions
- White and Taylor (Fig. 15(b)) which is optimized for reflective operation because it does not require polarizers and produces very bright segments against a coloured or grey background.

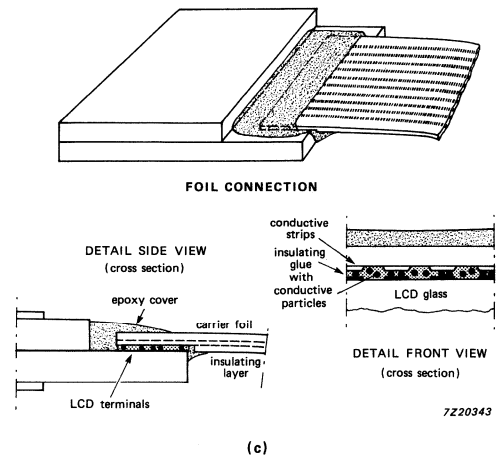
The advantage of GHDs over TN displays is the very wide and regular viewing cone. Disadvantages are the higher operating voltage and poor multiplexability.

CONNECTING TECHNIQUES

The terminals of an LCD are Indium/Tin Oxide and are situated on at least one side of the cell.
The three main methods used to electrically connect LCDs are: fixed pins, conductive rubber (elastomer) strips or foil.
Fixed pins are glued directly onto the LCD which can then be soldered on to a PC-board or connected via snap-on sockets (Fig. 16(a)). They are suitable for LCDs with a relatively low number of connections and when the glass length is enough to accommodate the required number of pins. However, they provide a reliable method of contact.
Elastomer connectors consist of alternate conductive and insulating sections which support the LCD and connect it to the PC-board (Fig. 16(b)). The contacts of the LCD are on the underside of the top glass and these connect to the PC-board via the conducting sections of the elastomer strip. Contact is maintained by mounting a bezel or clamp which squeezes the LCD, elastomer strip and the PC-board together. For the interconnection between PC-board and LCD, care must be taken to ensure that a constant pressure is maintained over all the connections; this requires special attention in the case of long displays. Without optical alignment a contact pitch down to about 1 mm can be used and down to about 0.5 mm with optical alignment.

Foil connectors (Fig. 16(c)) provide a flexible method for the connection of LCDs. They consist of parallel conductors mounted on a foil which is glued directly on to the LCD; the contact area is thus sealed from the atmosphere. Connection pitches at each end of the foil can vary and the drivers can be mounted on a remote PC-board which is advantageous when a very thin display or back-lighting is required.





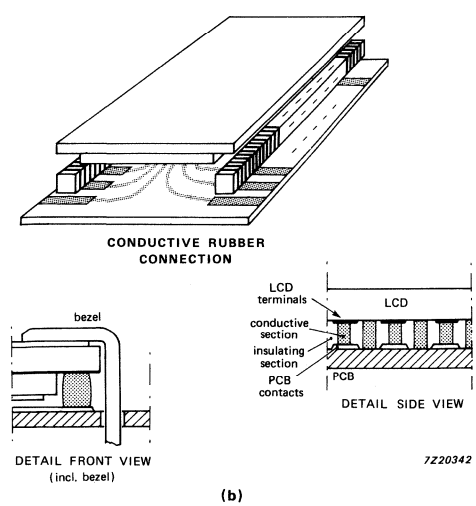


Fig.16 Connection techniques:

(a) fixed pin – displays with glued-on pins having a contact pitch of 2.54 mm that can be soldered directly into a PC-board

(b) elastomer (conductive rubber) – also known as zebra strips, clamped between LCD and PC-board at least one conductive layer will connect matched contact pads whilst at least one insulator will isolate adjacent circuits

(c) foil – removes the need for an adjacent PC-board and allows a display to be very thin.

MOUNTING AND ILLUMINATION TECHNIQUES

Reflective and transflective displays should be mounted as close as possible to the front surface of the equipment to gain maximum illumination from the ambient light. When choosing a mounting position the viewing angle and isocontrast diagram published in the LCD data sheet must be considered. Auxiliary front lighting for a reflective display should be at an angle close to the normal viewing direction to minimize reflection and shadow effects. Mounting pressure applied to LCDs using elastomer connectors should be as even as possible and pressure on the seal or the viewing areas must be avoided. Glass or non-birefringent plastic should be used to protect the front polarizers from scratches and humidity.

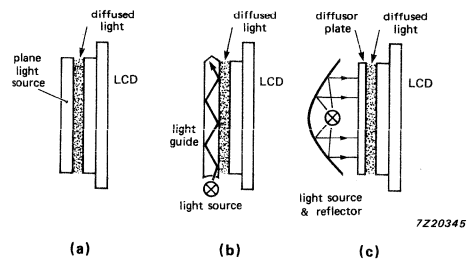


Fig.17 Back-lighting methods

Back-lighting

Back-lighting of a transflective display is necessary to maintain legibility under poor environmental light conditions.

The main methods used for LCD back-lighting are:
- electro-luminescent light source; has the advantage that it is very thin and emits a diffuse and evenly distributed light; however, its luminance is low, it requires a supply of 100 to 200 V at a few hundred Hz and it has a limited life (Fig. 17(a))
- light guide; a point source such as an LED or a linear source such as a fluorescent tube is distributed by a light guide using total reflection; its construction can be flat so little space is required behind the LCD; however; uniform light distribution can be difficult to obtain and light loss can be considerable (Fig. 17(b))
- light box; an LED, halogen or fluorescent light is distributed by a light box; this light source is very effective but needs considerable space immediately behind the display (Fig. 17(c)).

Any form of back-lighting for LCDs requires considerably more power than is used by an unlit display. This is a limiting factor when using a battery power supply.

Module user guide

Liquid Crystal Displays — Module user guide

INTRODUCTION TO LCD MODULES

An LCD module is a liquid crystal display complete with driving circuitry and, in many applications, decoding and control circuitry, which assists interfacing.
Typical applications for LCD modules include industrial display equipment, pocket VDUs, portable computers, telephony equipment, typewriters and point of sales equipment.
The internal inter-connection between driving circuitry and display can be elastomer (zebra stripes) or flex foil. One of the advantages of an LCD module over a loose display is that less external connections are required, allowing a mounting location which is remote from the control circuit.

The use of a complete LCD module in display equipment means a great deal less time in designing the display into the equipment, as all driving circuitry is internal and interface to a microprocessor is the design engineers only concern.

All of our modules are light and compact and can be easily mounted into display equipment. They have a good contrast over wide viewing angles.

We offer our modules in three display modes:

(i) segment display modules
(ii) character display modules
(iii) flat panels

For each mode we have standard types available which are listed in **Table 2.**

Table 2 LCD module types

DESCRIPTION	ILLUM. MODE	CLASS	TYPE NUMBER
1-line, 16-digit	reflective	segment	LTM233R-10
1-line, 16-character	reflective, 6 o'clock	character	LTN111R-10
	transflective, 6 o'clock		LTN111F-10
	reflective 12 o'clock		LTN111R-50
	transflective, 12 o'clock		LTN111F-50
2-line, 16-character	reflective, 6 o'clock	character	LTN211R-10
	transflective, 6 o'clock		LTN211F-10
	reflective, 12 o'clock		LTN211R-50
	transflective, 12 o'clock		LTN211F-50
2-line, 20-character	reflective	character	LTN221R-10
	transflective		LTN221F-10
2-line, 24-character	reflective	character	LTN222R-10
	transflective		LTN222F-10
2-line, 40-character	reflective, 6 o'clock	character	LTN243R-10
	transflective, 6 o'clock		LTN243F-10
	reflective, 12 o'clock		LTN243R-50

SEGMENT DISPLAY MODULES

Features

- Serial interface e.g. C-bus and I²C-bus
- Low MUX rate hence good contrast and viewing angle, especially in high ambient light conditions
- Low drive voltage
- Light, compact and easy to mount

Description

Segment display modules are intended for use in numeric applications (though the design can include some fixed symbols). In comparison to character types the restriction in data representation allows low MUX rates (up to 1:4), good contrast over wide viewing angles and low driving voltage. A typical application for segment display modules is in telephone sets, for displaying the dialled number.

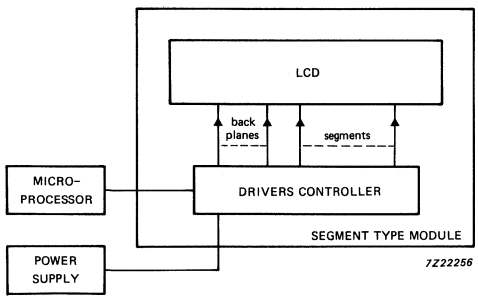


Fig.18 Configuration of segment type LCD.

CHARACTER DISPLAY MODULES

Features

- Interface with either 4-bit or 8-bit parallel data input (ASCII)
- Built in controller that includes a character generator and LCD driver functions
- Good legibility in bright light
- Light and compact and easy to mount

Description

Character liquid crystal display modules (also known as alpha-numeric displays) are light and compact modules with a controller, including a character generator, LCD driver LSI ICs and a character type LCD cell mounted on a single PC-board.
The built in character generator makes the design engineers task easier when incorporating one of our modules within his equipment. It is capable of generating 168-alphanumeric/Japanese characters and symbols (160 fixed characters and 8 user programmable characters).

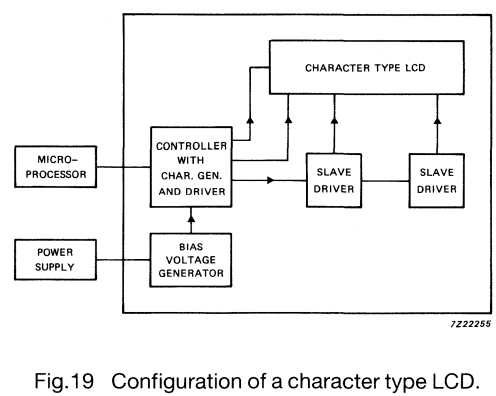


Fig.19 Configuration of a character type LCD.

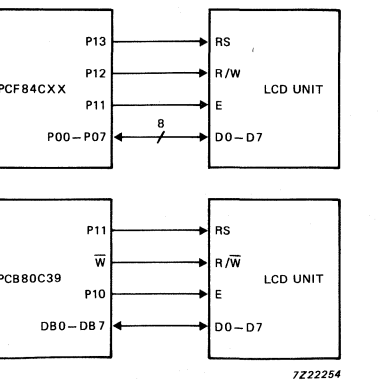


Fig.20 Microprocessor interface.

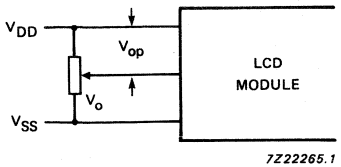


Fig.21 Power supply.

Our character display modules are offered with 1 or 2-lines of characters and a character font of 5 x 8 (5 x 7 dots + cursor). They can be interfaced with a 4- or 8-bit microprocessor and have a 1:16 multiplex rate (refer to TP 238 for further details about character display modules).

i) Interface signals

RS	register select
R/W	read/write select
E	enable read/write
D0 to D7	input/output data

ii) Supply voltages

V_{DD}	positive supply voltage for logic
V_{SS}	logic ground
V_O	contrast adjustment voltage: operational LCD voltage, V_{op} equals $V_{op} = V_{DD} - V_O$ (Fig. 21).

FLAT PANELS

Features

- Full dot graphic display capability
- Good legibility in bright light
- Light and compact and easy to mount

Description

Flat panels (also known as dot matrix modules) are capable of displaying a wide variety of data as each individual dot can be controlled ON or OFF. The dot matrix LCD module is ideal for displaying diagrams, graphs and text.

The number of horizontal (rows) and vertical (columns) electrodes multiplied gives the number of pixels or dots, as a pixel or dot is located at the cross point of the electrodes. The MUX rate is determined by the number of electrodes on the short side of the display, which also determines the display technology.

To enable higher contrast when using a high MUX rate display, the dot areas are separated into two display halves (upper and lower). This necessitates doubling the data bits.

Description of input data and control signals

Currently we offer our dot matrix displays with 1-bit serial data input or 2 x 4-bit parallel data input.
On the falling edge of CP2 the input data is sequentially transferred into the shift register in the column drivers. On the falling edge of CP1 the data is latched and displayed.

The scan sequence is started by clocking signal FS in on the HIGH to LOW transition of clock pulse CP1, after which the first row is scanning and the second row information is clocked in by CP2.

When all the data of row 2 has been entered and latched on the falling edge of CP1, the display proceeds to scanning the second row.
The data input continues until the whole area of the display is filled and then proceeds to the next display face.

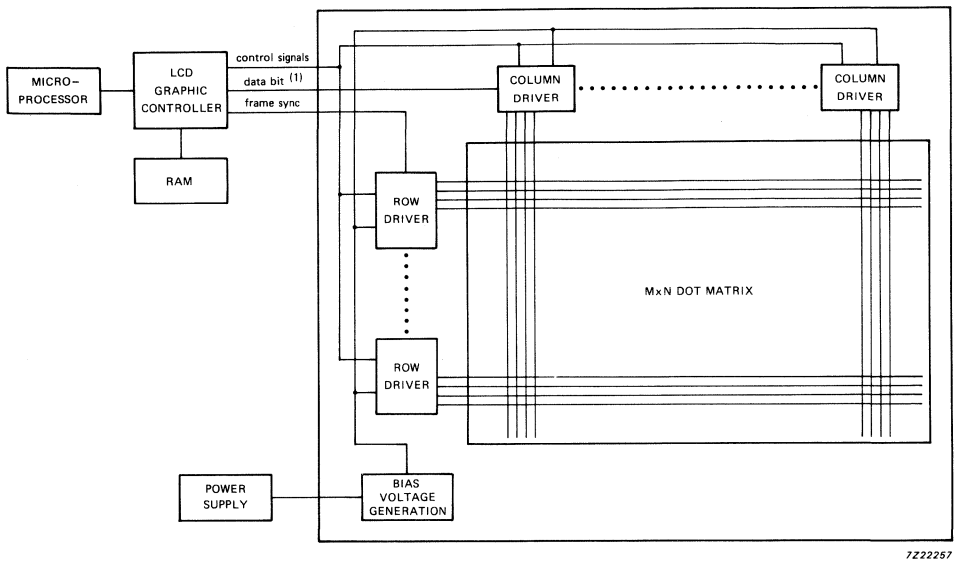


Fig.22 Configuration of a graphic display module when the MUX rate is equal to the number of rows. (1) 1-bit serial or 4-bit parallel.

i) Control signals (Fig. 24)

CP1	clock pulse 1 (latch)
CP2	clock pulse 2 (shift)
FS	frame synchronization
M	signal to convert the LCD drive waveform into AC

ii) Supply voltages

V_{DD}	positive supply voltage for logic
V_{SS}	logic ground
V_O	contrast adjustment voltage: operational LCD voltage, V_{op} equals $V_{op} = V_{DD} - V_O$

iii) Data inputs

a) module with a MUX rate equal to the number of rows (Fig. 22)	1-bit serial: used for displays with a relatively small number of dots; 4-bit parallel: used for displays with a larger number of dots
b) module with a MUX rate equal to half the number of rows (Fig. 23)	2 x 1-bit serial: used for displays with a relatively small number of dots; 2 x 4-bit parallel: used for displays with a larger number of dots.

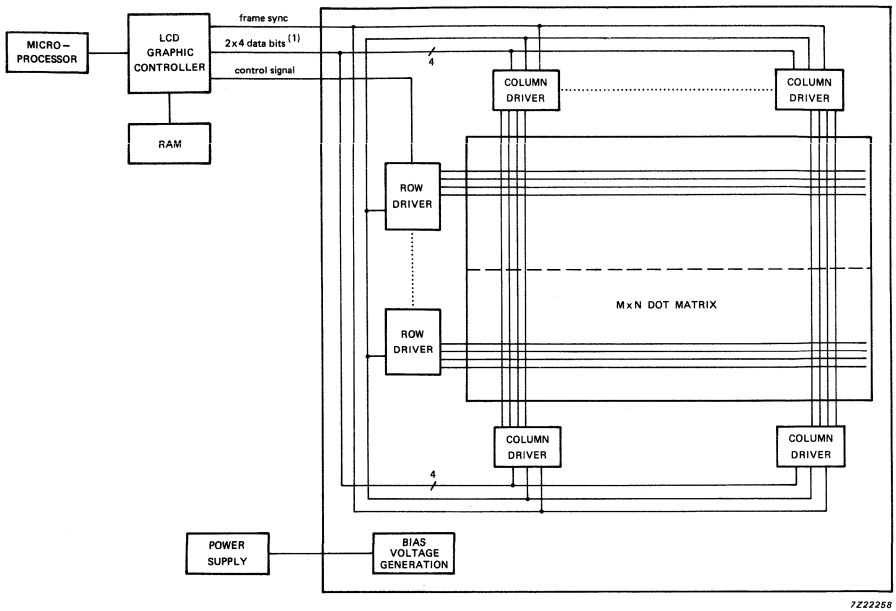


Fig.23 Configuration of a graphic display module when the MUX rate is half the number of rows (1) 2 x 1-bit serial or 2 x 4-bit parallel.

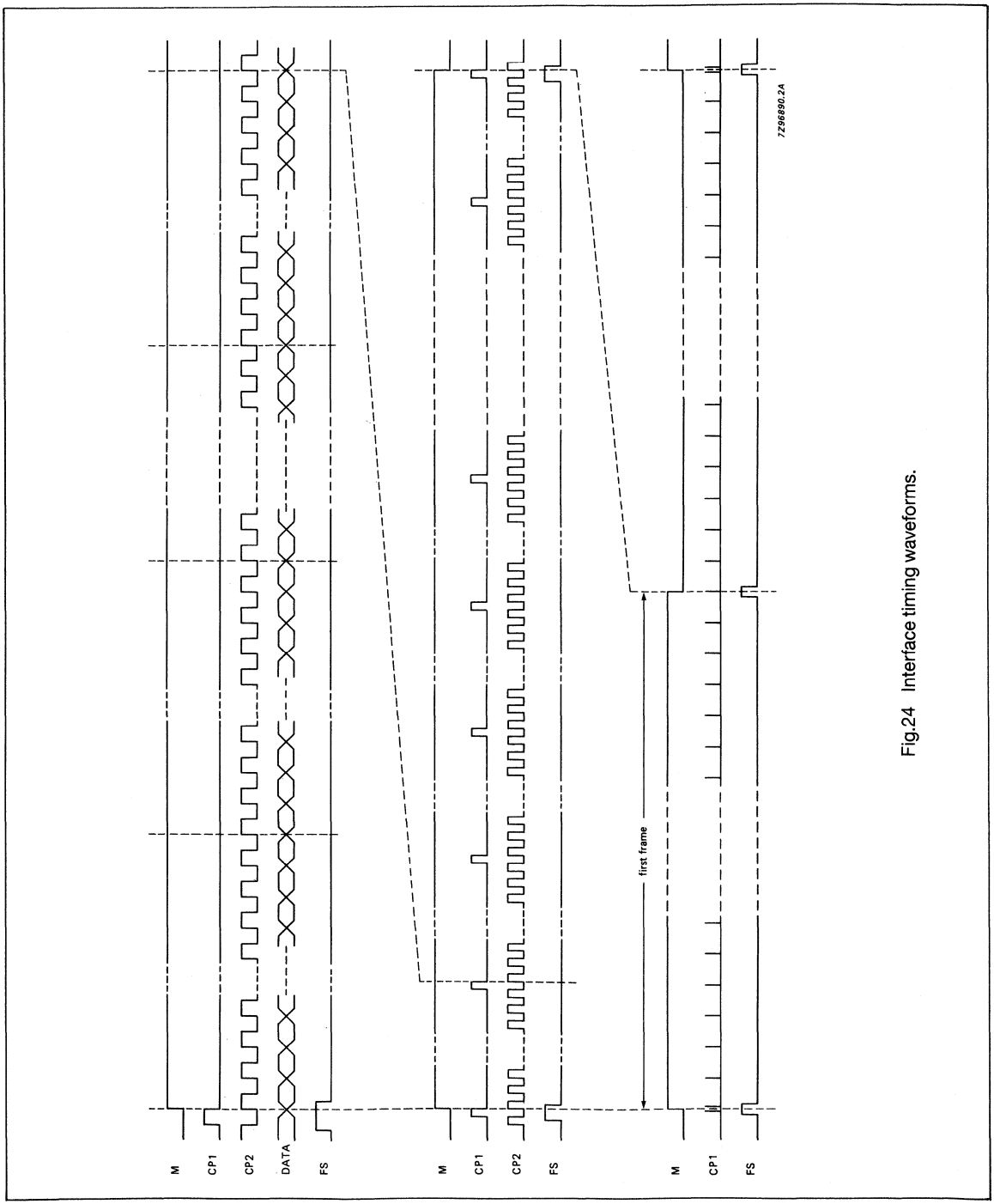


Fig.24 Interface timing waveforms.

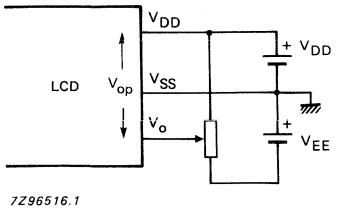


Fig.25 Power supply.

Quality

Liquid Crystal Displays — Quality

Note: for more detailed information refer to document 9398 359 30011 (General Quality Specification for Discrete Semiconductors LCD) URV-6-3-62/611 – Part E.

QUALITY IN DESIGN AND PRODUCTION

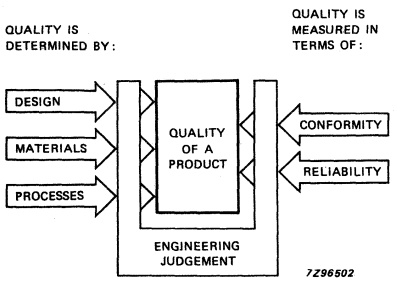


Fig.26 Quality of a product.

All appropriate aspects of quality are an integral part of our design rules for new LCD types, ensuring that quality is designed into our products from the beginning.
The development of each new type of LCD is finalized by a product release procedure, which reviews the quality of the design.

Our production quality assurance programme is based upon internationally accepted standards. The results of tests carried out during incoming inspection, at the in-line inspection and final acceptance stages are used as feedback in order to continually improve our process and design rules.

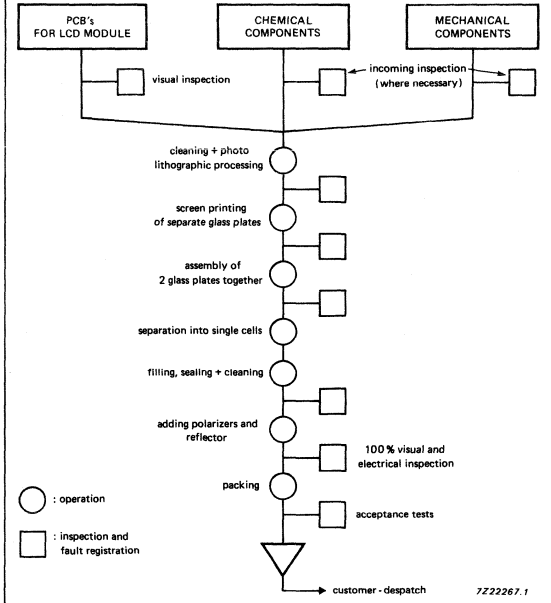


Fig.27 Simplified schematic.

PRODUCT RELEASE

To ensure that every LCD type fulfills its specified requirements, a product release procedure is carried out throughout the development of each new type.
This procedure guarantees that each product withstands an extensive programme of environmental tests in accordance with IEC standards, and a number of supplementary tests which are specific to LCDs.

The polarizers attached to the outside of the LCDs are available in distinct quality classes so we have also classified our LCDs into:
- commercial reliability grade
- extended reliability grade

Consequently there are differences in the product release tests (see Table 3).

Table 3 Product release tests in relation to the Quality Grade

TEST NAME	IEC-68	TEST DESCRIPTION		REMARKS
		COMMERCIAL GRADE	EXTENDED GRADE	
Change of temperature	2-14	–25 °C/30 min – +70 °C/30 min	–40 °C/30 min – +85 °C/30 min	10 times
Low temperature storage	2-1	–25 °C/dry/21 days	–40 °C/dry/21 days	
High temperature storage	2-2	+70 °C/dry/21 days +60 °C/dry/10 days	+85 °C/dry/21 days +90 °C/dry/21 days	depending upon type
Damp heat steady state	2-3	+40 °C/90 %RH/21 days +40 °C/90 %RH/10 days	+80 °C/90 %RH/10 days +60 °C/90 %RH/21 days +80 °C/90 %RH/21 days	depending upon type
Damp heat cyclic	2-30	--	25-40 °C/21 days/ 90-95 %RH	for fixed pin versions only
Sulphur dioxide	2-42	--	25 °C/75 %RH/25 ppm/ 10 days	
Low air pressure	2-13	+25 °C/500 mBar/2 days		
High pressure	–	+60 °C/5 Bar/1 hr.		
Leakage and seal-line adhesive strength	–	+25 °C/freon/3 hrs.		
Vibration	2-6	10-55 Hz/0.75 mm pp/2 hrs. per side		
Bump	2-29	6 ms/40 g peak/1000 times		

ACCEPTANCE TESTS

To ensure that the devices meet the electro-optical and mechanical specifications a statistical sampling is carried out prior to delivery, as described in ISO 2859. The following AQL levels apply:

- for inoperatives: AQL 0.25
- for other functional defects: AQL 0.65
- combined: AQL 1.0

Statistical sampling is also used to gather reliability data.

DEFINITION OF DEFECTS

Optical defects

Optical defects are defined as visible irregularities within the viewing area of a non-energized display. The limit of the acceptable size of an optical defect depends on the viewing distance and on the contrast of the optical defect. The acceptance criteria for optical defects are defined by means of limit samples, that represent aesthetic borderline conditions of LCDs when mounted in the finished product.
Limit samples for specific products can be agreed upon between the customer and the supplier.

Electro-optical defects

Electro-optical defects are defined as visible irregularities within the viewing area of a non-energized display. All segments must be visible perpendicular to the display at the specified minimum operating voltage, except for high MUX rate LCDs with a more specific viewing direction. In multiplex drive displays, non-selected segments must not be visible from the viewing angle specified for OFF conditions, except for high MUX rate LCDs with a more specific viewing direction.

Mechanical defects

Mechanical defects are defined as mechanical irregularities which do not influence the electrical or optical properties, but can cause mounting problems for the customer, if they do not meet the mechanical specification.

RELIABILITY

Conditions for long life operation

A lifetime of 10^5 hours can be expected under normal operating conditions:

- operating voltage and frequency must be within the specified ranges
- DC voltage must be less than 0.1 V
- operating ambient temperature range;
  5 to 40 °C for commercial reliability grade
  -5 to +55 °C for extended reliability grade
- relative humidity must be less than;
  60 % for commercial reliability grade
  75 % for extended reliability grade.

End of life definition

An LCD is to be considered at the end of its life if one of the following defects is found:

- optical or electro-optical defects
- electro-optical specifications are not met
- contrast is less than 50 % of its initial value
- total current consumption at T_{amb} = 25 °C exceeds more than twice the specified maximum value
- the clearing point of the liquid crystal is less than the specified maximum operating ambient temperature.

HANDLING ASPECTS

Unpacking

The instructions which are printed on the packaging should be followed.

Scratching

The front and rear sides of an LCD consist of polarizer and reflector foils; they are neither scratch nor pressure resistant, so avoid touching and treatment with rough or abrasive tools.

Fingerprints

Gloves should be worn when handling the displays as fingerprints on the polarizers can reduce the optical performance of the display, and fingerprints on the contact sides can cause connecting problems.

Protective foil

Usually the front polarizer of a display is provided with a protective, transparent foil (also the rear polarizer in transmissive mode LCDs). It should be kept in place as long as possible after the display has been removed from its original package, especially for temporary storage during manufacture. Ideally the protective foil should only be removed after the display is mounted in its final assembly. The foil can be removed using round tweezers, with which it should be lifted gently from a corner.

Cleaning

To clean a dirty LCD use a soft, clean, lint free, dry tissue. Loose dust may be removed with a clean, soft blower brush. If these methods are not sufficient then a tissue moistened with lead free benzine, petrol or freon, applied softly to the surface should be sufficient.
Other solvents, or water should be avoided as they may attack the polarizers.

Glass breakage/safety

LCDs are made of glass. Handle with care to avoid breakage or cracks. If a display is broken use an alcohol- or acetone-soaked tissue to remove the escaped fluid. This fluid may be toxic, avoid direct skin contact. Clean contaminated areas immediately with soap and warm, running water.

Storage precautions

LCDs should be kept in their original package and in a dust-free environment. For long term storage temperature should not exceed 45 °C and relative humidity should not exceed 40-50 %.
Avoid long term storage in direct sunlight, or fluorescent light; a yellow acryl box lends itself as a light, shock and dust protecting storage container.
Avoid moving a display from a cold storage area to a humid or hot storage area as it leads to condensation which can attack the polarizers.

MOUNTING ASPECTS

Housing

Housing and frame dimensions should be well adapted to the size of the display to ensure proper mounting. Mechanical pressure should be moderate and should be applied evenly between the frame and the full length of the display. No pressure should be exerted on the seal or on the display areas.
Module housings and frames have to be designed in such a way that bending of the display in the mounted position is avoided.
LCDs should preferably be housed with a transparent plate, e.g. glass or non-birefringent acrylic plate, mounted in front of the display to protect it from scratches, humidity and dirt.

Conductive rubber connections

Mounting instructions from the manufacturers of elastomeric connectors (conductive rubber 'zebra') have to be followed. Special attention should be given to prescribed contact pressure and its even spread over the full length of the contacting edges.

Soldering

When soldering LCDs with fixed pins, avoid temperature shocks. If using solder-wave equipment with preheating it may be necessary to cover the LCD to avoid exceeding the maximum storage temperature. As LCDs should not be washed it is recommended that the protective foil be left in place until after soldering as it helps to protect the display from solder flux splashes. Additional protection may be required.

Custom design guide

Liquid crystal displays — Custom design guide

page

INTRODUCTION TO CUSTOM DESIGN

The advantage of LCD technology over many other display technologies is the capability of supplying LCDs to specific customer requirements.

We offer a complete custom design service for LCD cells in which the following aspects can be customer specified:

- dimensions
- display pattern
- electro-optical characteristics
- connection methods

Customers wishing to order a custom design product or who require more information should contact our sales representative (see back of handbook for the address).

DEVELOPMENT PROCEDURE

Custom design projects consist of three main stages:

- product definition and quotation
- sample phase
- volume production

Product definition and quotation

In this phase our development department translates the customer requirements into a product specification (electro-optical characteristics and product drawing). This specification will enable assessment and will be offered to the customer as part of the final commercial quotation.

Sample phase

Once the final quotation has been accepted samples of the product will be made according to the agreed specification. The customer will be required to give formal approval of the samples prior to the volume production phase.

Volume production

Preparations for volume production will begin once the sample approval has been gained and the deliveries will begin after a specified lead time.

TECHNICAL ASPECTS OF CUSTOM DESIGN

Only basic aspects of **custom design** are outlined in this section. For more details please contact our local sales organization.

Mechanical data

There are three contact methods available for LCDs:
- for elastomer connection (see Fig.28 and Fig.29)
- with fixed pins (see Fig.30)
- with flexfoil (not shown)

Please see **Table 7** for an outline of possible dimensions. Please contact our local sales organization for preferred glass sizes.

Ratings

Maximum voltage between any two contacts	V_{max}	10 V RMS
Storage temperature		
Commercial quality grade	T_{stg}	−25 to +70 °C
Extended quality grade	T_{stg}	−40 to +85 °C

Electro-optical data

A range of standard specifications are available with the following optical description (see Table 5).

Full specifications are given in the chapter "Family Characteristics", except for **TU1, TU2** and **TU3.** A quick reference survey is given in **Table 6**, for convenience. Other specifications are available on special request.

Table 5 Survey of optical descriptions

PARAMETER	FAMILY CHARACTERISTICS		
	TR1, TR2, TR3	TF1, TF2, TF3	TU1, TU2, TU3
image mode illumination mode antiglare surface	positive reflective no	positive transflective no	negative transmissive no

Table 6 Quick reference survey

PARAMETER	SYMB.	FAMILY CHARACTERISTICS								UNIT
		TR1, TF1, TU1				TR2, TF2, TU2			TR3, TF3, TU3	
drive method	-	DD	1:2	1:3	1:4	DD	1:3	1:4	1:2	-
operating voltage	V_{op}	2.5-6	2.6	2.8	3.2	3.5	4.0	4.3	5	V
ambient operating temp. minimum	T_{amb}	−10	−10	−10	−10	−25	−25	−25	−25	°C
maximum	T_{amb}	60	55	55	40	80	65	50	80	°C
quality grade	-	commercial				extended			extended	-

Pattern dimensions

Minimum distance between segments without leads is between:
- both segments relating to the same backplane 0.2 mm
- both segments relating to a different backplane 0.3 mm
- with one lead in between 0.35 mm

Minimum distance between symbols depends upon the number of leads between the leads
Minimum distance between segments and viewing area border 1.0 mm
Positional tolerance of graphic elements with respect to each other +/-0.1 mm
Tolerance of graphics in relation to nominal glass edge position +/-0.2 mm

Terminal connections

If a symbol occurs more than once within a multiplexed LCD our development department will use the same segment-to-backplane assignment; this standard procedure simplifies the driver software because only one 'look-up' table is required.
As LCD technology allows only single layer interconnection tracks, customer requirements on segment to backplane assignment and on terminal connections may collide with LCD track routing restrictions. In order to obtain optimal LCD design and thereby, optimal optical appearance, the customer is advised to specify only minimum requirements on these aspects. If any additional requirements or preferences are indicated separately, our design department will advise accordingly.

Preferred letter types are:

- Akzidenz-grotesk stnd
- **Eurostyle bold**
- ***Futura bold italic***
- Helvetica medium
- Helvetica medium condensed
- *Helvetica medium italic*
- Univers 57
- **Univers 67**
- ***Univers 68***
- **univers 75**

Table 7 Dimensions for **Custom Design** (see Fig.28, Fig.29 and Fig.30)
If more than one nominal value is stated the customer has a free choice of values, unless otherwise specified.

DESCRIPTION	DIMENSION	NOMINAL VALUE (mm)	TOLERANCE +/- (mm)
length	A	38 to 160 (note 2)	0.3
height	B	18 to 120 (note 2)	0.3
width of contact strip	L	≥2 (note 2)	0.3
border viewing area	A-X	≥2 (note 2)	-
glass thickness	D	1.1 (note 2)	0.1
	D	0.7 (note 2)	0.1
rear polarizer thickness - reflective or transflective - transmissive	 G G	 0.3 0.2	 0.05 0.05
pitch of contacts for conductive rubber connection	N (note 1) N (note 1) N (note 1) N (note 1)	1.0 1.27 1.8 2.54	- - - -
width of contact for conductive rubber connection - for N = 1.0 mm - for N = 1.27 mm - for N = 1.8 mm - for N = 2.54 mm		 0.5 0.6 0.9 1.5	 - - - -

Notes:

1. Accumulated tolerance over the complete row of contacts = 0.1 mm
2. Not all combinations of these dimensions are allowed. Please contact our local sales organization for details.

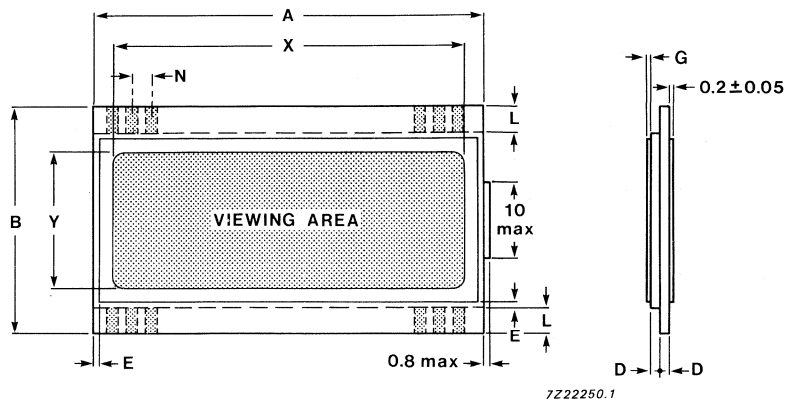


Fig.28 Version a, for conductive rubber connection, contacts top and bottom.

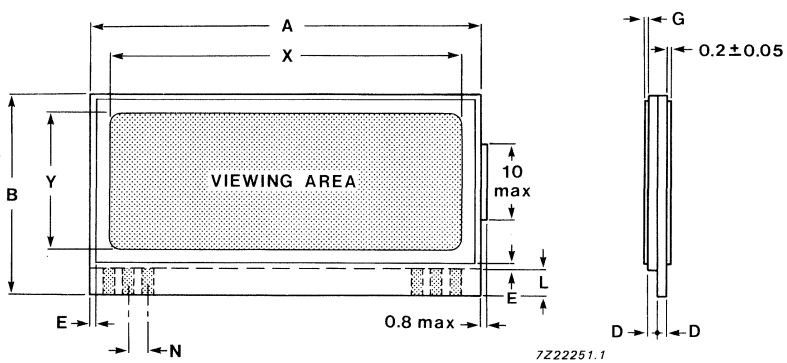


Fig.29 Version b, for conductive rubber connection, contacts bottom only.

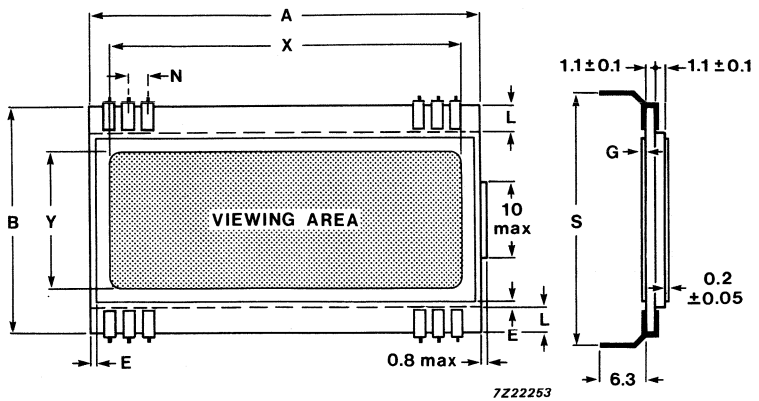


Fig.30 Version c, with fixed pins,contacts top and bottom.

Family characteristics

Liquid crystal displays — Family characteristics

INTRODUCTION

Standard range LCD cells are offered in two quality grades: commercial (over the commercial temperature range) and extended (over the extended temperature range). The following chapter contains the variations in operating characteristics for the two grades, in three illumination modes.

Note: The test conditions for these specifications have changed since the previous issue. The old and new conditions for LCDs with a positive image mode, where the ON-segments have a low brightness and the OFF-segments and background have a high brightness, are listed below.

The modified angle for specifying the ON-segments is more in line with the optical asymmetry of TN LCDs and with average application requirements.
In the new situation the switching speed is measured under the recommended operating conditions, rather than using fixed voltages.
Both changes are in line with developments in international standardization for LCD specification methods.

Due to these modified conditions many of the specification values have changed. However, please note that the **products themselves have not changed**.

TEST CONDITION	SYMBOL	OLD	NEW	UNIT
Measuring angle for ON-segment parameters	α	0	10	°
Measuring angle for OFF-segment parameters	α	40	40	°
Relative ON-segment brightness	B_{on}	10	10	%
Relative OFF-segment brightness	B_{off}	50	50	%
RMS voltage at which the switching speed is measured	V_{on}	4.5	note 1	V (RMS)
	V_{off}	0	note 1	V (RMS)
Recommended operating voltage	$V_{op\ typ}$	note 2	note 2	

Notes:

1. as determined by the recommended operating voltage and drive method
2. is specified to fulfill the values of B_{on} and B_{off} over the specified operating ambient temperature range (old and new situation)
3. all parameters are measured for $\phi = \phi_{pref}$

QUICK REFERENCE DATA

	ILLUMINATION MODE	RELIABILITY GRADE	DAMP HEAT STEADY STATE T_{amb}/R.H./duration	LOW TEMPERATURE STORAGE T_{amb}/duration	HIGH TEMPERATURE STORAGE T_{amb}/duration
TR0	reflective	commercial	+40 °C/90%/21 days	-25 °C/21 days	+70 °C/21 days
TF0	transflective	commercial	+40 °C/90%/21 days	-25 °C/21 days	+70 °C/21 days
TR1	reflective	commercial	+40 °C/90%/21 days	-25 °C/21 days	+70 °C/21 days
TF1	transflective	commercial	+40 °C/90%/21 days	-25 °C/21 days	+70 °C/21 days
TR2	reflective	extended	+80 °C/90%/21 days	-40 °C/21 days	+85 °C/21 days
TF2	transflective	extended	+80 °C/90%/21 days	-40 °C/21 days	+85 °C/21 days
TR3	reflective	extended	+80 °C/90%/21 days	-40 °C/21 days	+85 °C/21 days
TF3	transflective	extended	+80 °C/90%/21 days	-40 °C/21 days	+85 °C/21 days

CONSTANT DRIVE VOLTAGE

Optical description

Illumination mode:	reflective
Image mode:	positive
Front surface:	glossy
Quality grade:	commercial

Electro-optical characteristics for constant drive voltage

Typical values at T_{amb} = 25 °C; $V_{op} = V_{op\ typ}$; f_{dr} = 100 Hz; α = 10 °, unless otherwise stated.

PARAMETER	SYMBOL		DRIVE METHOD DD*	UNIT	NOTE
operating voltage	V_{op}	min	3.5	V	1
		typ	5.0	V	
		max	6.5	V	
operating ambient temperature	T_{amb}	min	−10	°C	
		max	+60	°C	
turn on time					
at T_{amb} = 25 °C	t_{on}		25	ms	2
at T_{amb} = 0 °C	t_{on}		100	ms	
turn off time at T_{amb} = 25 °C	t_{off}		40	ms	2
at T_{amb} = 0 °C	t_{off}		120	ms	
specific current consumption	I_S		24	nA/mm²	
frame frequency	f_{dr}	min	30	Hz	1
		max	200	Hz	
viewing angles for $C_R > 3$					
$\phi = \phi_{pref}$	α		60	o	3
$\phi = \phi_{pref}$ +180°	α		30	o	
$\phi = \phi_{pref}$ +270° or +90°	α		35	o	

* DD = direct drive

Notes:

1. For definition see Fig. 31.
2. For definition see Fig. 32.
3. For definition see Fig. 33.

Liquid Crystal Displays — Family characteristics - TF0

CONSTANT DRIVE VOLTAGE

Optical description

Illumination mode: transflective
Image mode: positive
Front surface: glossy
Quality grade: commercial

Electro-optical characteristics for constant drive voltage

Typical values at T_{amb} = 25 °C; $V_{op} = V_{op\ typ}$; f_{dr} = 100 Hz; α = 10 °, unless otherwise stated.

PARAMETER	SYMBOL		DRIVE METHOD DD*	UNIT	NOTE
operating voltage	V_{op}	min	3.5	V	1
		typ	5.0	V	
		max	6.5	V	
operating ambient temperature	T_{amb}	min	−10	°C	
		max	+60	°C	
turn on time					
at T_{amb} = 25 °C	t_{on}		25	ms	2
at T_{amb} = 0 °C	t_{on}		100	ms	
turn off time					
at T_{amb} = 25 °C	t_{off}		40	ms	2
at T_{amb} = 0 °C	t_{off}		120	ms	
specific current consumption	I_S		24	nA/mm^2	
frame frequency	f_{dr}	min	30	Hz	1
		max	200	Hz	
viewing angles for $C_R > 3$					
$\phi = \phi_{pref}$	α		55	o	3
$\phi = \phi_{pref}$ +180°	α		35	o	
$\phi = \phi_{pref}$ +270° or +90°	α		40	o	

* DD = direct drive

Notes:

1. For definition see Fig. 31.
2. For definition see Fig. 32.
3. For definition see Fig. 33.

CONSTANT DRIVE VOLTAGE

Optical description

Illumination mode: reflective
Image mode: positive
Front surface: glossy
Quality grade: commercial

Electro-optical characteristics for constant drive voltage

Typical values at T_{amb} = 25 °C; $V_{op} = V_{op\ typ}$; f_{dr} = 100 Hz; α = 10 °, unless otherwise stated.

PARAMETER	SYMBOL		DRIVE METHOD				UNIT
			DD*	1:2	1:3	1:4	
operating voltage	V_{op}	min	2.5	–	–	–	V
		typ	4.5	2.6	2.8	3.1	V (note 1)
		max	6.0	–	–	–	V
ambient operating temperature	T_{amb}	min	–10	–10	–10	–10	°C
		max	+60	+55	+55	+40	°C
turn on time							
at T_{amb} = 25 °C	t_{on}		35	160	240	190	ms (note 2)
at T_{amb} = 0 °C	t_{on}		170	970	1480	1270	ms
turn off time							
at T_{amb} = 25 °C	t_{off}		65	50	40	40	ms (note 2)
at T_{amb} = 0 °C	t_{off}		260	170	130	130	ms
specific current consumption	I_S		36	29	34	45	nA/mm^2
frame frequency	f_{dr}	min	30	30	30	30	Hz (note 1)
		max	200	100	100	100	Hz
viewing angle for CR > 3							
$\phi = \phi_{pref}$	α		55	35	35	35	° (note 3)
$\phi = \phi_{pref}$ +180°	α		45	20	5	0	°
$\phi = \phi_{pref}$ +90° or +270°	α		35	35	20	20	°

* DD = direct drive

Notes:

1. For definition see Fig. 31.
2. For definition see Fig. 32.
3. For definition see Fig. 33.

Liquid Crystal Displays — Family characteristics - TR1

TEMPERATURE COMPENSATED DRIVE VOLTAGE

Electro-optical characteristics for temperature compensated drive voltage

Typical values at T_{amb} = 25 °C; $V_{op} = V_{op\ typ} + TC.(T_{amb}-25)$; f_{dr} = 100 Hz; α = 10°, unless otherwise specified.

PARAMETER	SYMBOL		DRIVE METHOD			UNIT
			1:2	1:3	1:4	
operating voltage	$V_{op\ typ}$		2.9	3.1	3.1	V (note 1)
temperature coefficient of Vop	TC		−12	−13	−14	mV/°C
ambient operating temperature	T_{amb}	min	−10	−10	−10	°C
		max	+60	+60	+60	°C
turn on time						
at T_{amb} = 25 °C	t_{on}		90	145	190	ms (note 2)
at T_{amb} = 0 °C	t_{on}		430	550	810	ms
turn off time						
at T_{amb} = 25 °C	t_{off}		55	50	40	ms (note 2)
at T_{amb} = 0 °C	t_{off}		290	280	250	ms
frame frequency	f_{dr}	min	30	30	30	Hz (note 1)
		max	100	100	100	Hz

Notes:

1. For definition see Fig. 31.
2. For definition see Fig. 32.

Viewing angles as constant drive voltage.

Liquid Crystal Displays — Family characteristics - TF1

CONSTANT DRIVE VOLTAGE

Optical description

Illumination mode:	transflective
Image mode:	positive
Front surface:	glossy
Quality grade:	commercial

Electro-optical characteristics for constant drive voltage

Typical values at T_{amb} = 25 °C; $V_{op} = V_{op\ typ}$; f_{dr} = 100 Hz; α = 10 °, unless otherwise stated.

PARAMETER	SYMBOL		DRIVE METHOD				UNIT
			DD*	1:2	1:3	1:4	
operating voltage	V_{op}	min	2.5	–	–	–	V
		typ	4.5	2.6	2.8	3.1	V (note 1)
		max	6.0	–	–	–	V
ambient operating temperature	T_{amb}	min	–10	–10	–10	–10	°C
		max	+60	+55	+55	+40	°C
turn on time							
at T_{amb} = 25 °C	t_{on}		35	160	240	190	ms (note 2)
at T_{amb} = 0 °C	t_{on}		170	970	1480	1270	ms
turn off time							
at T_{amb} = 25 °C	t_{off}		65	50	40	40	ms (note 2)
at T_{amb} = 0 °C	t_{off}		260	170	130	130	ms
specific current consumption	I_S		36	29	34	45	nA/mm^2
frame frequency	f_{dr}	min	30	30	30	30	Hz (note 1)
		max	200	100	100	100	Hz
viewing angle for CR > 3							
$\phi = \phi_{pref}$	α		45	40	–	–	° (note 3)
$\phi = \phi_{pref}$ +180°	α		25	15	–	–	°
$\phi = \phi_{pref}$ +90° or +270°	α		35	40	–	–	°
$\phi = \phi_{pref}$	α_{opt}		–	–	20	20	°
$\phi = \phi_{pref}$	α_2-α_1		–	–	40	40	°

* DD = direct drive

Notes:

1. For definition see Fig. 31.
2. For definition see Fig. 32.
3. For definition see Fig. 33.

TEMPERATURE COMPENSATED DRIVE VOLTAGE

Electro-optical characteristics for temperature compensated drive voltage

Typical values at T_{amb} = 25 °C; $V_{op} = V_{op\ typ} + TC.(T_{amb}-25)$; f_{dr} = 100 Hz; α = 10°, unless otherwise specified.

PARAMETER	SYMBOL		DRIVE METHOD			UNIT
			1:2	1:3	1:4	
operating voltage	$V_{op\ typ}$		2.9	3.1	3.1	V (note 1)
temperature coefficient of V_{op}	TC		−12	−13	−14	mV/°C
ambient operating	T_{amb}	min	−10	−10	−10	°C
temperature		max	+60	+60	+60	°C
turn on time						
at T_{amb} = 25 °C	t_{on}		90	145	190	ms (note 2)
at T_{amb} = 0 °C	t_{on}		430	550	810	ms
turn off time						
at T_{amb} = 25 °C	t_{off}		55	50	40	ms (note 2)
at T_{amb} = 0 °C	t_{off}		290	280	250	ms
frame frequency	f_{dr}	min	30	30	30	Hz (note 1)
		max	100	100	100	Hz

Notes:

1. For definition see Fig. 31.
2. For definition see Fig. 32.

Viewing angles as for constant drive voltage.

Liquid crystal displays — Family characteristics - TR2

CONSTANT DRIVE VOLTAGE

Optical description

Illumination mode: reflective
Image mode: positive
Front surface: glossy
Quality grade: extended

Electro-optical characteristics for constant drive voltage

Typical values at T_{amb} = 25 °C; $V_{op} = V_{op\ typ}$; f_{dr} = 100 Hz; α = 10 °, unless otherwise stated.

PARAMETER	SYMBOL		DRIVE METHOD				UNIT
			DD*	1:2	1:3	1:4	
operating voltage	V_{op}	min	3.5	–	–	–	V
		typ	5.0	3.7	4.0	4.3	V (note 1)
		max	6.5	–	–	–	V
ambient operating temperature	T_{amb}	min	–25	–25	–25	–20	°C
		max	+80	+70	+65	+50	°C
turn on time							
at T_{amb} = 25 °C	t_{on}		25	75	125	115	ms (note 2)
at T_{amb} = 0 °C	t_{on}		100	320	495	535	ms
turn off time							
at T_{amb} = 25 °C	t_{off}		40	30	25	30	ms (note 2)
at T_{amb} = 0 °C	t_{off}		120	100	75	75	ms
specific current consumption	I_S		24	24	28	36	nA/mm^2
frame frequency	f_{dr}	min	30	30	30	30	Hz (note 1)
		max	200	100	100	100	Hz
viewing angle for CR > 3							
$\phi = \phi_{pref}$	ϕ		50	35	35	35	° (note 3)
$\phi = \phi_{pref}$ +180°	ϕ		40	25	25	25	°
$\phi = \phi_{pref}$ +90° or +270°	ϕ		30	35	30	20	°

* DD = direct drive

Notes:

1. For definition see Fig. 31.
2. For definition see Fig. 32.
3. For definition see Fig. 33.

TEMPERATURE COMPENSATED DRIVE VOLTAGE

Electro-optical characteristics for temperature compensated drive voltage

Typical values at T_{amb} = 25 °C; $V_{op} = V_{op\ typ} + TC.(T_{amb}-25)$; f_{dr} = 100 Hz; α = 10°, unless otherwise specified.

PARAMETER	SYMBOL		DRIVE METHOD			UNIT
			1:2	1:3	1:4	
operating voltage	$V_{op\ typ}$		4.1	4.3	4.3	V (note 1)
temperature coefficient of Vop	TC		−12	−14	−15	mV/°C
ambient operating temperature	T_{amb}	min	−25	−25	−25	°C
		max	+80	+80	+80	°C
turn on time						
at T_{amb} = 25 °C	t_{on}		45	95	115	ms (note 2)
at T_{amb} = 0 °C	t_{on}		205	365	465	ms
turn off time						
at T_{amb} = 25 °C	t_{off}		35	30	30	ms (note 2)
at T_{amb} = 0 °C	t_{off}		100	85	70	ms
frame frequency	f_{dr}	min	30	30	30	Hz (note 1)
		max	100	100	100	Hz

Notes:

1. For definition see Fig. 31.
2. For definition see Fig. 32.

Viewing angles as for constant drive voltage.

Liquid Crystal Displays — Family characteristics - TF2

CONSTANT DRIVE VOLTAGE

Optical description

Illumination mode:	transflective
Image mode:	positive
Front surface:	glossy
Quality grade:	extended

Electro-optical characteristics for constant drive voltage

Typical values at T_{amb} = 25 °C; $V_{op} = V_{op\ typ}$; f_{dr} = 100 Hz; α = 10 °, unless otherwise stated.

PARAMETER	SYMBOL		DRIVE METHOD				UNIT
			DD*	1:2	1:3	1:4	
operating voltage	V_{op}	min	3.5	–	–	–	V
		typ	5.0	3.7	4.0	4.3	V (note 1)
		max	6.5	–	–	–	V
ambient operating temperature	T_{amb}	min	–25	–25	–25	–20	°C
		max	+80	+70	+65	+50	°C
turn on time							
at T_{amb} = 25 °C	t_{on}		25	75	125	115	ms (note 2)
at T_{amb} = 0 °C	t_{on}		100	320	495	535	ms
turn off time							
at T_{amb} = 25 °C	t_{off}		40	30	25	30	ms (note 2)
at T_{amb} = 0 °C	t_{off}		120	100	75	75	ms
specific current consumption	I_S		24	24	28	36	nA/mm^2
frame frequency	f_{dr}	min	30	30	30	30	Hz (note 1)
		max	200	100	100	100	Hz
viewing angle for CR > 3							
$\phi = \phi_{pref}$	α		50	50	45	45	° (note 3)
$\phi = \phi_{pref}$ +180°	α		15	10	5	5	°
$\phi = \phi_{pref}$ +90° or +270°	α		35	35	35	30	°

* DD = direct drive

Notes:

1. For definition see Fig. 31.
2. For definition see Fig. 32.
3. For definition see Fig. 33.

TEMPERATURE COMPENSATED DRIVE VOLTAGE

Electro-optical characteristics for temperature compensated drive voltage

Typical values at T_{amb} = 25 °C; $V_{op} = V_{op\ typ} + TC.(T_{amb}-25)$; f_{dr} = 100 Hz; α = 10°, unless otherwise specified.

PARAMETER	SYMBOL		DRIVE METHOD			UNIT
			1:2	1:3	1:4	
operating voltage	$V_{op\ typ}$		4.1	4.3	4.3	V (note 1)
temperature coefficient of V_{op}	TC		−12	−14	−15	mV/°C
ambient operating temperature	T_{amb}	min	−25	−25	−25	°C
		max	+80	+80	+80	°C
turn on time						
at T_{amb} = 25 °C	t_{on}		45	95	115	ms (note 2)
at T_{amb} = 0 °C	t_{on}		205	365	465	ms
turn off time						
at T_{amb} = 25 °C	t_{off}		35	30	30	ms (note 2)
at T_{amb} = 0 °C	t_{off}		100	85	70	ms
frame frequency	f_{dr}	min	30	30	30	Hz (note 1)
		max	100	100	100	Hz

Notes:

1. For definition see Fig. 31.
2. For definition see Fig. 32.

Viewing angles as for constant drive voltage.

Liquid Crystal Displays — Family characteristics - TR3

CONSTANT DRIVE VOLTAGE

Optical description

Illumination mode:	reflective
Image mode:	positive
Front surface:	glossy
Quality grade:	extended

Electro-optical characteristics for constant drive voltage

Typical values at T_{amb} = 25 °C; $V_{op} = V_{op\ typ}$; f_{dr} = 100 Hz; α = 10 °, unless otherwise stated.

PARAMETER	SYMBOL		DRIVE METHOD 1:2	UNIT
operating voltage	V_{op}	min	–	V(DC)
		typ	5.0	V(DC) (note 1)
		max	–	V(DC)
ambient operating temperature	T_{amb}	min	–25	°C
		max	+80	°C
turn on time				
at T_{amb} = 25 °C	t_{on}		85	ms (note 2)
at T_{amb} = 0 °C	t_{on}		290	ms
turn off time				
at T_{amb} = 25 °C	t_{off}		25	ms (note 2)
at T_{amb} = 0 °C	t_{off}		75	ms
specific current consumption	I_S		25	nA/mm^2
frame frequency	f_{dr}	min	30	Hz (note 1)
		max	100	Hz
viewing angle for CR > 3				
$\phi = \phi_{pref}$	α		35	° (note 3)
$\phi = \phi_{pref}$ +180°	α		20	°
$\phi = \phi_{pref}$ +90° or +270°	α		35	°

* DD = direct drive

Notes:

1. For definition see Fig. 31.
2. For definition see Fig. 32.
3. For definition see Fig. 33.

Liquid Crystal Displays — Family characteristics - TF3

CONSTANT DRIVE VOLTAGE

Optical description

Illumination mode: transflective
Image mode: positive
Front surface: glossy
Quality grade: extended

Electro-optical characteristics for constant drive voltage

Typical values at T_{amb} = 25 °C; $V_{op} = V_{op\ typ}$; f_{dr} = 100 Hz; α = 10 °, unless otherwise stated.

PARAMETER	SYMBOL		DRIVE METHOD 1:2	UNIT
operating voltage	V_{op}	min	–	V(DC)
		typ	5.0	V(DC) (note 1)
		max	–	V(DC)
ambient operating temperature	T_{amb}	min	–25	°C
		max	+80	°C
turn on time				
at T_{amb} = 25 °C	t_{on}		85	ms (note 2)
at T_{amb} = 0 °C	t_{on}		290	ms
turn off time				
at T_{amb} = 25 °C	t_{off}		25	ms (note 2)
at T_{amb} = 0 °C	t_{off}		75	ms
specific current consumption	I_S		25	nA/mm^2
frame frequency	f_{dr}	min	30	Hz (note 1)
		max	100	Hz
viewing angle for CR > 3				
$\phi = \phi_{pref}$	α		35	o
$\phi = \phi_{pref}$ +180°	α		15	o
$\phi = \phi_{pref}$ +90° or +270°	α		35	o

* DD = direct drive

Notes:

1. For definition see Fig. 31.
2. For definition see Fig. 32.
3. For definition see Fig. 33.

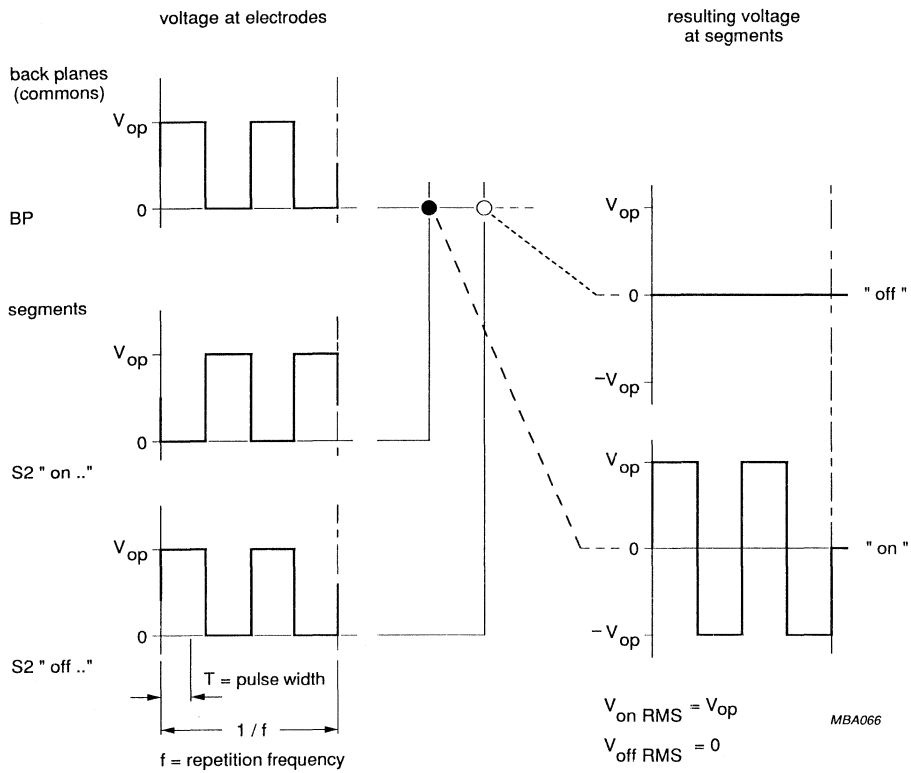


Fig.31 (a) Typical waveforms of V_{op} for static drive.

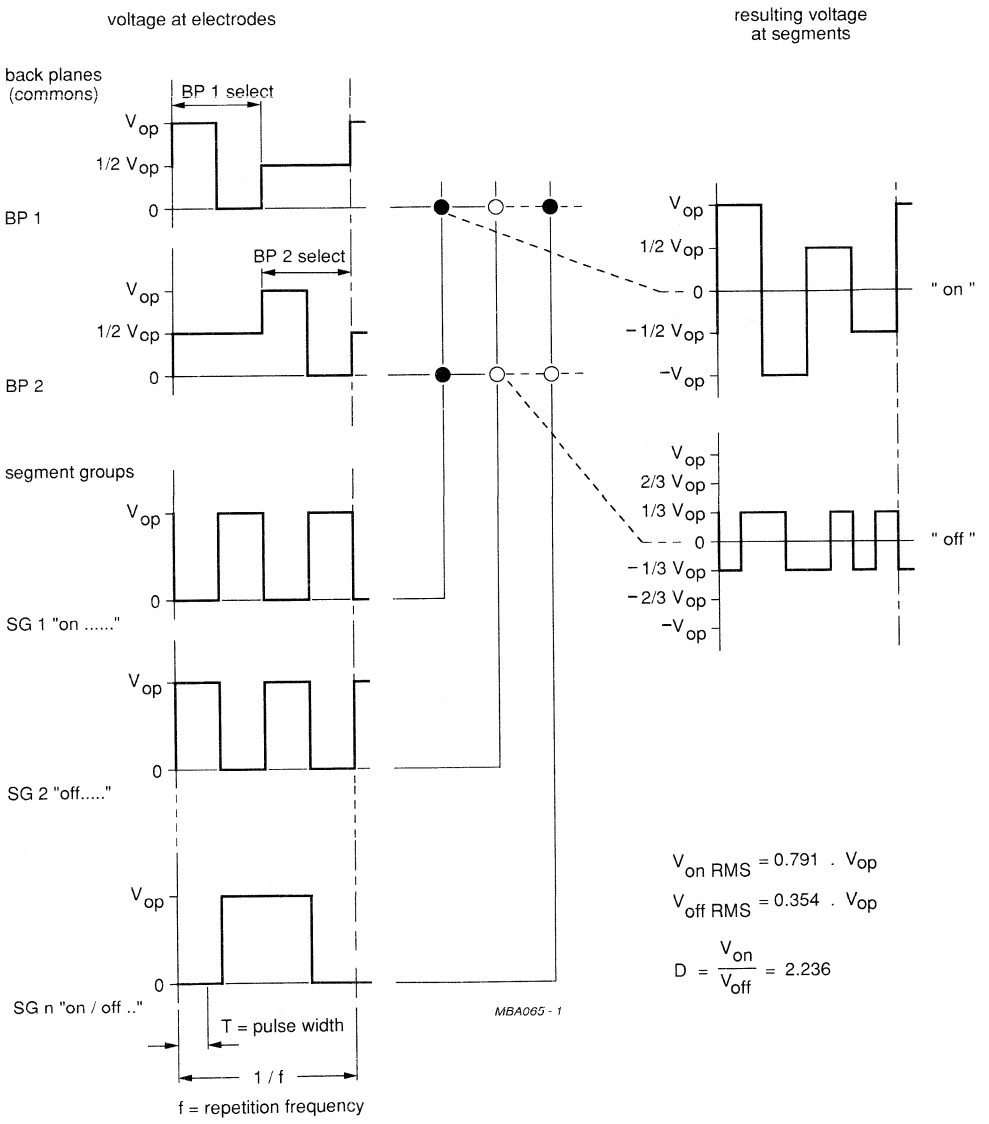


Fig.31 (b) Typical waveforms of V_{op} for MUX 1:2.

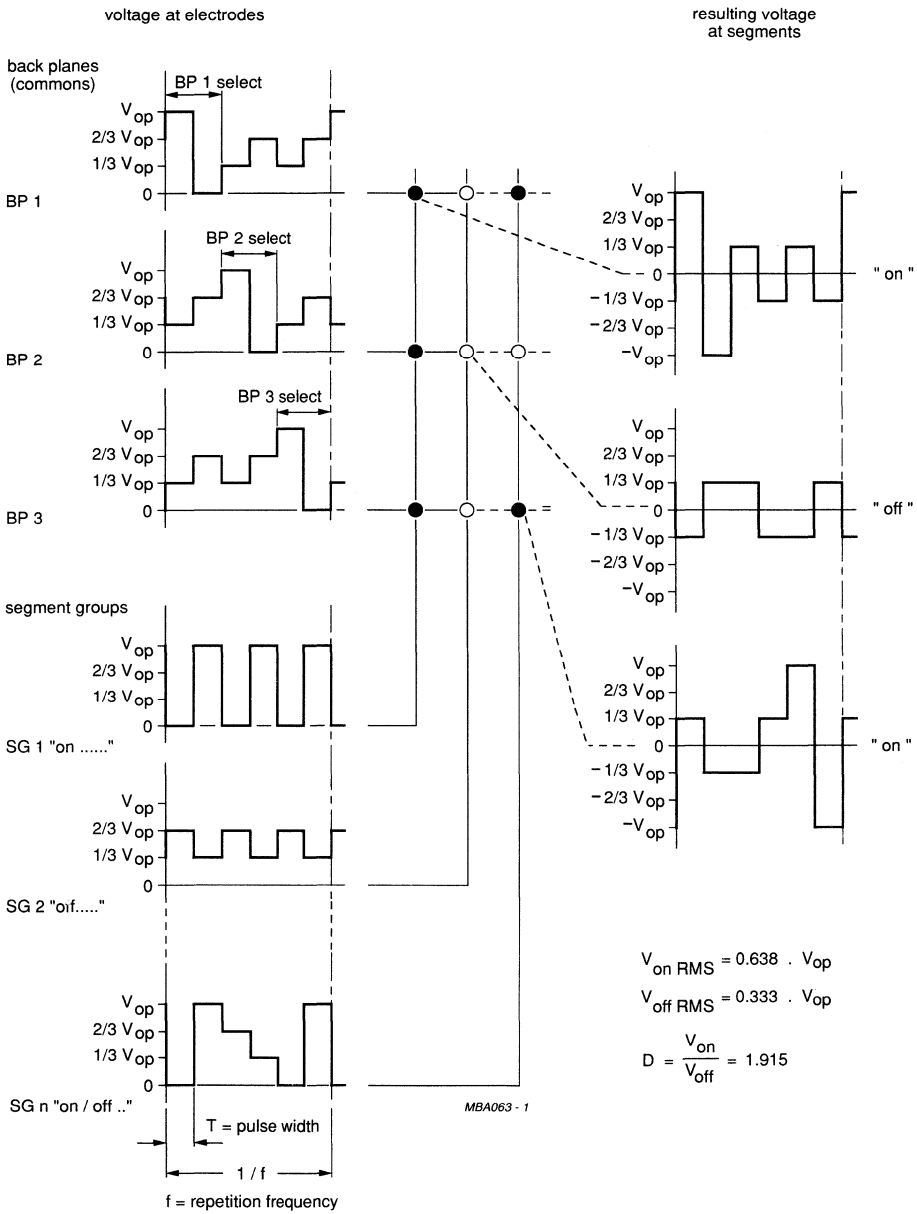


Fig.31 (c) Typical waveforms of V_{op} for MUX 1:3.

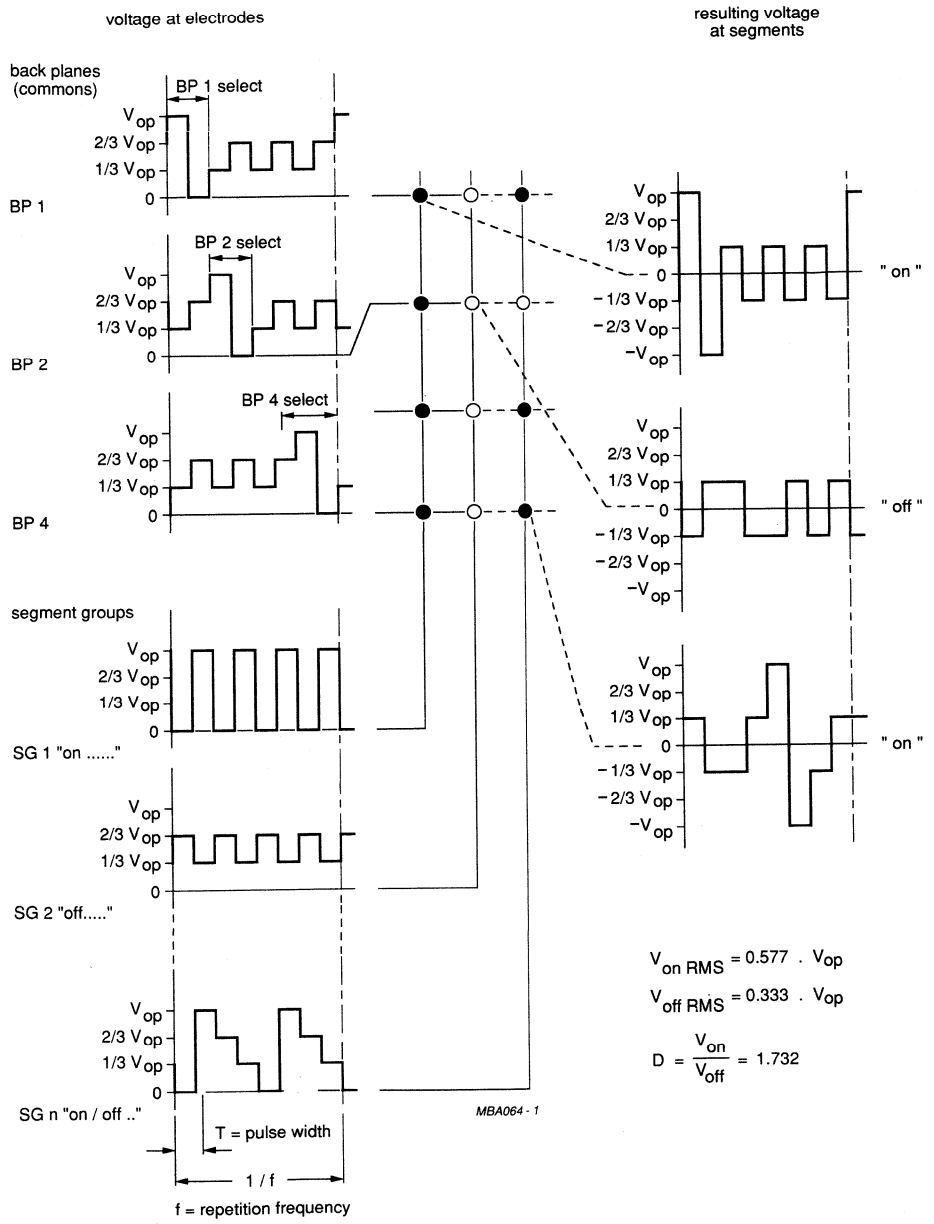
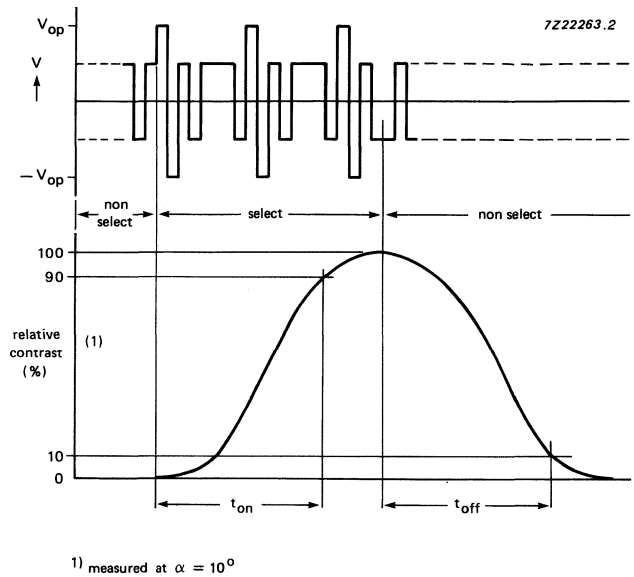


Fig.31 (d) Typical waveforms of V_{op} for MUX 1:4.



1) measured at $\alpha = 10^{o}$

Fig.32 Definition of response times.

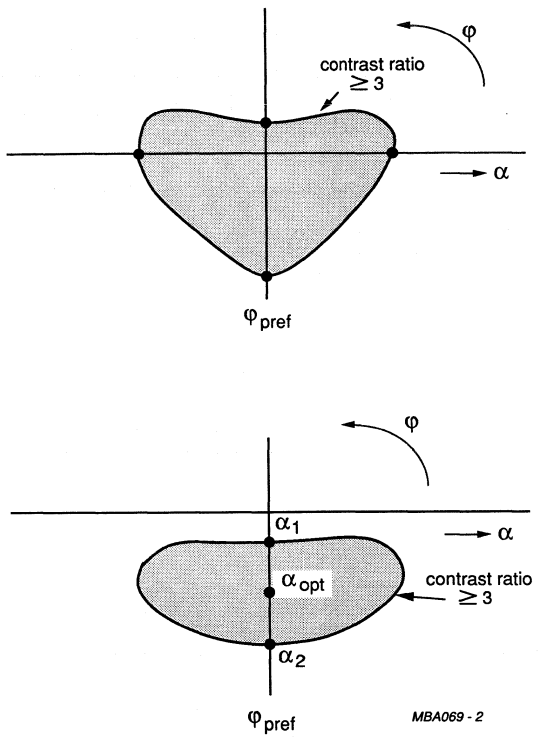
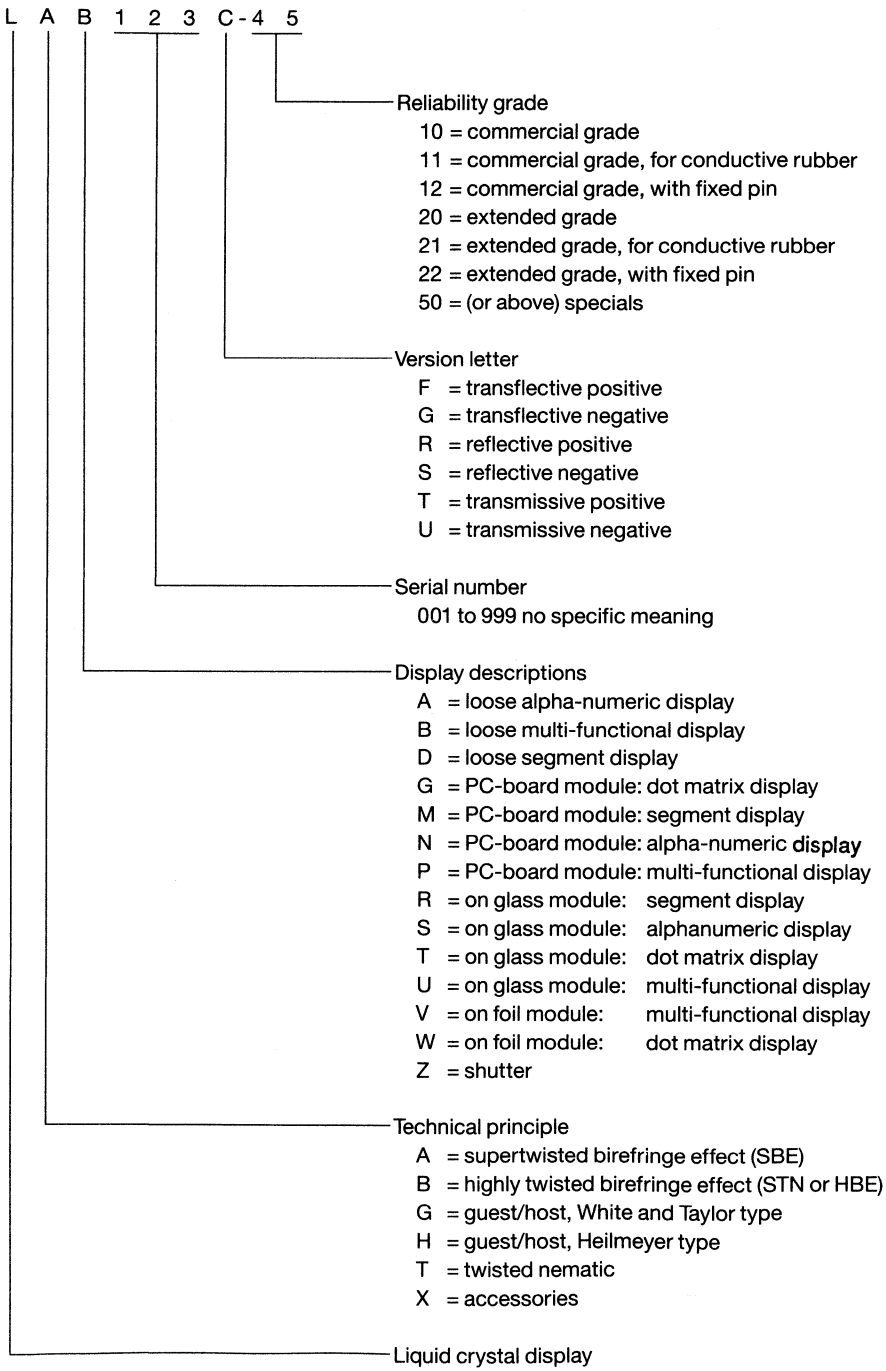


Fig.33 Definition of viewing angles α and ϕ.

Liquid crystal display — Type number designations



LCD cells

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LHA142
Liquid crystal display

DEVICE DESCRIPTION

The LHA142 is a single character display in Heilmeyer Guest-Host technology. Typical applications include information panels for air terminals, bus stations and railway stations.

QUICK REFERENCE DATA

Viewing area dimensions	44.8 x 66.4 mm
Overall glass dimensions	50.8 x 80.0 mm
Thickness	2.7 +/– 0.2 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive

DISPLAY MODE

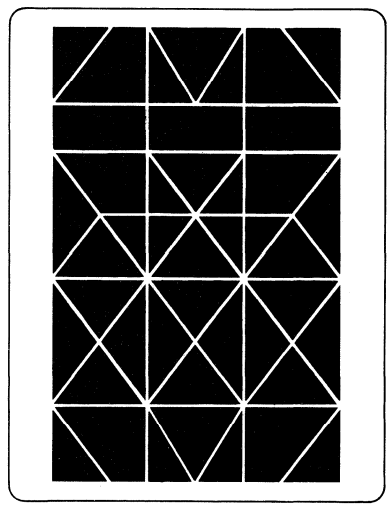


Fig.1 1-character display.

TYPE DEPENDENT CHARACTERISTICS

TYPE	ILLUMINATION MODE	IMAGE MODE	CONNECTION METHOD	RELIABILITY GRADE	OPERATING VOLTAGE (V)
LHA142U–22	transmissive	negative	with fixed pins	extended	7.5 to 9.5

MECHANICAL DATA

Dimensions in mm

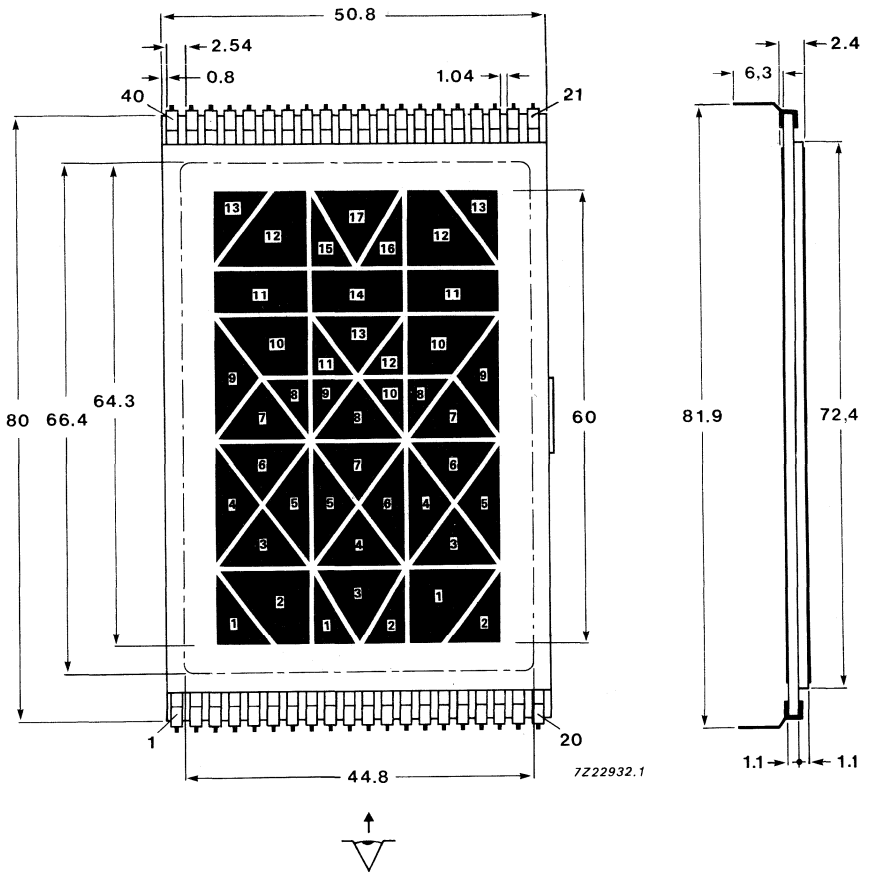


Fig.2 Display dimensions.

Liquid crystal display

LHA142

PIN DESCRIPTION

PIN NO.	SEGMENT
1	comm
2	b8
3	a4
4	a6
5	a5
6	a1
7	a2,a3
8	b5
9	b3
10	b1,b2
11	b4
12	b7
13	b6
14	c1
15	c2
16	c3
17	c4
18	c6
19	c5
20	c7

PIN NO.	SEGMENT
21	b10
22	c8
23	c9
24	c10
25	b12
26	c11
27	b15,b16
28	c12
29	c13
30	b17
31	a13
32	a12
33	a11
34	b13,b14
35	b11
36	a10
37	a9
38	a8
39	a7
40	b9

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two contacts (see note)	V_{max}	15 V RMS
Storage temperature range	T_{stg}	−40 to +85 °C

Note: maximum DC component = 0.1 V

OPERATING CHARACTERISTICS

All values at, T_{amb} = 25 °C; $V_{op} = V_{op\ typ}$; f_{dr} = 100 Hz; α = 10°; $\phi = \phi_{opt}$, unless otherwise specified

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
operating operating voltage	V_{op}	7.5	8.5	9.5	V
operating ambient temperature range	T_{amb}	−25	-	+80	°C
turn on time at T_{amb} = 25 °C at T_{amb} = 0 °C	t_{on} t_{on}	- -	60 260	120 520	ms ms
turn off time at T_{amb} = 25 °C at T_{amb} = 0 °C	t_{off} t_{off}	- -	35 125	70 250	ms ms
specific current consumption*	I	-	62	124	µA
frame frequency	f_{dr}	30	-	200	Hz

* All segments on.

APPLICATION INFORMATION

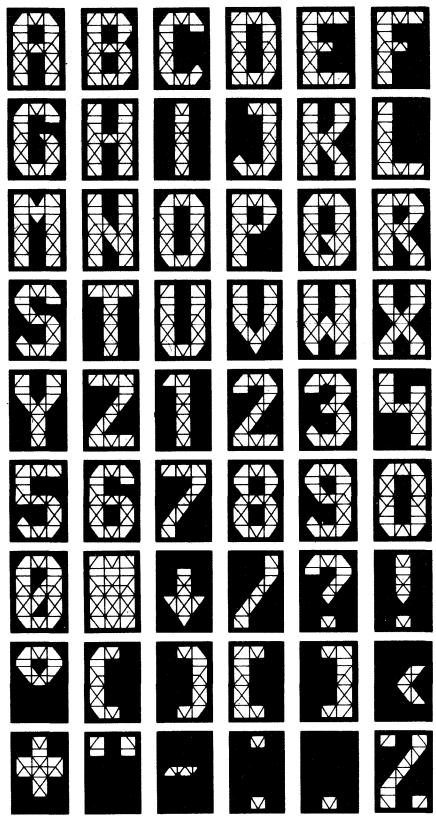


Fig.3 Examples of symbols that can be displayed by the LHA142. Other symbols are possible by selection of appropriate pin numbers.

	PIN NUMBERS																		
	1*	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A		X	X	X	X	X	X							X	X	X	X	X	X	X
B		X	X	X	X	X	X		X	X				X		X	X	X	X	X
C			X	X	X		X		X	X				X		X				
D			X	X	X	X	X		X	X				X		X	X	X	X	X
E		X	X	X	X	X	X		X	X				X	X					
F		X	X	X	X	X	X													
G			X	X	X		X		X	X				X		X	X	X	X	X
H		X	X	X	X	X	X							X	X	X	X	X	X	X
I		X						X	X	X	X	X	X							
J							X		X	X				X		X	X	X	X	X
K		X	X	X	X	X	X					X	X	X	X	X	X			
L			X	X	X	X	X		X	X				X	X					
M			X	X	X	X	X							X	X	X	X	X	X	X
N		X	X	X	X	X	X					X	X	X	X	X	X	X	X	X
O			X	X	X		X		X	X				X		X	X	X	X	X
P		X	X	X	X	X	X													
Q			X	X	X		X		X	X		X	X	X	X	X	X	X	X	X
R		X	X	X	X	X	X					X	X	X	X	X	X			
S		X					X		X	X				X		X	X	X	X	X
T		X						X	X	X	X	X	X							
U			X	X	X		X		X	X				X		X	X	X	X	X
V				X	X			X	X		X		X				X	X		X
W		X	X	X	X		X	X				X	X	X		X	X	X	X	X
X		X			X	X	X	X				X	X	X	X	X	X			
Y		X						X	X	X	X	X	X							
Z		X			X	X	X	X	X	X		X		X	X					
?		X							X	X		X								
!		X							X	X		X								
+		X						X			X	X	X							X
-		X																		X
:								X			X	X	X							X
.									X	X	X									
/		X			X	X	X	X				X								
\		X										X	X	X	X	X	X			
{			X	X	X		X		X	X										
}									X	X				X		X	X	X	X	X
[			X	X	X	X	X		X	X										
]									X	X				X	X	X	X	X	X	X
■		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
↓		X		X	X			X	X		X	X	X				X	X		
1		X						X	X	X	X	X	X							
2		X			X	X	X	X	X	X		X		X	X					
3		X					X		X	X				X		X	X	X	X	X
4		X												X	X	X	X	X	X	X
5		X					X		X	X				X		X	X	X	X	X
6		X	X	X	X		X		X	X				X		X	X	X	X	X
7		X			X	X	X	X				X								
8		X	X	X	X		X		X	X				X		X	X	X	X	X
9		X					X		X	X				X		X	X	X	X	X
0		X	X	X	X		X	X	X	X		X		X		X	X	X	X	X
°																				
%		X			X	X	X	X				X		X	X					

* Pin 1 = common; X = ON: blank = OFF

	PIN NUMBERS (cont.)																			
	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
A	X	X	X	X		X	X	X		X		X	X			X	X	X	X	X
B	X	X		X	X	X	X	X		X		X	X			X	X	X	X	X
C						X	X	X		X		X	X			X	X	X	X	
D		X	X	X		X	X	X		X	X	X	X			X	X	X	X	
E	X						X	X	X	X	X	X	X			X	X	X	X	X
F	X						X	X	X	X	X	X	X			X	X	X	X	X
G	X	X					X	X		X		X	X			X	X	X	X	
H	X	X	X	X		X		X	X		X	X	X			X	X	X	X	X
I	X				X		X			X				X	X					X
J		X	X	X		X	X	X	X	X										
K	X	X		X	X	X		X	X		X	X	X			X	X	X	X	X
L											X	X	X			X	X	X	X	
M		X	X	X		X	X	X	X		X	X	X	X		X	X	X	X	
N		X	X	X		X		X	X		X	X	X		X	X	X	X	X	X
O		X	X	X		X	X	X		X		X	X			X	X	X	X	
P	X	X		X	X	X	X	X		X	X	X	X			X	X	X	X	
Q		X	X	X		X	X	X		X		X	X			X	X	X	X	
R	X	X		X	X	X	X	X		X	X	X	X			X	X	X	X	X
S	X	X				X	X	X		X		X	X		X	X		X		X
T	X				X		X	X	X	X	X	X		X	X					X
U		X	X	X		X		X	X		X	X	X			X	X	X	X	
V		X	X	X		X		X	X		X	X	X			X	X	X	X	
W		X	X	X		X		X	X		X	X	X			X	X	X	X	
X	X	X		X	X	X		X	X		X	X	X		X	X		X		X
Y	X	X		X	X	X		X	X		X	X	X		X	X		X		X
Z	X	X		X	X	X	X	X	X	X	X	X								
?	X	X		X	X	X	X	X	X		X	X	X							
!	X				X		X			X				X	X					X
+	X	X	X	X	X			X		X				X	X	X	X	X	X	X
-	X	X	X	X	X									X	X	X	X	X	X	X
:					X									X	X					
.																				
/	X	X		X	X	X		X	X											
\											X	X	X		X	X		X		X
{							X			X		X	X			X	X	X	X	
}		X	X	X		X	X	X		X										
[							X			X	X	X	X			X	X	X	X	
]		X	X	X		X	X	X	X	X										
■	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
↓	X				X									X	X					X
1	X				X		X			X		X		X	X					X
2	X	X		X	X	X	X	X		X		X	X							
3	X	X		X	X	X	X	X		X		X	X							X
4	X	X	X	X		X					X	X	X			X	X	X	X	X
5	X	X					X	X	X	X	X	X	X			X	X	X	X	X
6	X	X				X	X	X		X		X	X			X	X	X	X	X
7	X	X		X	X	X	X	X	X	X	X	X								
8	X	X		X	X	X	X	X		X		X	X			X		X	X	X
9	X	X		X		X	X	X		X		X	X		X	X		X		X
0	X	X		X		X	X	X		X		X	X			X	X	X	X	
o				X	X	X	X	X		X		X	X	X	X	X				
%	X	X		X	X	X		X	X		X	X								

* Pin 1 = common; X = ON: blank = OFF

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTA141

Liquid Crystal Display

DEVICE DESCRIPTION

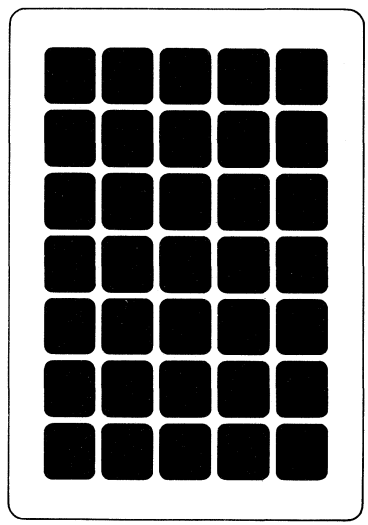
The LTA141 is a single character display of 5 x 7 dots. Typical applications include communications panels for air terminals, bus stations and railway stations.

QUICK REFERENCE DATA

Viewing area dimensions	45.8 x 67.4 mm
Overall glass dimensions	50.8 x 80.0 mm
Thickness	2.7 +/– 0.4 mm
Digit height	37.2 x 57.3 mm
Preferred viewing direction	12 o'clock
Driving method	direct drive

DISPLAY MODE

scale 1:1



7Z22323

Fig.1 Universal display.

MECHANICAL DATA

Dimensions in mm

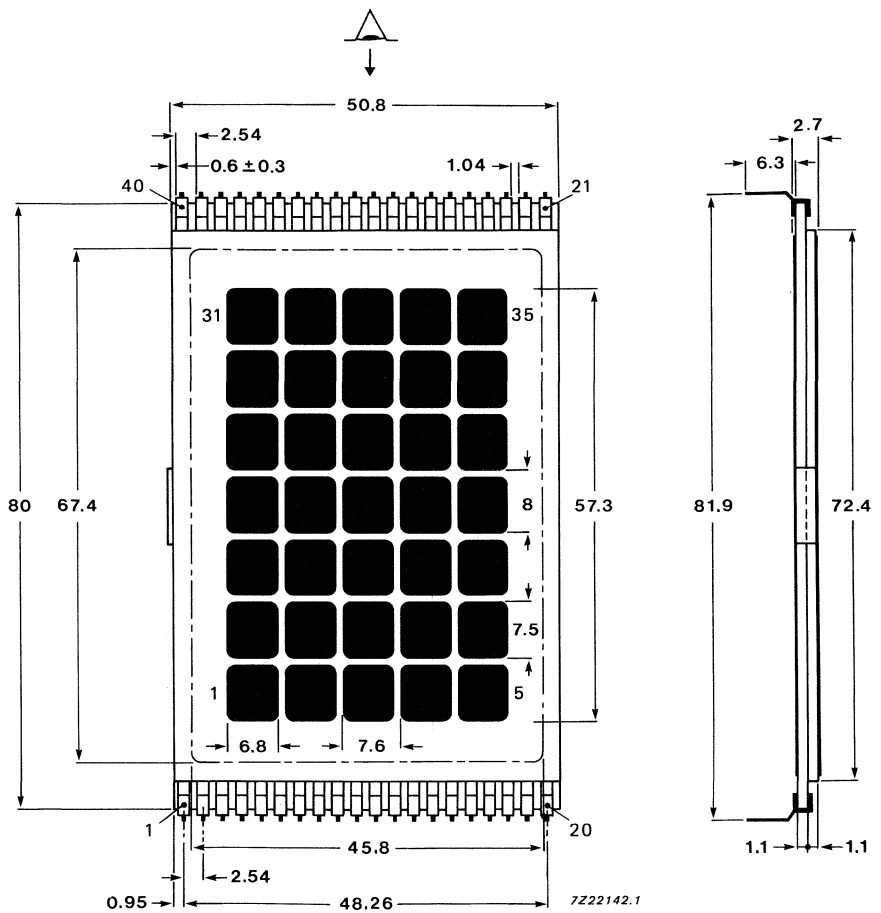


Fig.2 Display dimensions.

Liquid crystal display LTA141

PIN DESCRIPTION

PIN NO.	SEGMENT	PIN NO.	SEGMENT
1	comm	21	16
2	n.c.	22	25
3	n.c.	23	26
4	n.c.	24	35
5	1	25	24
6	10	26	27
7	12	27	34
8	2	28	23
9	9	29	28
10	8	30	33
11	3	31	18
12	13	32	19
13	7	33	32
14	4	34	29
15	14	35	22
16	17	36	31
17	5	37	30
18	6	38	21
19	15	39	20
20	n.c.	40	11

TYPE DEPENDENT CHARACTERISTICS (1)

TYPE	ILLUMINATION MODE	CONNECTION METHOD	QUALITY GRADE	FAMILY CHARACTERISTICS (2)	OPERATING VOLTAGE (V)
LTA141R–12	reflective	with fixed pins	commercial	TR0	3.5 – 6.5
LTA141F–12	transflective	with fixed pins	commercial	TF0	3.5 – 6.5
LTA141R–22	reflective	with fixed pins	extended	TR2	3.5 – 6.5
LTA141F–22	transflective	with fixed pins	extended	TF2	3.5 – 6.5

Note: (1) drive method = direct drive for all types
(2) see chapter "Family Characteristics" for complete specfication

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two contacts (see note) V_{max} 15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	Low temperature storage T_{amb}/duration	High temperature storage T_{amb}/duration (dry)
LTA141R–12	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days
LTA141F–12	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days
LTA141R–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days
LTA141F–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTA331
Liquid Crystal Display

DEVICE DESCRIPTION

The LTA331 is a 16-character, 1-line dot matrix display. Typical applications include hand held equipment and industrial applications. The display can be inverted to adapt the optimal viewing direction to the application. The symmetrical pinout allows the use of only one PC-board.

QUICK REFERENCE DATA

Viewing area dimensions	65 x 14.4 mm
Overall glass dimensions	69 x 23 mm
Character format	5 x 7 dots and cursor
Character size	6.56 x 3.07 mm
Dot size (spacing 0.08 mm)	0.83 x 0.55 mm
Drive method	MUX 1:16
Operating voltage	5 V
Illumination mode	reflective/ transflective
Preferred viewing direction	6 o'clock

DISPLAY MODE

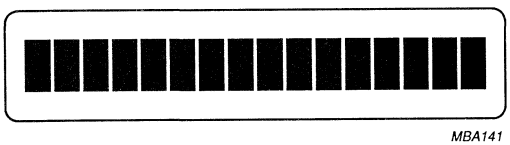


Fig.1 1-line, 16-character, dot matrix display.

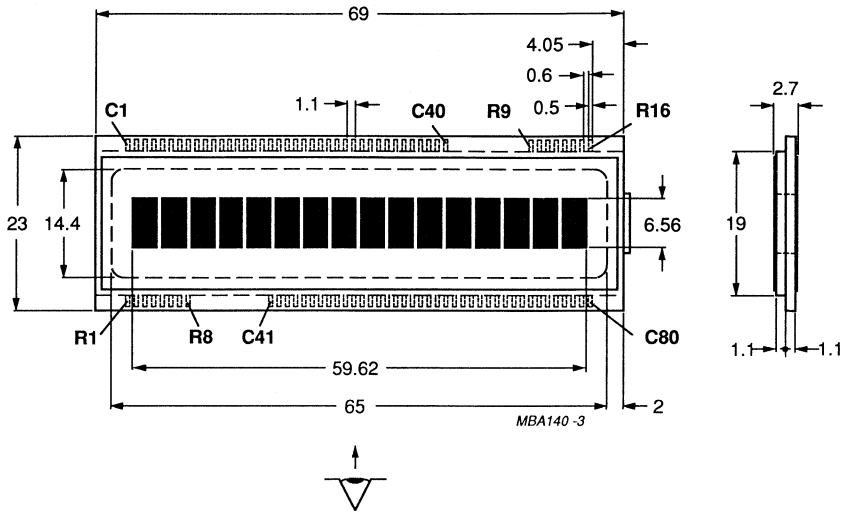
TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	OPERATING AMBIENT TEMPERATURE RANGE	RELIABILITY GRADE
LTA331R-11	reflective	for conductive rubber	−10 to +60 °C	commercial
LTA331F-11	transflective	for conductive rubber	−10 to +60 °C	commercial

Liquid Crystal Display LTA331

MECHANICAL DATA

Dimensions in mm



PIN DESCRIPTION

R = row
C = column

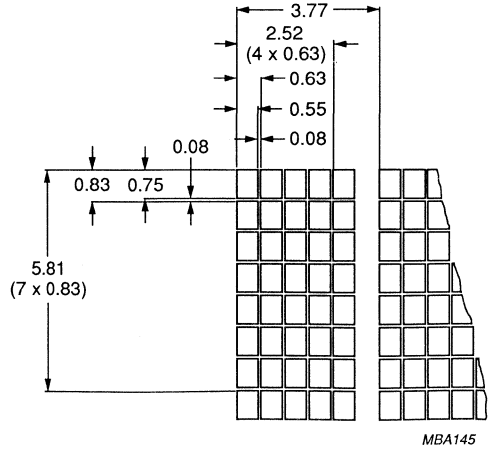


Fig.2 Display area dimensions.

Liquid Crystal Display LTA331

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections (see note)	V_{max}	10 V RMS
Storage temperature range	T_{stg}	−25 to +70 °C

Note: maximum DC component = 0.1 V

OPERATING CONDITIONS

All values at, T_{amb} = 25 °C; $V_{op} = V_{op\ typ}$; f_{dr} = 100 Hz, unless otherwise specified

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
operating voltage	V_{op}	-	5	-	V
temperature compensation of V_{op}	TC	-	−20	-	mV/°C
operating ambient temperature	T_{amb}	−10	-	+60	°C
current consumption (see note)	I	-	52	110	µA
frame frequency	f_{dr}	30	-	100	Hz

Note: with all dots "ON".

ELECTRO-OPTICAL CHARACTERISTICS

T_{amb} = 25 °C, $V_{op} = V_{op\ typ}$, α = 10°, $\phi = \phi_{opt}$, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	TYP.	MAX.	UNIT
Response times	t_{on}	T_{amb} = 0 °C T_{amb} = 25 °C T_{amb} = 50 °C	380 110 45	760 220 90	ms ms ms
	t_{off}	T_{amb} = 0 °C T_{amb} = 25 °C T_{amb} = 50 °C	470 110 45	940 220 90	ms ms ms
Viewing Angles (contrast ratio CR > 3)	α_{opt} α_2-α_1	reflective types	30 30	- -	o o
	α_{opt} α_2-α_1	transflective types reflective operation	30 25	- -	o o
	α_{opt} α_2-α_1	transflective types transmissive operation	30 20	- -	o o

For definitions of contrast ratio, viewing angles and response times see notes 1 to 3.

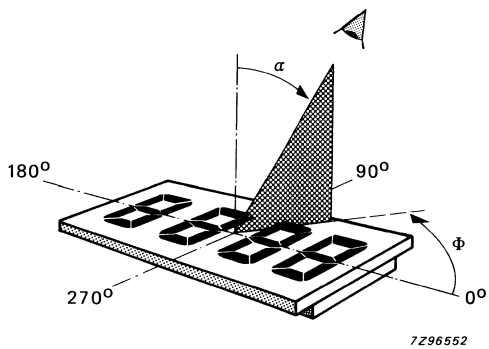
Note 1 Definition of contrast ratio (C_R).

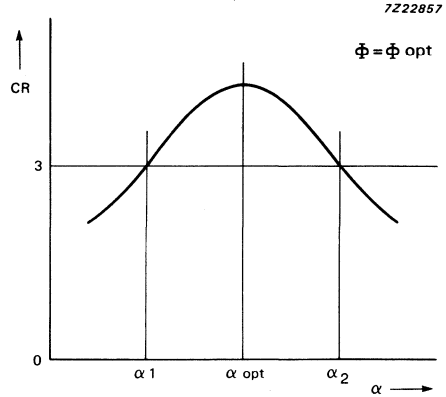
$$\text{in positive image mode: } CR = \frac{B_{off}}{B_{on}}$$

$$\text{in negative image mode: } CR = \frac{B_{on}}{B_{off}}$$

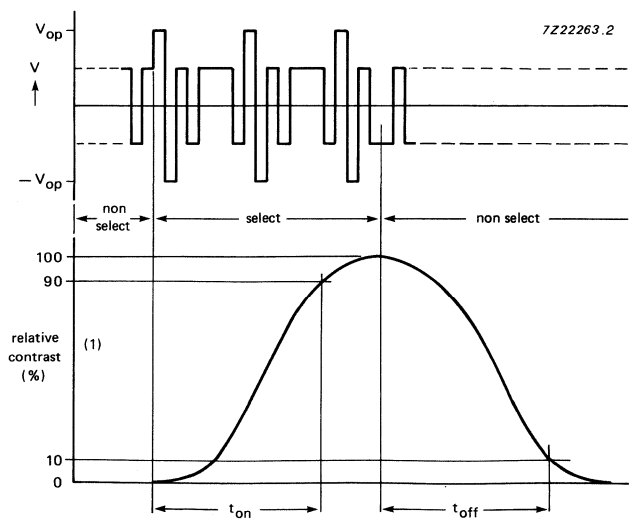
B_{on} is the brightness of selected segments
B_{off} is the brightness of non-selected segments

Note 2 Definition of viewing angles α and ϕ.



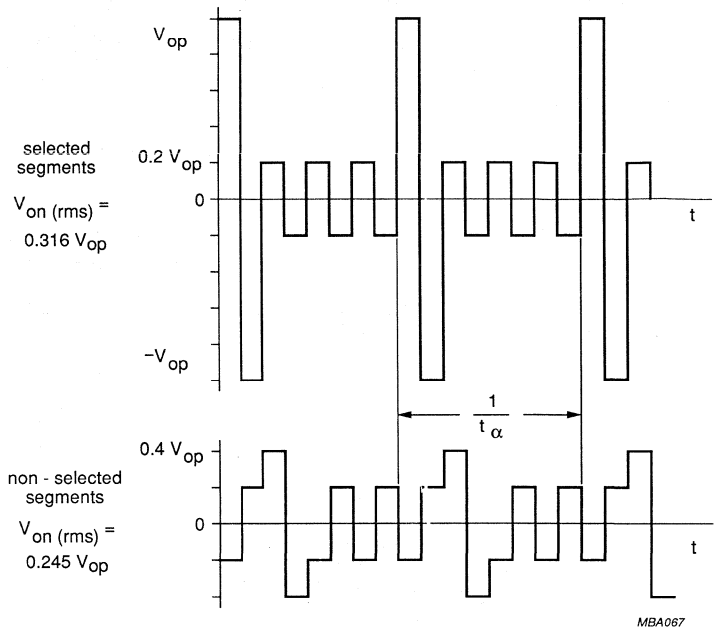


Note 3 Definition of response times.



1) measured at $\alpha = 10^o$

Note 4 Definition of waveforms.



Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTA332
Liquid Crystal Display

DEVICE DESCRIPTION

The LTA332 is a 16-character, 2-line dot matrix display. Typical applications include hand held equipment and industrial applications. The display can be inverted to adapt the optimal viewing direction to the application. The symmetrical pinout allows the use of only one PC-Board.

QUICK REFERENCE DATA

Viewing area dimensions	63 x 16.4 mm
Overall glass dimensions	69 x 24.7 mm
Character format	5 x 7 dots and cursor
Character size	5.56 x 2.96 mm
Dot size (spacing 0.06 mm)	0.66 x 0.56 mm
Drive method	MUX 1:16
Operating voltage	5 V
Illumination mode	reflective/trans-flective
Preferred viewing direction	6 o'clock

DISPLAY MODE

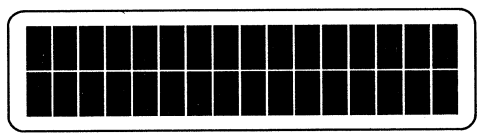
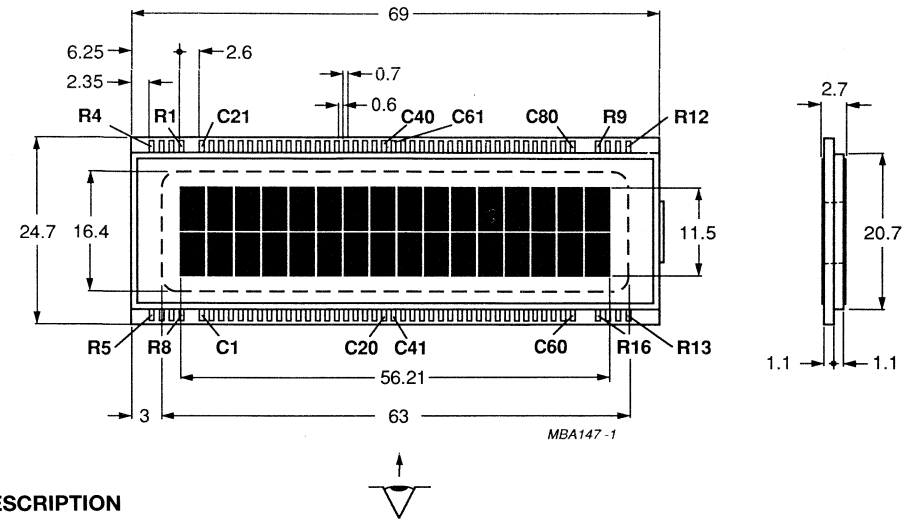


Fig.1 2-line, 16-character, dot matrix display.

TYPE DEPENDENT DATA

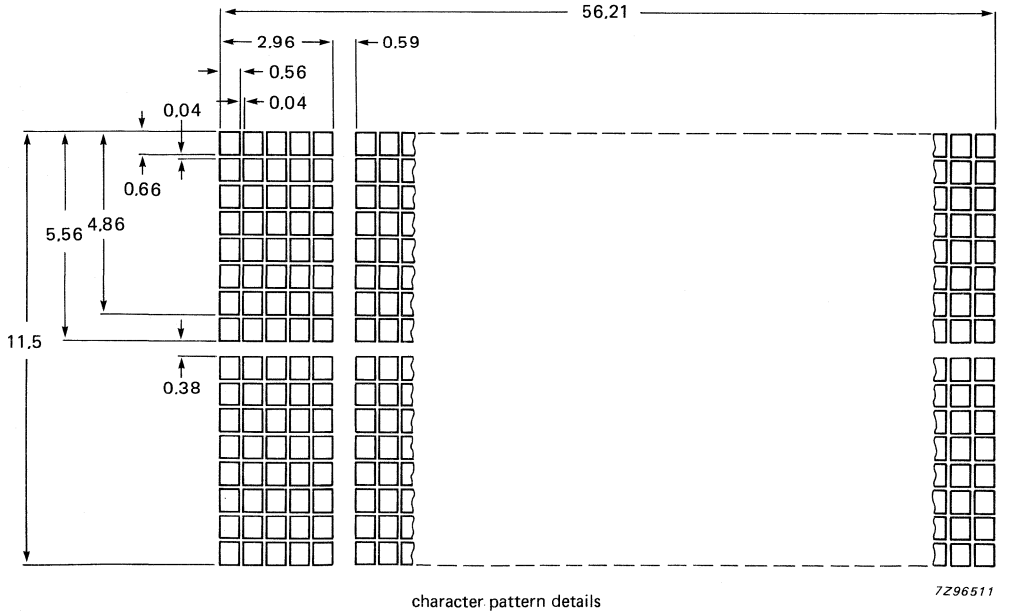
TYPE	ILLUMINATION MODE	CONNECTION METHOD	OPERATING AMBIENT TEMPERATURE RANGE	RELIABILITY GRADE
LTA332R–11	reflective	for conductive rubber	–10 to +60 °C	commercial
LTA332F–11	transflective	for conductive rubber	–10 to +60 °C	commercial

MECHANICAL DATA



PIN DESCRIPTION

R = row
C = column



character pattern details

Fig.2 Display area dimensions.

Liquid Crystal Display LTA332

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections (see note)	V_{max}	10 V RMS
Storage temperature range	T_{stg}	–25 to +70 °C

Note: maximum DC component = 0.1 V

OPERATING CONDITIONS

All values at, T_{amb} = 25 °C; $V_{op} = V_{op\ typ}$; f_{dr} = 100 Hz, unless otherwise specified.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
operating voltage	V_{op}	-	5	-	V
temperature compensation of V_{op}	TC	-	–20	-	mV/°C
operating ambient temperature	T_{amb}	–10	-	+60	°C
current consumption (see note)	I	-	92	184	µA
frame frequency	f_{dr}	30	-	100	Hz

Note: with all dots "ON".

ELECTRO-OPTICAL CHARACTERISTICS

T_{amb} = 25 °C, $V_{op} = V_{op\ typ}$, α = 10°, $\phi = \phi_{opt}$, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	TYP.	MAX.	UNIT
Response times	t_{on}	T_{amb} = 0 °C T_{amb} = 25 °C T_{amb} = 0 °C	380 110 45	760 220 90	ms ms ms
	t_{off}	T_{amb} = 0 °C T_{amb} = 25 °C T_{amb} = 50 °C	470 110 45	940 220 90	ms ms ms
Viewing Angles (contrast ratio CR > 3)	α_{opt} α_2-α_1	reflective types	30 30	- -	° °
	α_{opt} α_2-α_1	transflective types reflective operation	30 25	- -	° °
	α_{opt} α_2-α_1	transflective types transmissive operation	30 20	- -	° °

For definitions of contrast ratio, viewing angles and response times see notes 1 to 3.

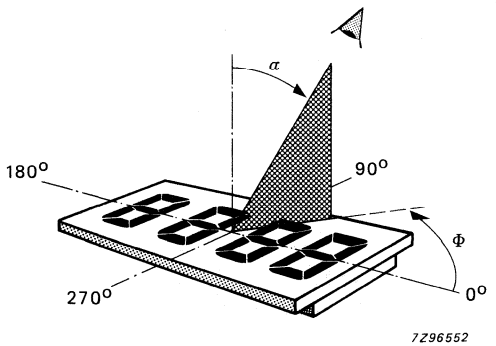
Note 1 Definition of contrast ratio (C_R).

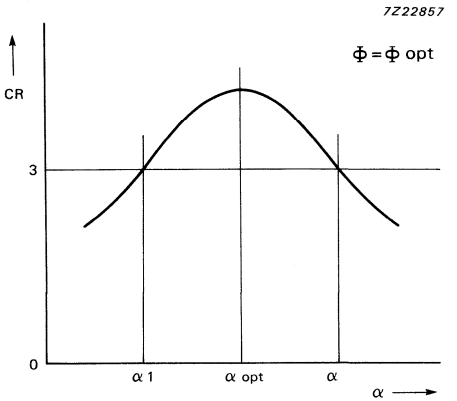
in positive image mode: $CR = \frac{B_{off}}{B_{on}}$

in negative image mode: $CR = \frac{B_{on}}{B_{off}}$

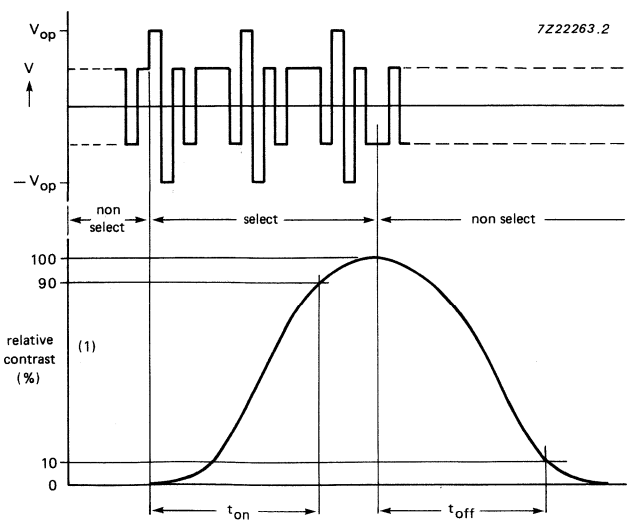
B_{on} is the brightness of selected segments
B_{off} is the brightness of non-selected segments

Note 2 Definition of viewing angles α and ϕ.



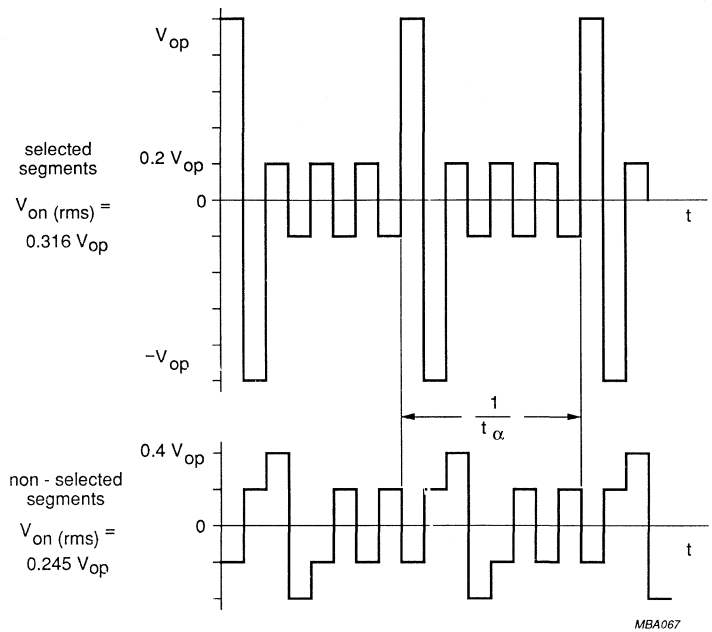


Note 3 Definition of response times.



1) measured at $\alpha = 10°$

Note 4 Definition of waveforms.



Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTA341

Liquid Crystal Display

DEVICE DESCRIPTION

The LTA341 is a 20-character, 2-line dot matrix display. Typical applications include hand held equipment and industrial applications. The display can be inverted to adapt the optimal viewing direction to the application.

QUICK REFERENCE DATA

Viewing area dimensions	83 x 18.6 mm
Overall glass dimensions	93.6 x 34.6 mm
Character format	5 x 7 dots and cursor
Character size	5.55 x 3.2 mm
Dot size (spacing 0.06 mm)	0.65 x 0.65 mm
Drive method	MUX 1:16
Operating voltage	5 V
Illumination mode	reflective/trans-flective
Preferred viewing direction	6 o'clock

DISPLAY MODE

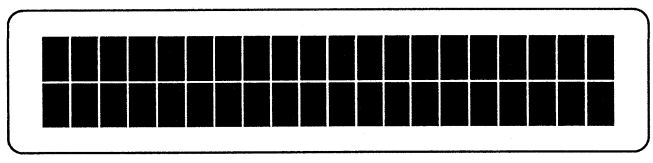
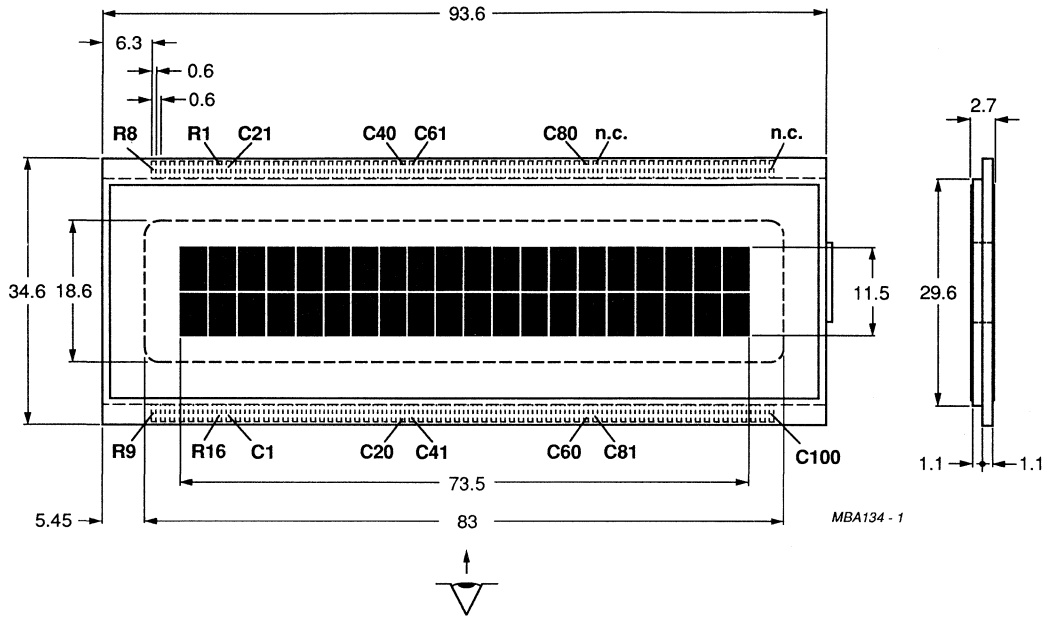


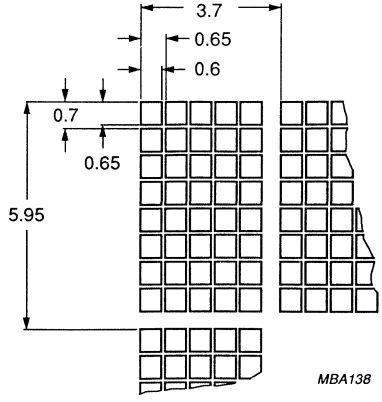
Fig.1 2-line, 20-character, dot matrix display.

TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	OPERATING AMBIENT TEMPERATURE RANGE	RELIABILITY GRADE
LTA341R–11	reflective	for conductive rubber	–10 to +60 °C	commercial
LTA341F–11	transflective	for conductive rubber	–10 to +60 °C	commercial

MECHANICAL DATA





PIN DESCRIPTION

R = row
C = column

Fig.2 Display area dimensions.

Liquid Crystal Display LTA341

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections (see note)	V_{max}	10 V RMS
Storage temperature range	T_{stg}	–25 to +70 °C

Note: maximum DC component = 0.1 V

OPERATING CONDITIONS

All values at, T_{amb} = 25 °C; $V_{op} = V_{op\ typ}$; f_{dr} = 100 Hz, unless otherwise specified.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
operating voltage	V_{op}	-	5	-	V
temperature compensation of V_{op}	TC	-	–13	-	mV/°C
operating ambient temperature	T_{amb}	–10	-	+60	°C
current consumption (see note)	I	-	175	350	µA
frame frequency	f_{dr}	30	-	100	Hz

Note: with all dots "ON".

ELECTRO-OPTICAL CHARACTERISTICS

T_{amb} = 25 °C, $V_{op} = V_{op\ typ}$, α = 10°, $\phi = \phi_{opt}$, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	TYP.	MAX.	UNIT
Response times	t_{on}	T_{amb} = 0 °C T_{amb} = 25 °C T_{amb} = 50 °C	380 110 45	760 220 90	ms ms ms
	t_{off}	T_{amb} = 0 °C T_{amb} = 25 °C T_{amb} = 50 °C	470 110 45	940 220 90	ms ms ms
Viewing Angles (contrast ratio CR > 3)	α_{opt} α_2-α_1	reflective types	30 25	- -	° °
	α_{opt} α_2-α_1	transflective types reflective operation	30 25	- -	° °
	α_{opt} α_2-α_1	transflective types transmissive operation	30 20	- -	° °

For definitions of contrast ratio, viewing angles and response times see notes 1 to 3.

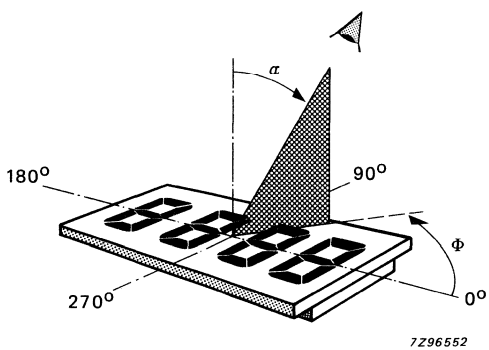
Note 1 Definition of contrast ratio (C_R).

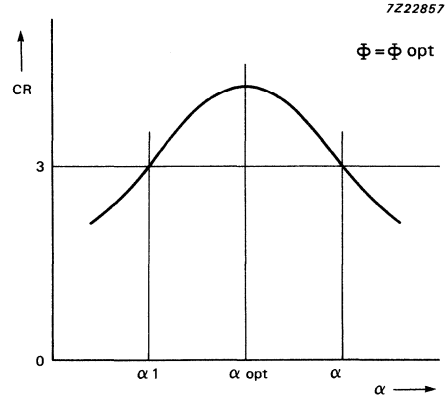
$$\text{in positive image mode: } CR = \frac{B_{off}}{B_{on}}$$

$$\text{in negative image mode: } CR = \frac{B_{on}}{B_{off}}$$

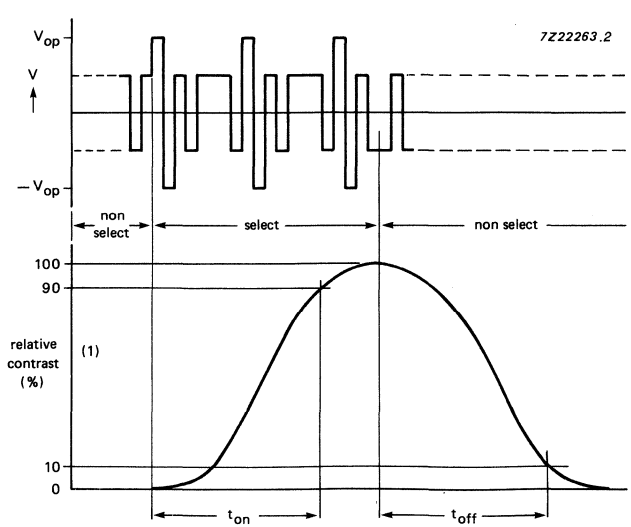
B_{on} is the brightness of selected segments
B_{off} is the brightness of non-selected segments

Note 2 Definition of viewing angles α and ϕ.



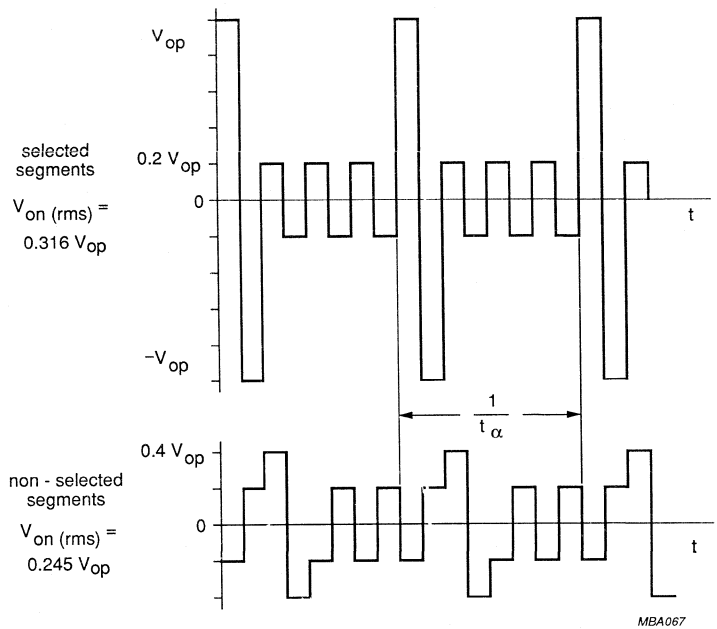


Note 3 Definition of response times.



1) measured at $\alpha = 10°$

Note 4 Definition of waveforms.



Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTA342
Liquid Crystal Display

DEVICE DESCRIPTION

The LTA342 is a 24-character, 2-line dot matrix display. Typical applications include hand held equipment and industrial applications. The display may be inverted to adapt the optimal viewing direction to the application.

QUICK REFERENCE DATA

Viewing area dimensions	83 x 18.6 mm
Overall glass dimensions	93.6 x 34.6 mm
Character format	5 x 7 dots and cursor
Character size	5.55 x 2.95 mm
Dot size (spacing 0.05 mm)	0.65 x 0.65 mm
Drive method	MUX 1:16
Operating voltage	5 V
Illumination mode	reflective/trans-flective
Preferred viewing direction	6 o'clock

DISPLAY MODE

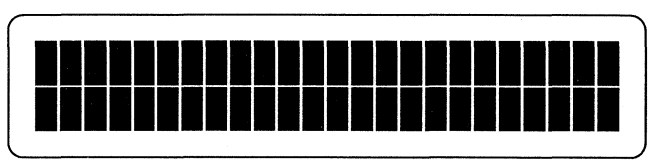


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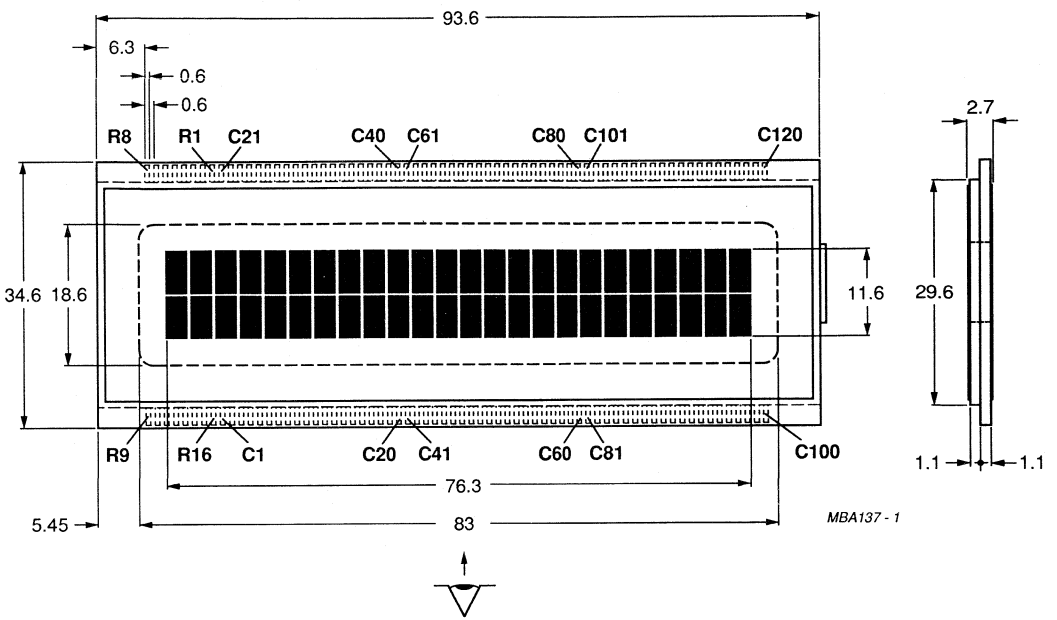
Fig.1 2-line, 24-character, dot matrix display.

TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	OPERATING AMBIENT TEMPERATURE RANGE	RELIABILITY GRADE
LTA342R–11	reflective	for conductive rubber	–10 to +60 °C	commercial
LTA342F–11	transflective	for conductive rubber	–10 to +60 °C	commercial

Liquid Crystal Display LTA342

MECHANICAL DATA



PIN DESCRIPTION

R = row
C = column

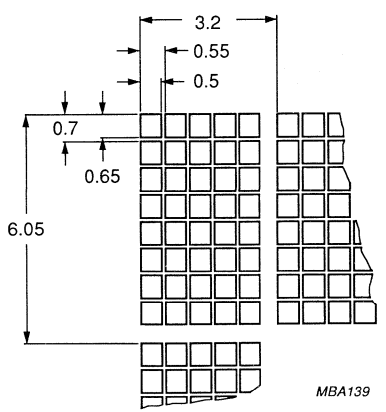


Fig.2 Display area dimensions.

Liquid Crystal Display LTA342

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections (see note)	V_{max}	10 V RMS
Storage temperature range	T_{stg}	–25 to +70 °C

Note: maximum DC component = 0.1 V

OPERATING CONDITIONS

All values at, T_{amb} = 25 °C; $V_{op} = V_{op\ typ}$; f_{dr} = 100 Hz, unless otherwise specified

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
operating voltage	V_{op}	-	5	-	V
temperature compensation of V_{op}	TC	-	–13	-	mV/°C
operating ambient temperature	T_{amb}	–10	-	+60	°C
current consumption (see note)	I	-	175	350	µA
frame frequency	f_{dr}	30	-	100	Hz

Note: with all dots "ON".

ELECTRO-OPTICAL CHARACTERISTICS

T_{amb} = 25 °C, $V_{op} = V_{op\ typ}$, α = 10°, $\phi = \phi_{opt}$, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	TYP.	MAX.	UNIT
Response times	t_{on}	T_{amb} = 0 °C T_{amb} = 25 °C T_{amb} = 50 °C	380 110 45	760 220 90	ms ms ms
	t_{off}	T_{amb} = 0 °C T_{amb} = 25 °C T_{amb} = 50 °C	470 110 45	940 220 90	ms ms ms
Viewing Angles (contrast ratio CR > 3)	α_{opt} α_2-α_1	reflective types	30 30	- -	° °
	α_{opt} α_2-α_1	transflective types reflective operation	30 25	- -	° °
	α_{opt} α_2-α_1	transflective types transmissive operation	30 20	- -	° °

For definitions of contrast ratio, viewing angles and response times see notes 1 to 3.

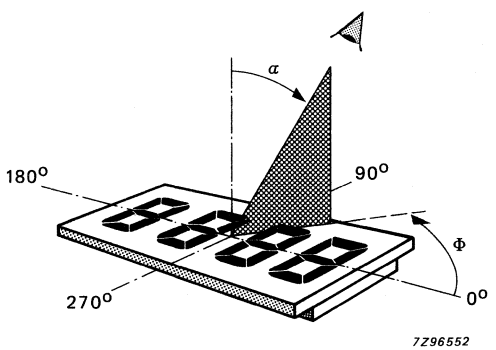
Note 1 Definition of contrast ratio (C_R).

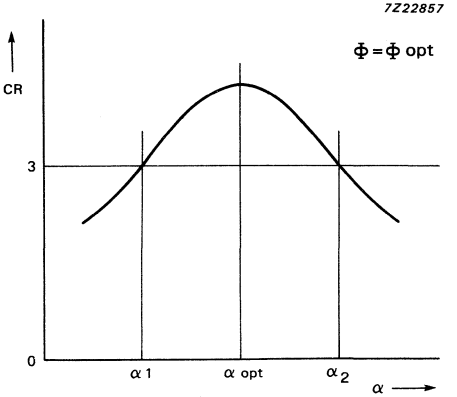
in positive image mode: $CR = \frac{B_{off}}{B_{on}}$

in negative image mode: $CR = \frac{B_{on}}{B_{off}}$

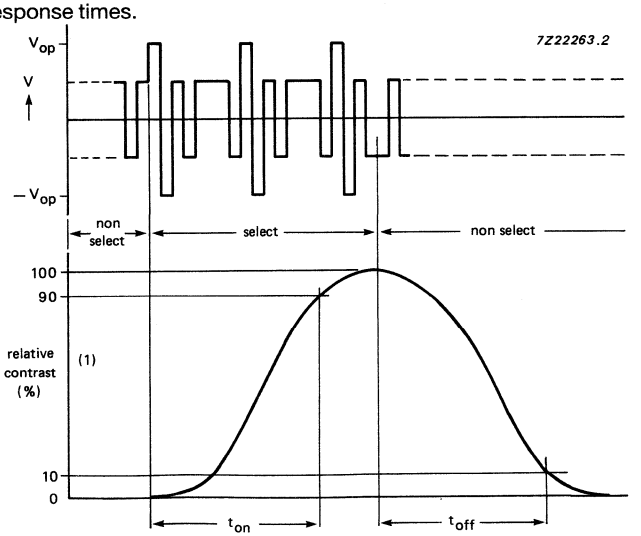
B_{on} is the brightness of selected segments
B_{off} is the brightness of non-selected segments

Note 2 Definition of viewing angles α and ϕ.



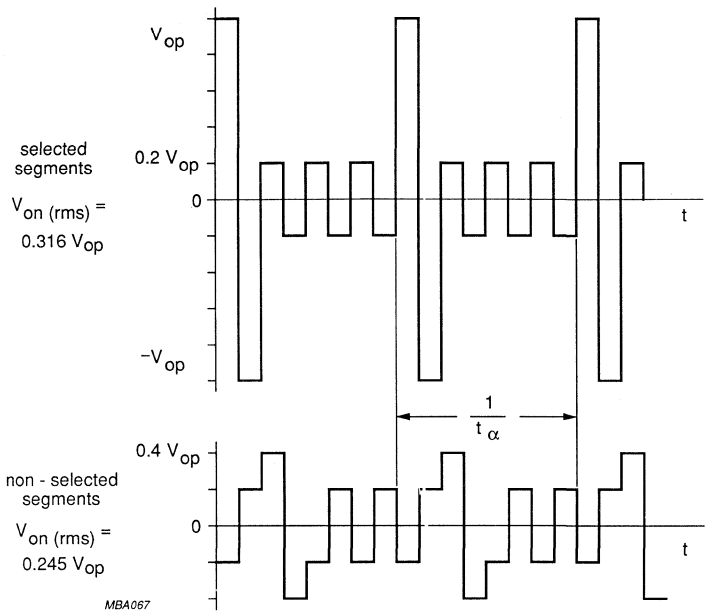


Note 3 Definition of response times.



1) measured at $\alpha = 10^o$

Note 4 Definition of waveforms.



Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTA343
Liquid Crystal Display

DEVICE DESCRIPTION

The LTA343 is a 40-character, 2-line dot matrix display. Typical applications include hand held equipment and industrial applications. The display can be inverted to adapt the optimal viewing direction to the application.

QUICK REFERENCE DATA

Viewing area dimensions	155 x 17.5 mm
Overall glass dimensions	160 x 27.4 mm
Character format	5 x 7 dots and cursor
Character size	4.85 x 3.2 mm
Dot size (spacing 0.05 mm)	0.65 x 0.60 mm
Drive method	MUX 1:16
Operating voltage	5 V
Illumination mode	reflective/trans-flective
Preferred viewing direction	6 o'clock

DISPLAY MODE

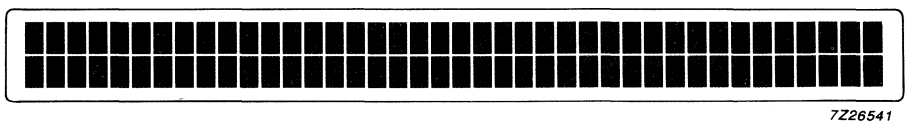


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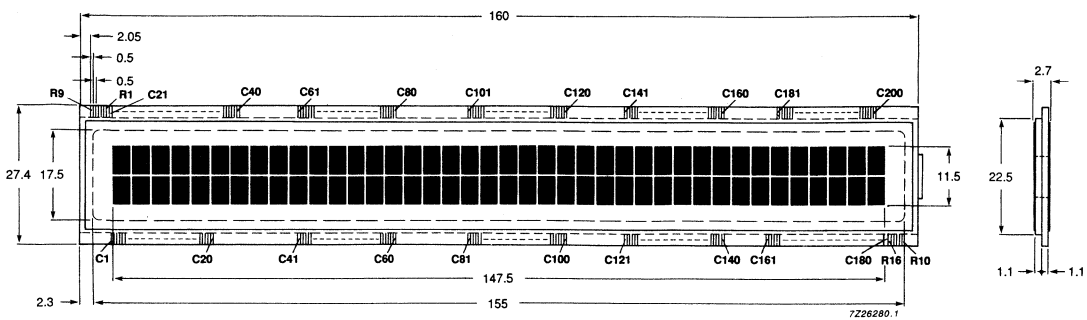
Fig.1 2-line, 40-character, dot matrix display.

TYPE DEPENDENT DATA

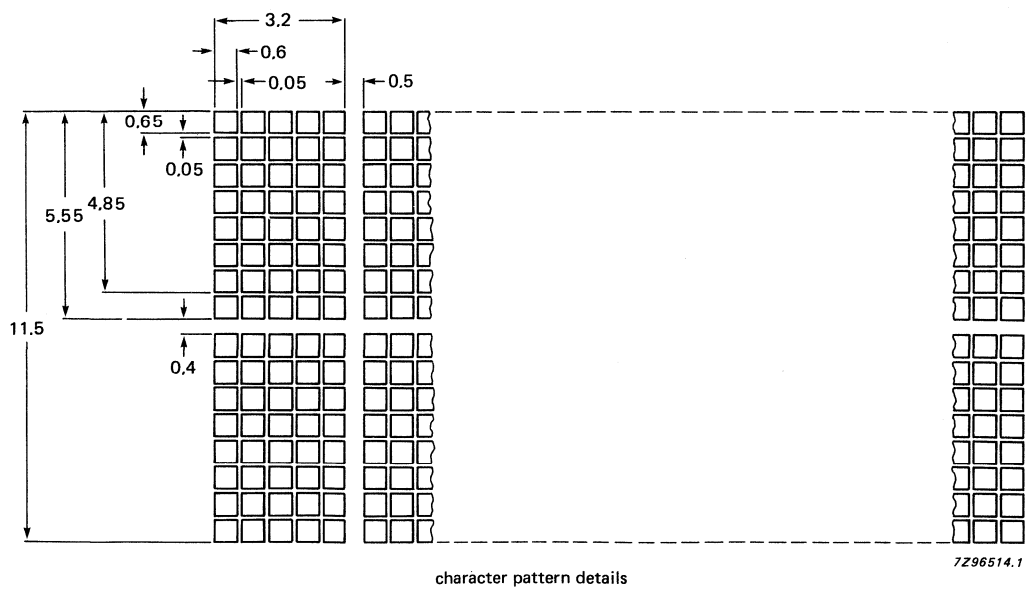
TYPE	ILLUMINATION MODE	CONNECTION METHOD	OPERATING AMBIENT TEMPERATURE RANGE	RELIABILITY GRADE
LTA343R–11	reflective	for conductive rubber	–10 to +60 °C	commercial
LTA343F–11	transflective	for conductive rubber	–10 to +60 °C	commercial

MECHANICAL DATA



PIN DESCRIPTION

R = row
C = column



character pattern details

Fig.2 Display area dimensions.

Liquid Crystal Display LTA343

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections (see note)	V_{max}	10 V RMS
Storage temperature range	T_{stg}	–25 to +70 °C

Note: maximum DC component = 0.1 V

OPERATING CONDITIONS

All values at, T_{amb} = 25 °C; $V_{op} = V_{op\ typ}$; f_{dr} = 100 Hz, unless otherwise specified

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
operating voltage	V_{op}	-	5	-	V
temperature compensation of V_{op}	TC	-	–20	-	mV/°C
operating ambient temperature	T_{amb}	–10	-	+60	°C
current consumption (see note)	I	-	287	574	µA
frame frequency	f_{dr}	30	-	100	Hz

Note: with all dots "ON".

ELECTRO-OPTICAL CHARACTERISTICS

T_{amb} = 25 °C, $V_{op} = V_{op\ typ}$, α = 10°, $\phi = \phi_{opt}$, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	TYP.	MAX.	UNIT
Response times	t_{on}	T_{amb} = 0 °C T_{amb} = 25 °C	380 110	760 220	ms ms
	t_{off}	T_{amb} = 0 °C T_{amb} = 25 °C	470 110	940 220	ms ms
Viewing Angles (contrast ratio CR > 3)	α_{opt} α_2-α_1	reflective types	35 25	- -	o o
	α_{opt} α_2-α_1	transflective types reflective operation	35 25	- -	o o
	α_{opt} α_2-α_1	transflective types transmissive operation	35 20	- -	o o

For definitions of contrast ratio, viewing angles and response times see notes 1 to 3.

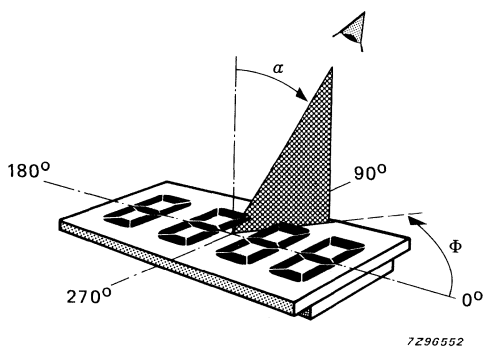
Note 1 Definition of contrast ratio (C_R).

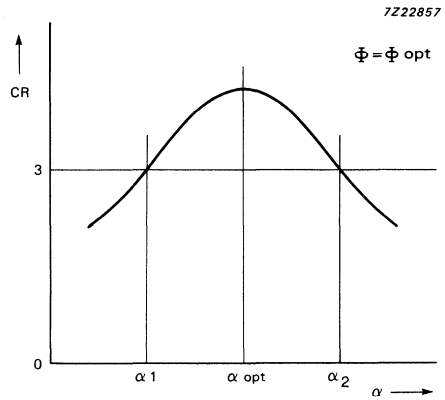
in positive image mode: $CR = \frac{B_{off}}{B_{on}}$

in negative image mode: $CR = \frac{B_{on}}{B_{off}}$

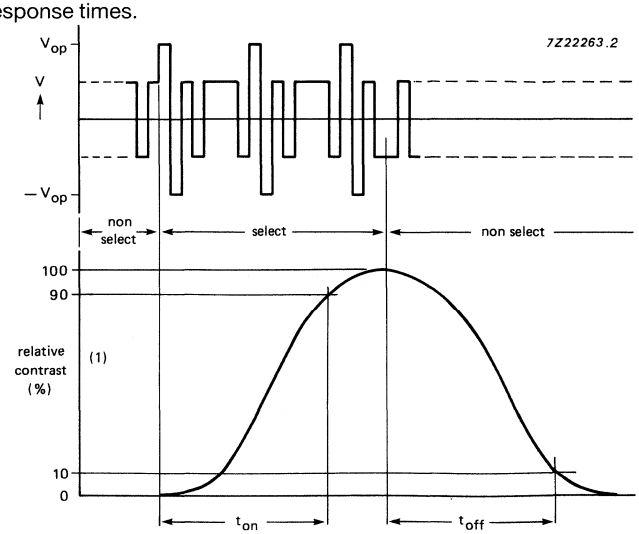
B_{on} is the brightness of selected segments
B_{off} is the brightness of non-selected segments

Note 2 Definition of viewing angles α and ϕ.



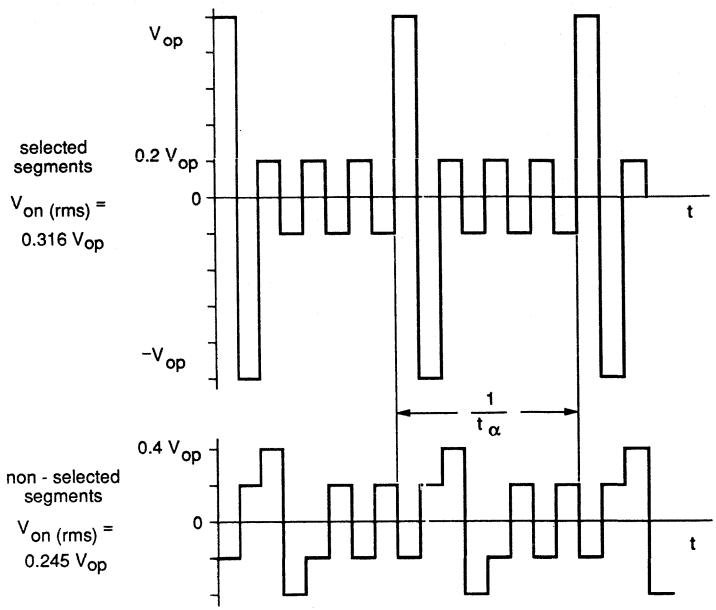


Note 3 Definition of response times.



1) measured at $\alpha' = 10^o$

Note 4 Definition of waveforms.



Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD101
Liquid crystal display

DEVICE DESCRIPTION

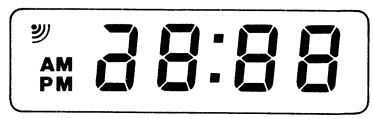
The LTD101 is a 3 1/2-digit 7 segment clock display with AM and PM functions. It is intended for use in small alarm clocks, in either 12 hr or 24 hr mode.

QUICK REFERENCE DATA

Viewing area dimensions	46.4 x 13.4 mm
Overall glass dimensions	50.8 x 22.9 mm
Thickness	2.7 +/– 0.4 mm
Digit height	8.9 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive

DISPLAY MODE

scale 1:1



7Z22295

Fig.1 Clock display.

TYPE DEPENDENT CHARACTERISTICS (1)

TYPE	ILLUMINATION MODE	CONNECTION METHOD	QUALITY GRADE	FAMILY CHARACTERISTICS (2)	OPERATING VOLTAGE (V)
LTD101R–11	reflective	for conductive rubber	commercial	TR0	3.5 – 6.5

Note: (1) drive method = direct drive
(2) see chapter "Family Characteristics" for complete specification

MECHANICAL DATA

Dimensions in mm

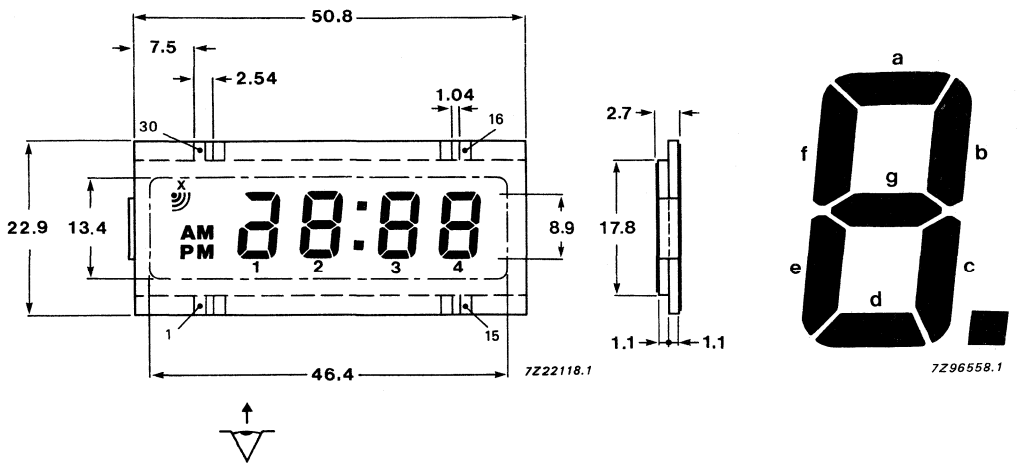


Fig.2 Display dimensions.

Liquid crystal display LTD101

PIN DESCRIPTION

PIN NO.	SEGMENT	PIN NO.	SEGMENT
1	n.c.	16	b4
2	comm	17	a4
3	PM	18	f4
4	a1,d1,e1,g1	19	g4
5	c1	20	b3
6	e2	21	a3
7	d2	22	f3
8	c2	23	g3
9	dp1	24	b2
10	e3	25	a2
11	d3	26	f2
12	c3	27	g2
13	e4	28	b1
14	d4	29	AM
15	c4	30	x

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections (see note) V_{rmax} 15 V RMS

Note: maximum DC component = 0.1 V.

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	Low temperature storage T_{amb}/duration	High temperature storage T_{amb}/duration (dry)
LTD101R–11	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD132
Liquid crystal display

DEVICE DESCRIPTION

The LTD132 is a 3 1/2-digit 7 segment clock display intended for use in alarm clocks, combined with an anologue clock display.

QUICK REFERENCE DATA

Viewing area dimensions	38.0 x 49.8 mm
Overall glass dimensions	46.8 x 54.8 mm
Thickness	2.7 +/ 0.4 mm
Digit height	5.6 mm
Preferred viewing direction	12 o'clock
Driving method	MUX 1:2

DISPLAY MODE

scale 1:1

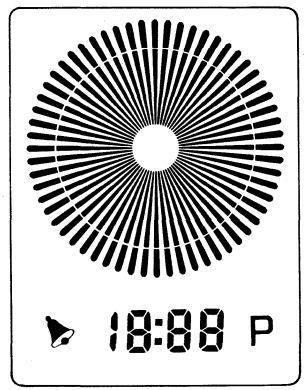


Fig.1 Analogue clock display.

TYPE DEPENDENT CHARACTERISTICS (1)

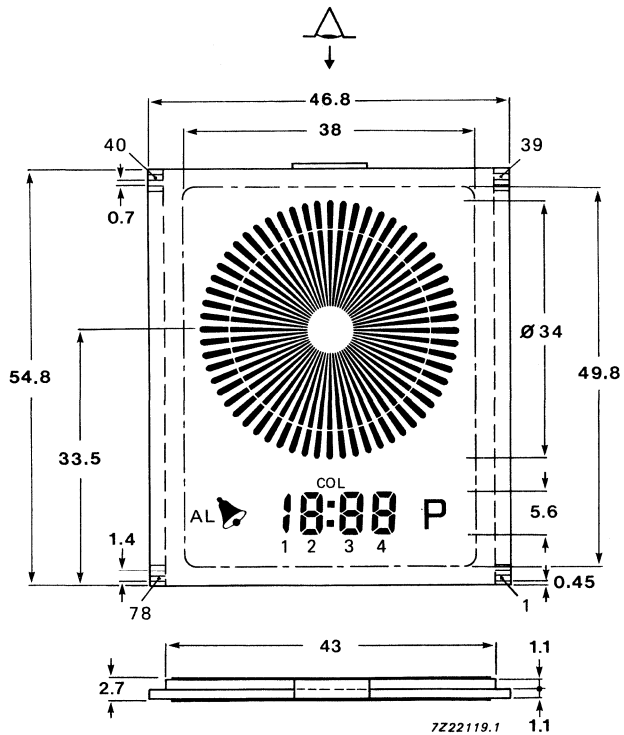
TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY CHARACTERISTICS (2)	OPERATING VOLTAGE (V)
LTD132R-11	reflective	for conductive rubber	commercial	TR1	typ. 5

Note: (1) drive method = 1:2
(2) see chapter "Family Characteristics" for complete specification

Liquid crystal display LTD132

MECHANICAL DATA

Dimensions in mm



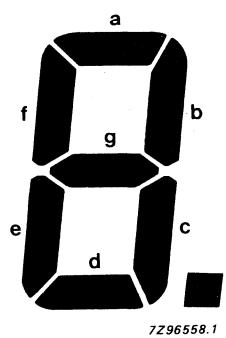


Fig.2 Display dimensions.

Liquid crystal display LTD132

PIN DESCRIPTION

PIN NO.	SEGMENT ASSIGNED TO COMMON 1	SEGMENT ASSIGNED TO COMMON 2
1	f2	e2
2	comm 1	n.c.
3	a2d2	g2
4	b2	c2
5	f3	e3
6	g3	d3
7	b3	c3
8	p	n.c.
9	a3	dp1/2
10	x29	y29
11	x28	y28
12	x27	y27
13	x26	y26
14	x25	y25
15	x24	y24
16	x23	y23
17	x22	y22
18	x21	y21
19	x20	y20
20	x19	y19
21	x18	y18
22	x17	y17
23	x16	y16
24	x15	y15
25	x14	y14
26	x13	y13
27	x12	y12
28	x11	y11
29	x10	y10
30	x9	y9
31	x8	y8
32	x7	y7
33	x6	y6
34	x5	y5
35	x4	y4
36	x3	y3
37	x2	y2
38	comm 1	n.c.
39	x1	y1

PIN NO.	SEGMENT ASSIGNED TO COMMON 1	SEGMENT ASSIGNED TO COMMON 2
40	n.c.	comm 2
41	x60	y60
42	x59	y59
43	x58	y58
44	x57	y57
45	x56	y56
46	x55	y55
47	x54	y54
48	x53	y53
49	x52	y52
50	x51	y51
51	x50	y50
52	x49	y49
53	x48	y48
54	x47	y47
55	x46	y46
56	x45	y45
57	x44	y44
58	x43	y43
59	x42	y42
60	x41	y41
61	x40	y40
62	x39	y39
63	x38	y38
64	x37	y37
65	x36	y36
66	x35	y35
67	x34	y34
68	x33	y33
69	x32	y32
70	x31	y31
71	x30	y30
72	n.c.	al
73	a1	h
74	f1	e1
75	g1	d1
76	b1	c1
77	n.c.	comm 2
78	n.c.	n.c.

Liquid crystal display LTD132

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections (see note)	V_{max}	10 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./21 days	**Low temperature storage T_{amb}/duration**	**High temperature storage T_{amb}/duration (dry)**
LTD132R-11	+40 °C/90%/21 days	25 °C/21 days	+70 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD133

Liquid crystal display

DEVICE DESCRIPTION

The LTD133 is a 3 1/2-digit 7 segment clock display with AM and PM functions. It is designed for use with the PCF1175 clock circuit.

QUICK REFERENCE DATA

Viewing area dimensions	32.5 x 14.1 mm
Overall glass dimensions	37.5 x 20.8 mm
Thickness	1.9 +/– 0.2 mm
Digit height	8.5 mm
Preferred viewing direction	12 o'clock
Driving method	MUX 1:2

DISPLAY MODE

scale 1:1

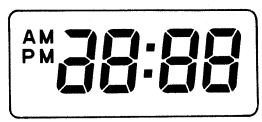


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Fig.1 Clock display.

TYPE DEPENDENT CHARACTERISTICS (1)

TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY CHARACTERISTICS (2)	OPERATING VOLTAGE (V)
LTD133F-21	transflective	for conductive rubber	extended	TF3	typ. 5

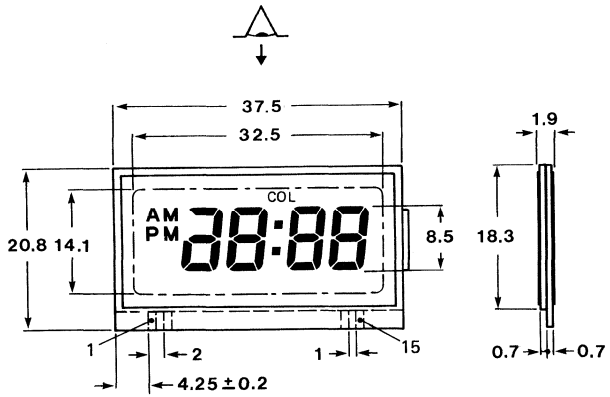
Note: (1) drive method = 1:2
(2) see chapter "Family Characteristics" for complete specification

Liquid crystal display

LTD133

MECHANICAL DATA

Dimensions in mm



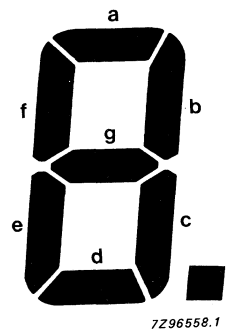


Fig.2 Display dimensions.

Liquid crystal display LTD133

PIN DESCRIPTION

PIN NO.	SEGMENT ASSIGNED TO COMMON 1	SEGMENT ASSIGNED TO COMMON 2
1	comm 1	n.c.
2	n.c.	comm 2
3	AM	PM
4	a2	adeg1
5	b1	c1
6	f2	e2
7	g2	d2
8	b2	c2
9	a4	col
10	f3	e3
11	g3	ad3
12	b3	c3
13	f4	e4
14	g4	d4
15	b4	c4

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections (see note) V_{max} 10 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./21 days	Low temperature storage T_{amb}/duration	High temperature storage T_{amb}/duration (dry)
LTD133F-21	+80 °C/90%/21 days	40 °C/21 days	+85 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD201
Liquid Crystal Display

DEVICE DESCRIPTION

The LTD201 is a 4-digit, 7-segment display. It is intended for use in applications which require a small display.

QUICK REFERENCE DATA

Viewing area dimensions	21.5 x 9.4 mm
Overall glass dimensions	23.9 x 14.0 mm
Thickness	1.6 +/– 0.4 mm
Digit height	6.8 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive

DISPLAY MODE

scale 1:1

7Z22297

Fig.1 Universal display.

TYPE DEPENDENT CHARACTERISTICS (1)

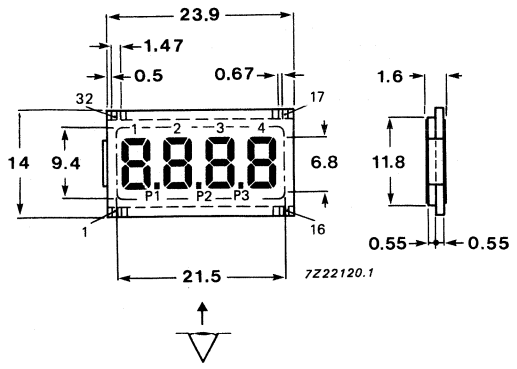
TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY CHARACTERISTICS (2)	OPERATING VOLTAGE (V)
LTD201R–11	reflective	for conductive rubber	commercial	TR0	3.5 – 6.5

Note: (1) drive method = direct drive
(2) see chapter "Family Characteristics" for complete specfication

Liquid crystal display LTD201

MECHANICAL DATA

Dimensions in mm



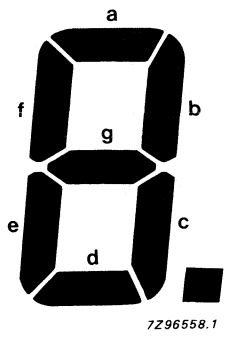


Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT	PIN NO.	SEGMENT
1	comm	17	b4
2	e1	18	a4
3	d1	19	f4
4	c1	20	g4
5	p1	21	b3
6	e2	22	a3
7	d2	23	f3
8	c2	24	g3
9	p2	25	b2
10	e3	26	a2
11	d3	27	f2
12	c3	28	g2
13	p3	29	b1
14	e4	30	a1
15	d4	31	f1
16	c4	32	g1

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections (see note) V_{max} 15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	Low temperature storage T_{amb}/duration	High temperature storage T_{amb}/duration
LTD201R–11	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD202
Liquid crystal display

DEVICE DESCRIPTION

The LTD202 is a 2-digit, 7-segment LCD. It is intended for use in small counter and indicator panel applications.

QUICK REFERENCE DATA

Viewing area dimensions	23.5 x 18.4 mm
Overall glass dimensions	27.9 x 30.4 mm
Thickness	2.7 +/– 0.4 mm
Digit height	12.7 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive

DISPLAY MODE

scale 1:1

Fig.1 Universal display.

TYPE DEPENDENT CHARACTERISTICS (1)

TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY (2) CHARACTERISTICS	OPERATING VOLTAGE (V)
LTD202R–12	reflective	with fixed pins	commercial	TR0	3.5 – 6.5
LTD202R–22	reflective	with fixed pins	extended	TR2	3.5 – 6.5
LTD202F–22	transflective	with fixed pins	extended	TF2	3.5 – 6.5

Note: (1) drive method = direct drive for all types
(2) see chapter "Family Characteristics" for complete specification

Liquid crystal display LTD202

MECHANICAL DATA

Dimensions in mm

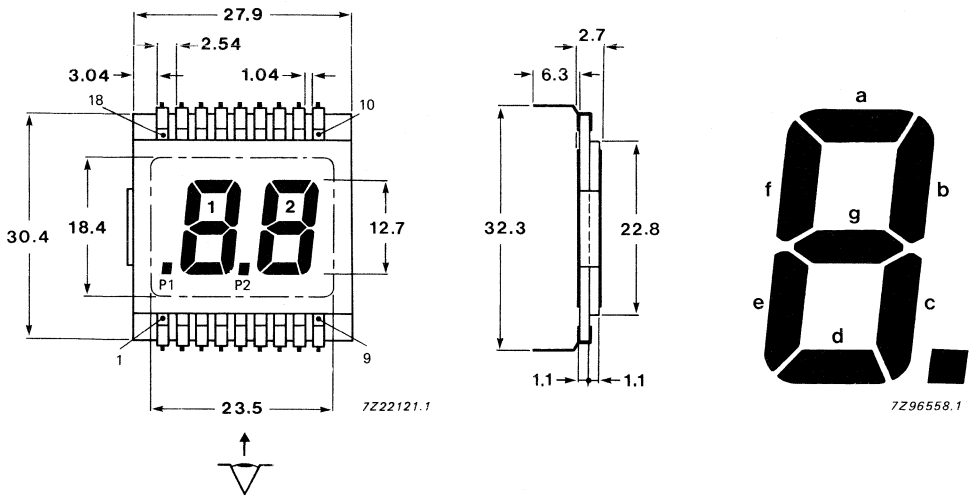


Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT
1	comm
2	p1
3	e1
4	d1
5	c1
6	p2
7	e2
8	d2
9	c2

PIN NO.	SEGMENT
10	b2
11	a2
12	f2
13	g2
14	b1
15	a1
16	f1
17	g1
18	n.c.

Liquid crystal display LTD202

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two contacts (see note)	V_{max}	15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	Low temperature storage T_{amb}/duration	High temperature storage T_{amb}/duration
LTD202R–12	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days
LTD202R–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days
LTD202F–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD203
Liquid crystal display

DEVICE DESCRIPTION

The LTD203 is a 4-digit, 7-segment multi-function LCD. Typical applications include counters, multi-meters and 24 hr clocks.

QUICK REFERENCE DATA

Viewing area dimensions	34.0 x 11.2 mm
Overall glass dimensions	38.0 x 20.3 mm
Thickness	2.2 +/– 0.4 mm
Digit height	8.0 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive

DISPLAY MODE

scale 1:1

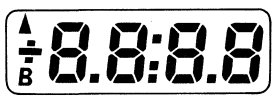


Fig.1 Universal display.

TYPE DEPENDENT CHARACTERISTICS (1)

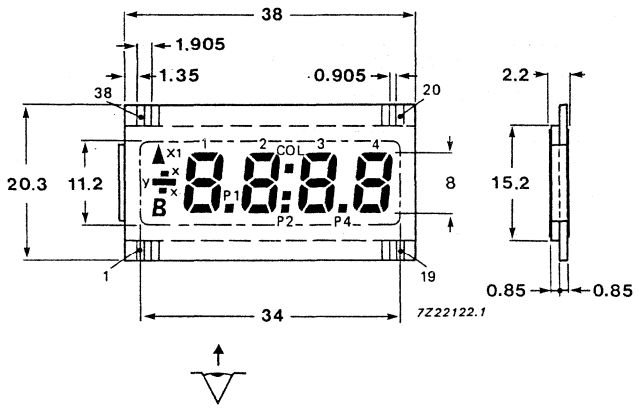
TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY (2) CHARACTERISTICS	OPERATING VOLTAGE (V)
LTD203R–11	reflective	for conductive rubber	commercial	TR0	3.5 – 6.5
LTD203R–21	reflective	for conductive rubber	extended	TR2	3.5 – 6.5
LTD203F–21	transflective	for conductive rubber	extended	TF2	3.5 – 6.5

Note: (1) drive method = direct drive for all types
(2) see chapter "Family Characteristics" for the complete specification

Liquid crystal display LTD203

MECHANICAL DATA

Dimensions in mm



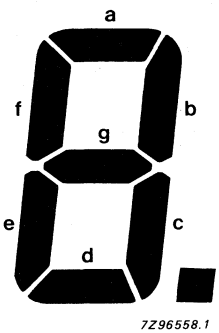


Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT
1	comm
2	B
3	e1
4	d1
5	c1
6	p1
7	e2
8	d2
9	c2
10	p2
11	e3
12	d3
13	c3
14	p4
15	e4
16	d4
17	c4
18	g4
19	n.c.

PIN NO.	SEGMENT
20	b4
21	a4
22	f4
23	g3
24	b3
25	a3
26	f3
27	col
28	g2
29	b2
30	a2
31	f2
32	g1
33	b1
34	a1
35	f1
36	y
37	x
38	X1

Liquid crystal display LTD203

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two contacts (see note)	V_{max}	15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	Low temperature storage T_{amb}/duration	High temperature storage T_{amb}/duration (dry)
LTD203R–11	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days
LTD203R–21	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days
LTD203F–21	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD211
Liquid crystal display

DEVICE DESCRIPTION

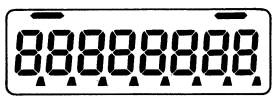
The LTD211 is an 8-digit, 7-segment multi-function display. Typical applications include cordless telephones and industrial instruments.

QUICK REFERENCE DATA

Viewing area dimensions	34.0 x 11.2 mm
Overall glass dimensions	38.0 x 20.3 mm
Thickness	2.2 +/– 0.4 mm
Digit height	6.0 mm
Preferred viewing direction	6 o'clock
Driving method	MUX 1:2

DISPLAY MODE

scale 1:1



7Z22300

Fig.1 Telecom display.

TYPE DEPENDENT CHARACTERISTICS (1)

TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY (2) CHARACTERISTICS	OPERATING VOLTAGE (V)
LTD211R–11	reflective	for conductive rubber	commercial	TR1	typ. 2.6
LTD211F–11	transflective	for conductive rubber	commercial	TF1	typ. 2.6
LTD211R–21	reflective	for conductive rubber	extended	TR2	typ. 4.1
LTD211F–21	transflective	for conductive rubber	extended	TF2	typ. 4.1

Note: (1) drive method = MUX 1:2 for all types
(2) see chapter "Family Characteristics" for complete specification

Liquid crystal display LTD211

MECHANICAL DATA

Dimensions in mm

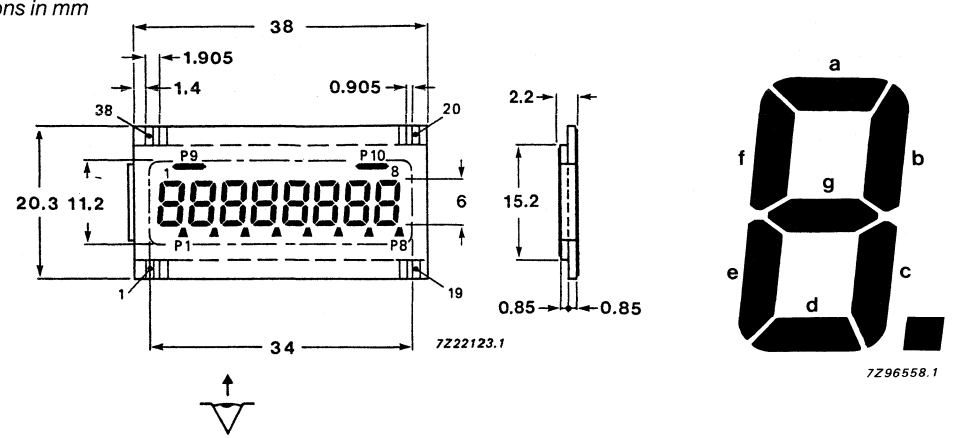


Fig.2 Display dimensions.

MULTIPLEX DUTY FACTOR 1:2

PIN NO.	COMMON 1	COMMON 2
1	n.c.	comm 2
2	g1	e1
3	c1	d1
4	g2	e2
5	c2	d2
6	g3	e3
7	c3	d3
8	g4	e4
9	c4	d4
10	g5	e5
11	c5	d5
12	g6	e6
13	c6	d6
14	g7	e7
15	c7	d7
16	g8	e8
17	c8	d8
18	n.c.	comm 2
19	comm 1	n.c.

PIN NO.	COMMON 1	COMMON 2
20	b8	p8
21	a8	f8
22	p10	nc
23	b7	p7
24	a7	f7
25	b6	p6
26	a6	f6
27	b5	p5
28	a5	f5
29	b4	p4
30	a4	f4
31	b3	p3
32	a3	f3
33	b2	p2
34	a2	f3
35	p9	n.c.
36	b1	p1
37	a1	f1
38	comm 1	n.c.

Preferred drivers: PCF2111, PCF8576, PCF8577

Liquid crystal display LTD211

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two contacts (see note) V_{max} 15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	**Low temperature storage T_{amb}/duration**	**High temperature storage T_{amb}/duration**
LTD211R–11	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days
LTD211F–11	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days
LTD211R–21	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days
LTD211F–21	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD221
Liquid crystal display

DEVICE DESCRIPTION

The LTD221 is a 3 1/2-digit, 7-segment multi-function LCD with additional indicators. Typical applications include multimeters and panelmeters.

QUICK REFERENCE DATA

Viewing area dimensions	46.8 x 18.4 mm
Overall glass dimensions	50.8 x 30.4 mm
Thickness	2.7 +/– 0.4 mm
Digit height	12.7 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive

DISPLAY MODE

scale 1:1

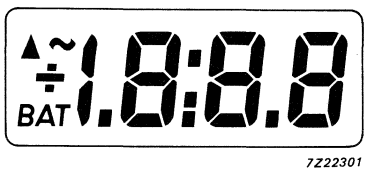


Fig.1 Multimeter display.

TYPE DEPENDENT CHARACTERISTICS (1)

TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY (2) CHARACTERISTICS	OPERATING VOLTAGE
LTD221R–11	reflective	for conductive rubber	commercial	TR0	3.5 – 6.5
LTD221R–12	reflective	with fixed pins	commercial	TR0	3.5 – 6.5
LTD221F–12	transflective	with fixed pins	commercial	TF0	3.5 – 6.5
LTD221R–22	reflective	with fixed pins	extended	TR2	3.4 – 6.5
LTD221F–22	transflective	with fixed pins	extended	TF2	3.5 – 6.5

Note: (1) drive method = direct drive for all types
(2) see chapter "Family Characteristics for complete specification

Liquid crystal display LTD221

MECHANICAL DATA

Dimensions in mm

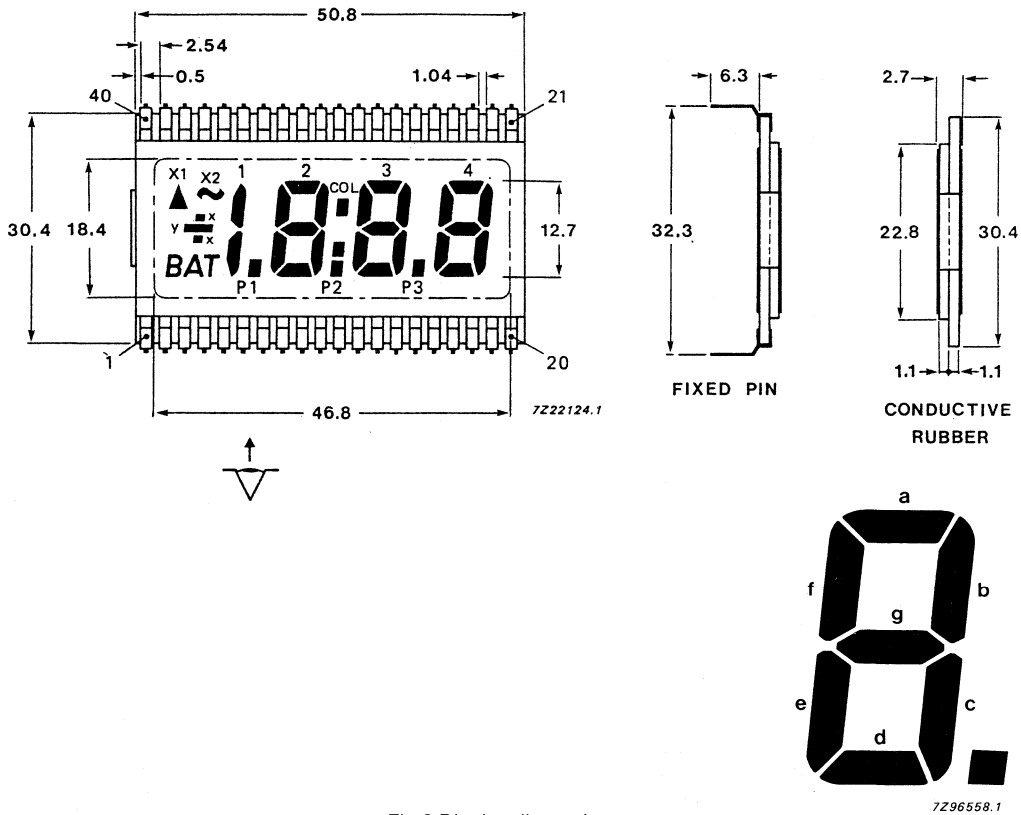


Fig.2 Display dimensions.

Liquid crystal display LTD221

PIN DESCRIPTION

PIN NO.	SEGMENT	PIN NO.	SEGMENT
1	comm	21	a3
2	y	22	f3
3	x3	23	g3
4	nc	24	b2
5	nc	25	a2
6	nc	26	f2
7	nc	27	g2
8	p1	28	col
9	e1	29	b1
10	d1	30	a1
11	c1	31	f1
12	p2	32	g1
13	e2	33	nc
14	d2	34	nc
15	c2	35	nc
16	p3	36	nc
17	e3	37	x2.
18	d3	38	x1.
19	c3	39	x
20	b3	40	BAT

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two contacts (see note) V_{max} 15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	Low temperature storage T_{amb}/duration	High temperature storage T_{amb}/duration
LTD221R–11	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days
LTD221R–12	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days
LTD221F–12	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days
LTD221R–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days
LTD221F–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD222
Liquid crystal display

DEVICE DESCRIPTION

The LTD222 is a 3 1/2-digit, 7-segment, multi-function LCD. Typical applications include multimeters and panelmeters.

QUICK REFERENCE DATA

Viewing area dimensions	46.7 x 18.4 mm
Overall glass dimensions	50.7 x 30.4 mm
Thickness	2.7 +/– 0.4 mm
Digit height	12.7 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive

DISPLAY MODE

scale 1:1

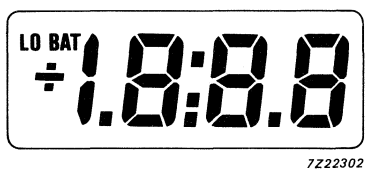


Fig.1 Multimeter display.

TYPE DEPENDENT CHARACTERISTICS (1)

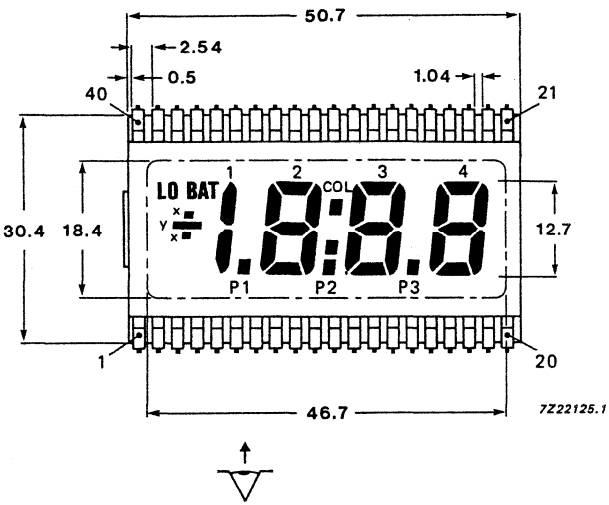
TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY (2) CHARACTERISTICS	OPERATING VOLTAGE (V)
LTD222R–11	reflective	for conductive rubber	commercial	TR0	3.5 – 6.5
LTD222R–12	reflective	with fixed pins	commercial	TR0	3.5 – 6.5
LTD222F–12	transflective	with fixed pins	commercial	TF0	3.5 – 6.5
LTD222R–21	reflective	for conductive rubber	extended	TR2	3.5 – 6.5
LTD222F–21	transflective	for conductive rubber	extended	TF2	3.5 – 6.5
LTD222R–22	reflective	with fixed pins	extended	TR2	3.5 – 6.5
LTD222F–22	transflective	with fixed pins	extended	TF2	3.5 – 6.5

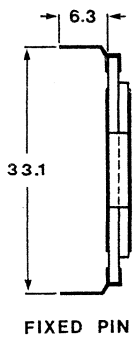
Note: (1) drive method = direct drive for all types
(2) see chapter "Family Characteristics" for complete specification

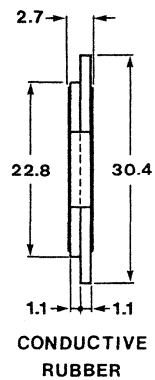
Liquid crystal display LTD222

MECHANICAL DATA

Dimensions in mm







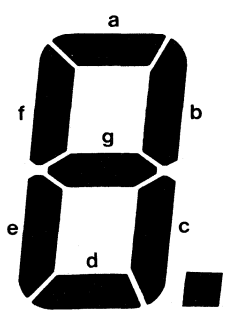


Fig.2 Display dimensions.

Liquid crystal display LTD222

PIN DESCRIPTION

PIN NO.	SEGMENT
1	comm
2	y
3	1
4	n.c.
5	n.c.
6	n.c.
7	n.c.
8	p1
9	e2
10	d2
11	c2
12	p2
13	e3
14	d3
15	c3
16	p3
17	e4
18	d4
19	c4
20	b4

PIN NO.	SEGMENT
21	a4
22	f4
23	g4
24	b3
25	a3
26	f3
27	g3
28	col
29	b2
30	a2
31	f2
32	g2
33	n.c.
34	n.c.
35	n.c.
36	n.c.
37	n.c.
38	LOBAT
39	x
40	comm

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two contacts (see note) V_{max} 15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	Low temperature storage T_{amb}/duration	High temperature storage T_{amb}/duration
LTD222R–11	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days
LTD222R–12	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days
LTD222F–12	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days
LTD222R–21	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days
LTD222F–21	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days
LTD222R–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days
LTD222F–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD224
Liquid crystal display

DEVICE DESCRIPTION

The LTD224 is a 3 1/2-digit, 7-segment multi-function display. It is intended for use in multimeters and panel-meters.

QUICK REFERENCE DATA

Viewing area dimensions	45.8 x 17.8 mm
Overall glass dimensions	50.8 x 30.4 mm
Thickness	2.7 +/– 0.4 mm
Digit height	12.7 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive

DISPLAY MODE

scale 1:1

Fig. 1 Multimeter display.

TYPE DEPENDENT CHARACTERISTICS (1)

TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY (2) CHARACTERISTICS	OPERATING VOLTAGE (V)
LTD224R–11	reflective	for conductive rubber	commercial	TR0	3.5 – 6.5

Note: (1) drive method = direct drive
(2) see chapter "Family Characteristics" for complete specification

MECHANICAL DATA

Dimensions in mm

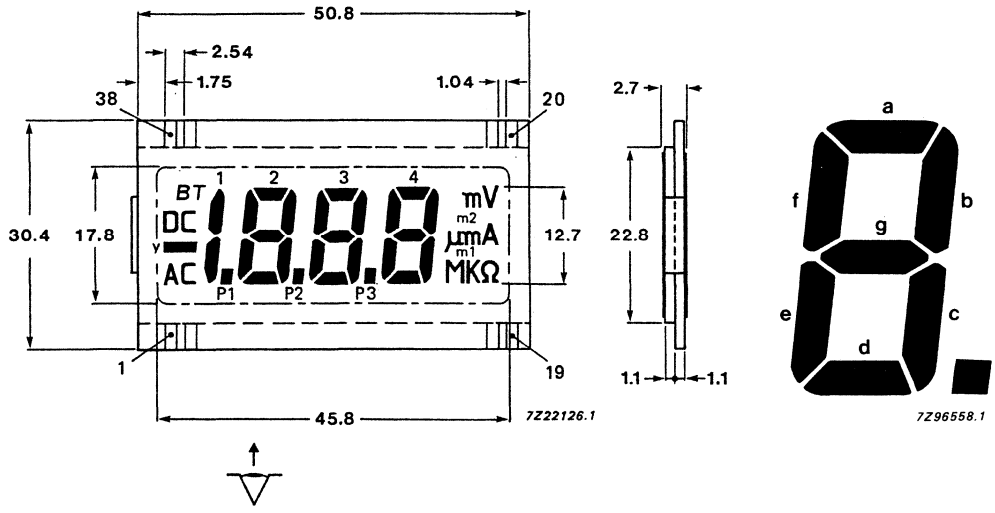


Fig.2 Display dimensions.

Liquid crystal display LTD224

PIN DESCRIPTION

PIN NO.	SEGMENT	PIN NO.	SEGMENT
1	AC	20	V
2	y	21	m2
3	1	22	m1
4	p1	23	μ
5	e2	24	b4
6	d2	25	a4
7	c2	26	f4
8	p2	27	g4
9	e3	28	b3
10	d3	29	a3
11	c3	30	f3
12	p3	31	g3
13	e4	32	b2
14	d4	33	a2
15	c4	34	f2
16	M	35	g2
17	K	36	BT
18	Ω	37	DC
19	A	38	comm

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections (see note) V_{max} 15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	Low temperature storage T_{amb}/duration	High temperature storage T_{amb}/duration
LTD224R–11	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD225
Liquid crystal display

DEVICE DESCRIPTION

The LTD225 is a 3 1/2-digit, 7-segment multi-function display. It is intended for use in multimeters and panel-meters.

QUICK REFERENCE DATA

Viewing area dimensions	45.8 x 17.8 mm
Overall glass dimensions	50.8 x 30.4 mm
Thickness	2.7 +/– 0.4 mm
Digit height	12.7 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive

DISPLAY MODE

scale 1:1

Fig.1 Multimeter display.

TYPE DEPENDENT CHARACTERISTICS (1)

TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY (2) CHARACTERISTICS	OPERATING VOLTAGE (V)
LTD225R–11	reflective	for conductive rubber	commercial	TR0	3.5 – 6.5

Note: (1) drive method = direct drive
(2) see chapter "Family Characteristics" for complete specification

Liquid crystal display LTD225

MECHANICAL DATA

Dimensions in mm

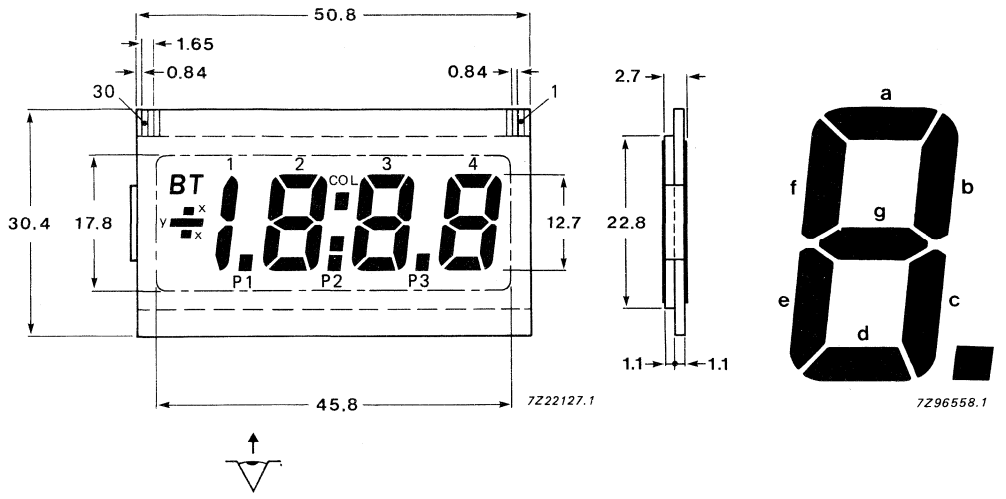


Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT
1	d2
2	c2
3	b2
4	a2
5	f2
6	g2
7	e2
8	p3
9	d3
10	c3
11	b3
12	a3
13	f3
14	g3
15	e3

PIN NO.	SEGMENT
16	col
17	p2
18	d2
19	c2
20	b2
21	a2
22	f2
23	g2
24	e2
25	p1
26	1
27	y
28	x
29	BT
30	comm

Liquid crystal display LTD225

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections (see note)	V_{max}	15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	**Low temperature storage T_{amb}/duration**	**High temperature storage T_{amb}/duration**
LTD225R–11	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD226
Liquid crystal display

DEVICE DESCRIPTION

The LTD226 is a 4-digit, 7-segment, multi-function LCD. Typical applications include 24 hr. clocks and industrial equipment.

QUICK REFERENCE DATA

Viewing area dimensions	46.7 x 18.4 mm
Overall glass dimensions	50.7 x 30.4 mm
Thickness	2.7 +/– 0.4 mm
Digit height	12.7 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive

DISPLAY MODE

scale 1:1

Fig.1 Universal display.

TYPE DEPENDENT CHARACTERISTICS (1)

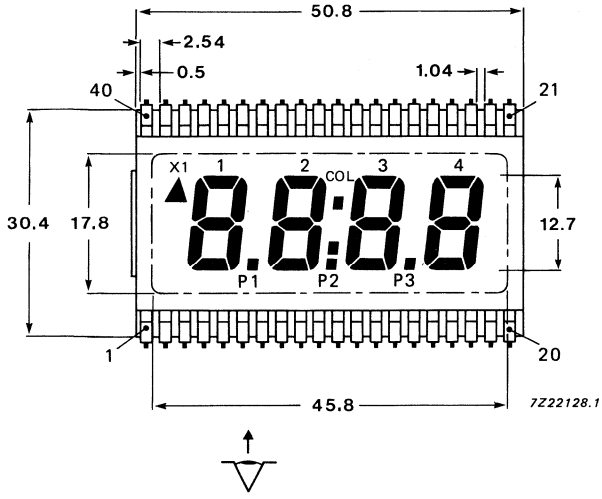
TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY (2) CHARACTERISTICS	OPERATING VOLTAGE (V)
LTD226R–11	reflective	for conductive rubber	commercial	TR0	3.5 – 6.5
LTD226R–12	reflective	with fixed pins	commercial	TR0	3.5 – 6.5
LTD226F–12	transflective	with fixed pins	commercial	TF0	3.5 – 6.5
LTD226R–21	reflective	for conductive rubber	extended	TR2	3.5 – 6.5
LTD226F–21	transflective	for conductive rubber	extended	TF2	3.5 – 6.5
LTD226R–22	reflective	with fixed pins	extended	TR2	3.5 – 6.5
LTD226F–22	transflective	with fixed pins	extended	TF2	3.5 – 6.5

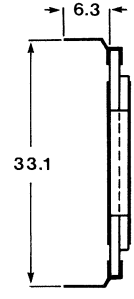
Note: (1) drive method = direct drive for all types
(2) see chapter "Family Characteristics" for complete specification

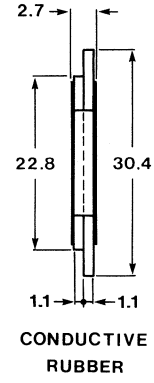
Liquid crystal display LTD226

MECHANICAL DATA

Dimensions in mm







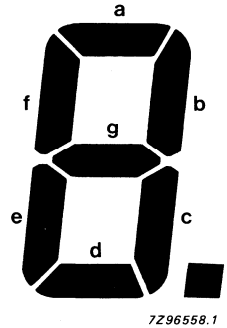


Fig.2 Display dimensions.

Liquid crystal display LTD226

PIN DESCRIPTION

PIN NO.	SEGMENT	PIN NO.	SEGMENT
1	comm	21	a4
2	n.c.	22	f4
3	n.c.	23	g4
4	n.c.	24	b3
5	e1	25	a3
6	d1	26	f3
7	c1	27	g3
8	p1	28	col
9	e2	29	b2
10	d2	30	a2
11	c2	31	f2
12	p2	32	g2
13	e3	33	n.c.
14	d3	34	b1
15	c3	35	a1
16	p3	36	f1
17	e4	37	g1
18	d4	38	x1
19	c4	39	n.c.
20	b4	40	comm

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two contacts (see note) V_{max} 15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	Low temperature storage T_{amb}/duration	High temperature storage T_{amb}/duration (dry)
LTD226R–11	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days
LTD226R–12	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days
LTD226F–12	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days
LTD226R–21	+85 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days
LTD226F–21	+85 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days
LTD226R–22	+85 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days
LTD226F–22	+85 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD227
Liquid crystal display

DEVICE DESCRIPTION

The LTD227 is a 4 1/2-digit, 7-segment multi-function LCD. Typical applications include panelmeters and multimeters.

QUICK REFERENCE DATA

Viewing area dimensions	46.8 x 18.8 mm
Overall glass dimensions	50.8 x 30.4 mm
Thickness	2.7 +/– 0.4 mm
Digit height	10.0 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive

DISPLAY MODE

scale 1:1

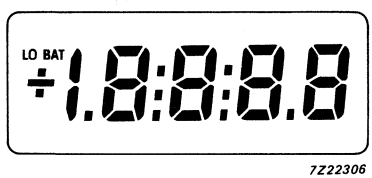


Fig.1 Multimeter display.

TYPE DEPENDENT CHARACTERISTICS (1)

TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY (2) CHARACTERISTICS	OPERATING VOLTAGE (V)
LTD227R–12	reflective	with fixed pins	commercial	TR0	3.5 – 6.5
LTD227R–22	reflective	with fixed pins	extended	TR2	3.5 – 6.5
LTD227F–22	transflective	with fixed pins	extended	TF2	3.5 – 6.5

Note: (1) drive method = direct drive for all types
(2) see chapter "Family characteristics for complete specfication

Liquid crystal display LTD227

MECHANICAL DATA

Dimensions in mm

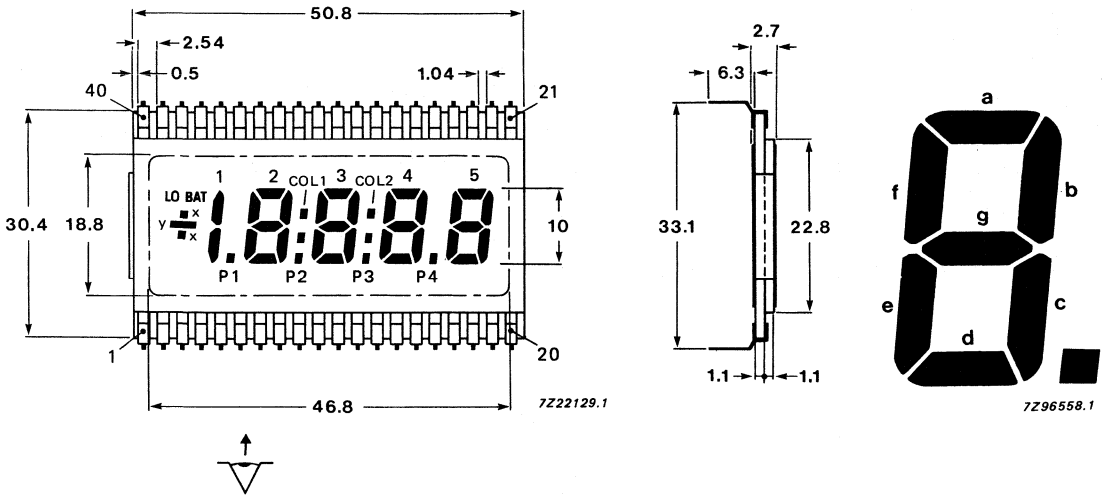


Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT
1	comm
2	y
3	1
4	p1
5	e2
6	d2
7	c2
8	p2
9	e3
10	d3
11	c3
12	p3
13	e4
14	d4
15	c4
16	p4
17	e5
18	d5
19	c5
20	b5

PIN NO.	SEGMENT
21	a5
22	f5
23	g5
24	b4
25	a4
26	f4
27	g4
28	col2
29	b3
30	a3
31	f3
32	g3
33	col1
34	b2
35	a2
36	f2
37	g2
38	LOBAT
39	x
40	n.c.

Liquid crystal display LTD227

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two contacts (see note)	V_{max}	15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	Low temperature storage T_{amb}/duration	High temperature storage T_{amb}/duration (dry)
LTD227R–12	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days
LTD227R–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days
LTD227F–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD228
Liquid crystal display

DEVICE DESCRIPTION

The LTD228 is a 5-digit, 7-segment multi-function display. Typical applications include counters and instruments.

QUICK REFERENCE DATA

Viewing area dimensions	45.8 x 17.8 mm
Overall glass dimensions	50.8 x 30.4 mm
Thickness	2.7 +/– 0.4 mm
Digit height	10.0 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive

DISPLAY MODE

scale 1:1

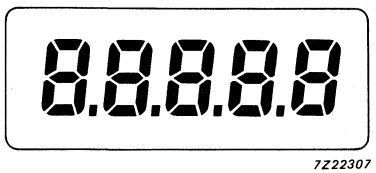


Fig.1 Universal display.

TYPE DEPENDENT CHARACTERISTICS (1)

TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY (2) CHARACTERISTICS	OPERATING VOLTAGE (V)
LTD228R–12	reflective	with fixed pins	commercial	TR0	3.5 – 6.5

Note: (1) drive method = direct drive
(2) see chapter "Family Characteristics" for complete specification

Liquid crystal display LTD228

MECHANICAL DATA

Dimensions in mm

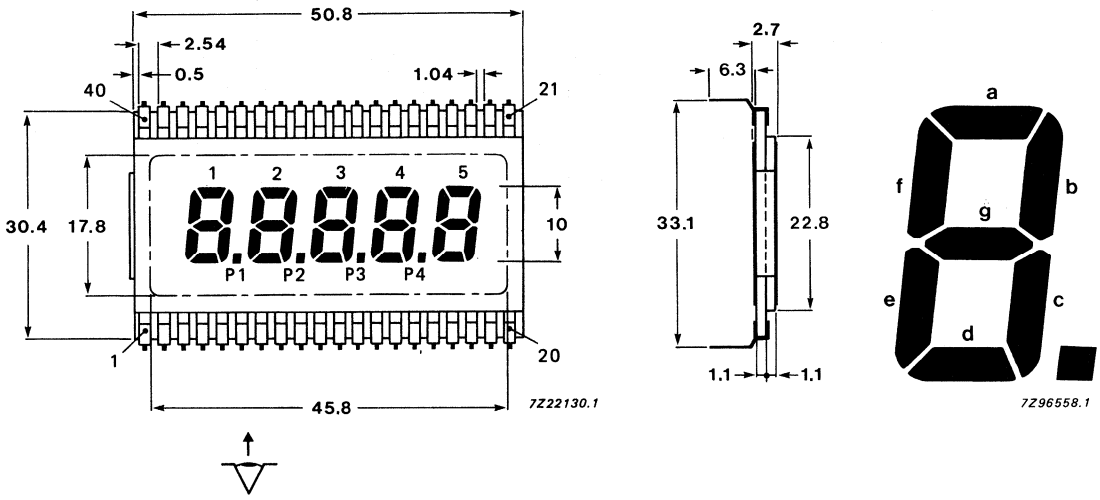


Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT
1	comm
2	g1
3	e1
4	d1
5	c1
6	e2
7	d2
8	c2
9	e3
10	d3
11	c3
12	p3
13	e4
14	d4
15	c4
16	p4
17	e5
18	d5
19	c5
20	b5

PIN NO.	SEGMENT
21	a5
22	f5
23	g5
24	b4
25	a4
26	f4
27	g4
28	b3
29	a3
30	f3
31	g3
32	p2
33	b2
34	a2
35	f2
36	g2
37	p1
38	b1
39	a1
40	f1

Liquid crystal display LTD228

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections (see note)	V_{max}	15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	**Low temperature storage T_{amb}/duration**	**High temperature storage T_{amb}/duration (dry)**
LTD228R–12	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD229
Liquid crystal display

DEVICE DESCRIPTION

The LTD229 is a 6-digit, 7-segment multi-function LCD. Typical applications include 24 hr. clocks with a seconds display, counters, and instruments requiring a large display.

QUICK REFERENCE DATA

Viewing area dimensions	65.8 x 18.4 mm
Overall glass dimensions	69.8 x 30.4 mm
Thickness	2.7 +/– 0.4 mm
Digit height	12.7 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive

DISPLAY MODE

scale 1:1

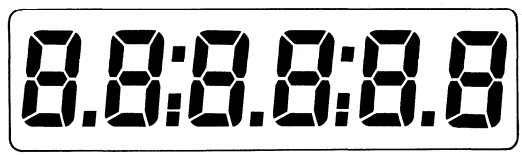


Fig.1 Universal display.

TYPE DEPENDENT CHARACTERISTICS (1)

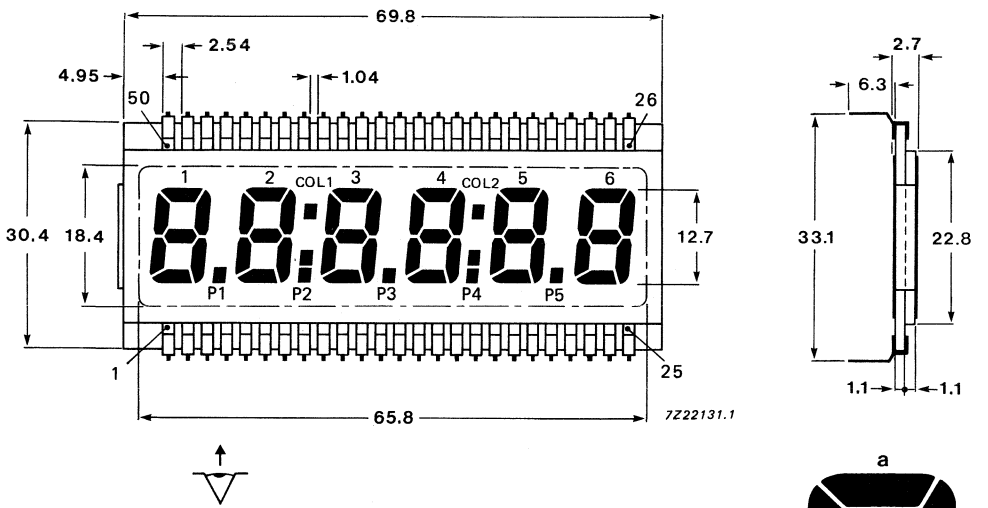
TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY (2) CHARACTERISTICS	OPERATING VOLTAGE (V)
LTD229R–12	reflective	with fixed pins	commercial	TR0	3.5 – 6.5
LTD229R–22	reflective	with fixed pins	extended	TR2	3.5 – 6.5
LTD229F–22	transflective	with fixed pins	extended	TF2	3.5 – 6.5

Note: (1) drive method = direct drive for all types
(2) see chapter "Family Characteristics for complete specification

Liquid crystal display LTD229

MECHANICAL DATA

Dimensions in mm



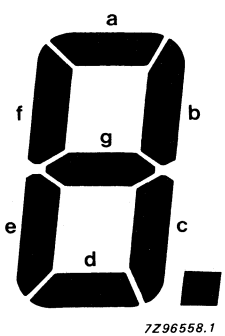


Fig.2 Display dimensions.

Liquid crystal display LTD229

PIN DESCRIPTION

PIN NO.	SEGMENT	PIN NO.	SEGMENT
1	comm	26	a6
2	e1	27	f6
3	d1	28	g6
4	c1	29	b5
5	p1	30	a5
6	e2	31	f5
7	d2	32	g5
8	c2	33	col2
9	p2	34	b4
10	e3	35	a4
11	d3	36	f4
12	c3	37	g4
13	p3	38	b3
14	e4	39	a3
15	d4	40	f3
16	c4	41	g3
17	p4	42	col1
18	e5	43	b2
19	d5	44	a2
20	c5	45	f2
21	p5	46	g2
22	e6	47	b1
23	d6	48	a1
24	c6	49	f1
25	b6	50	g1

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two contacts (see note) V_{max} 15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	Low temperature storage T_{amb}/duration	High temperature storage T_{amb}/duration (dry)
LTD229R–12	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days
LTD229R–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days
LTD229F–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD231
Liquid Crystal Display

DEVICE DESCRIPTION

The LTD231 is a 3 1/2-digit, 7-segment multi-function display. It is intended for use in multimeters and panel-meters.

QUICK REFERENCE DATA

Viewing area dimensions	45.8 x 17.1 mm
Overall glass dimensions	50.8 x 30.4 mm
Thickness	2.7 +/– 0.4 mm
Digit height	10.2 mm
Preferred viewing direction	6 o'clock
Driving method	MUX 1:3

DISPLAY MODE

scale 1:1

Fig.1 Multimeter display.

TYPE DEPENDENT CHARACTERISTICS (1)

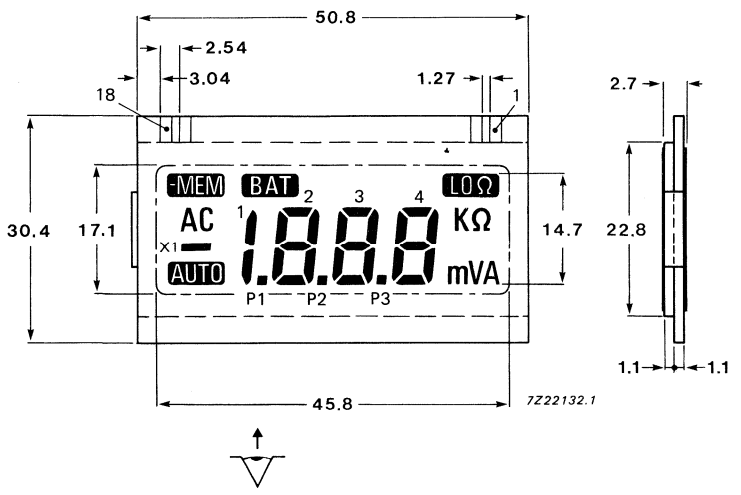
TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY CHARACTERISTICS (2)	OPERATING VOLTAGE (V)
LTD231R–11	reflective	for conductive rubber	commercial	TR1	typ. 2.8

Note: (1) drive method = MUX 1:3
(2) see chapter "Family Characteristics" for complete specification

Liquid crystal display LTD231

MECHANICAL DATA

Dimensions in mm



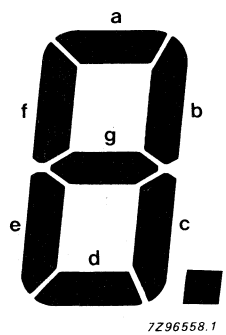


Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENTS ASSIGNED TO COMMON 1	SEGMENTS ASSIGNED TO COMMON 2	SEGMENTS ASSIGNED TO COMMON 3
1	comm 1	n.c.	n.c.
2	n.c.	comm 2	n.c.
3	n.c.	n.c.	comm 3
4	n.c.	LOΩ	A
5	n.c.	Ω	V
6	n.c.	K	m
7	b4	c4	n.c.
8	a4	g4	d4
9	f4	e4	n.c.
10	b3	c3	p3
11	a3	g3	d3
12	f3	e3	n.c.
13	b2	c2	p2
14	a2	g2	d2
15	f2	e2	n.c.
16	b1	c1	p1
17	AC	x1	AUTO
18	BAT	-MEM	n.c.

Liquid crystal display LTD231

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections (see note)	V_{max}	15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	**Low temperature storage T_{amb}/duration**	**High temperature storage T_{amb}/duration (dry)**
LTD231R–11	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD232

Liquid crystal display

DEVICE DESCRIPTION

The LTD232 is a 4 1/2-digit, 7-segment multi-function display. It is intended for use in multimeters and panel-meters.

QUICK REFERENCE DATA

Viewing area dimensions	44.8 x 16.8 mm
Overall glass dimensions	50.8 x 30.4 mm
Thickness	2.7 +/– 0.4 mm
Digit height	11.0 mm
Preferred viewing direction	6 o'clock
Driving method	MUX 1:3

DISPLAY MODE

scale 1:1

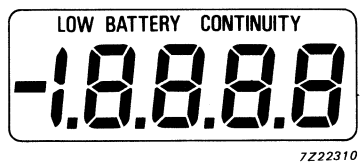


Fig.1 Multimeter display.

TYPE DEPENDENT CHARACTERISTICS (1)

TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY CHARACTERISTICS (2)	OPERATING VOLTAGE (V)
LTD232R-11	reflective	for conductive rubber	commercial	TR1	typ. 2.8

Note: (1) drive method = MUX 1:3
(2) see chapter "Family Characteristics" for complete specification

Liquid crystal display LTD232

MECHANICAL DATA

Dimensions in mm

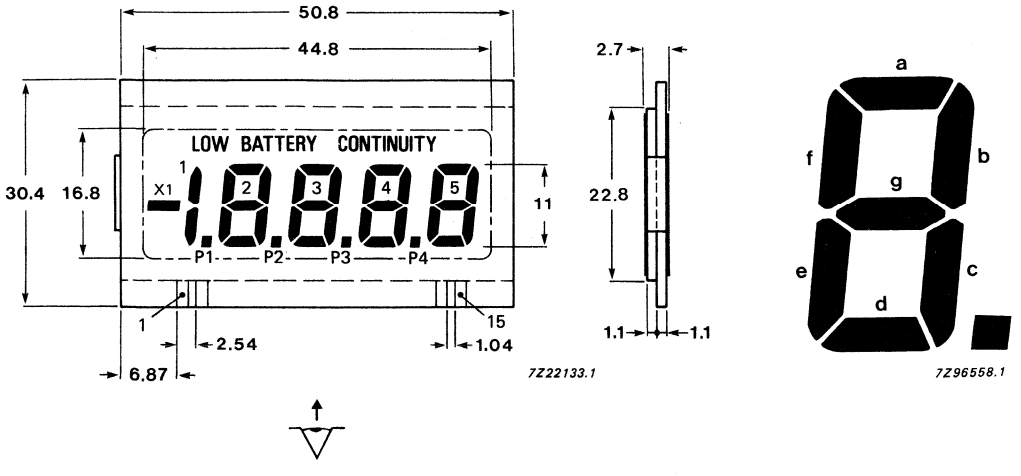


Fig.2 Display dimensions.

Liquid crystal display LTD232

PIN DESCRIPTION

PIN NO.	SEGMENTS ASSIGNED TO COMMON 1	SEGMENTS ASSIGNED TO COMMON 2	SEGMENTS ASSIGNED TO COMMON 3
1	f2	e2	p1
2	a2	g2	d2
3	b2	c2	1
4	f3	e3	p2
5	a3	g3	d3
6	b3	c3	x1
7	f4	e4	p3
8	a4	g4	d4
9	b4	c4	LOW BATTERY
10	f5	e5	p4
11	a5	g5	d5
12	b5	c5	CONTINUITY
13	comm 1	n.c.	n.c.
14	n.c.	comm 2	n.c.
15	n.c.	n.c.	comm 3

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections (see note) V_{max} 15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	Low temperature storage T_{amb}/duration	High temperature storage T_{amb}/duration (dry)
LTD232R-11	+40 °C/90%/21 days	25 °C/21 days	+70 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD233
Liquid crystal display

DEVICE DESCRIPTION

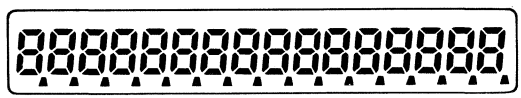
The LTD233 is a 16-digit, 7-segment display used for telephony.

QUICK REFERENCE DATA

Viewing area dimensions	65.8 x 11.2 mm
Overall glass dimensions	69.8 x 20.3 mm
Thickness	2.2 +/– 0.4 mm
Digit height	6.0 mm
Preferred viewing direction	6 o'clock
Driving method	MUX 1:2

DISPLAY MODE

scale 1:1



7Z22311

Fig.1 Telecom display.

TYPE DEPENDENT CHARACTERISTICS (1)

TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY (2) CHARACTERISTICS	OPERATING VOLTAGE (V)
LTD233R–11	reflective	for conductive rubber	commercial	TR1	typ. 2.6

Note: (1) drive method = MUX 1:2
(2) see chapter "Family Characteristics" for complete specification

Liquid crystal display LTD233

MECHANICAL DATA

Dimensions in mm

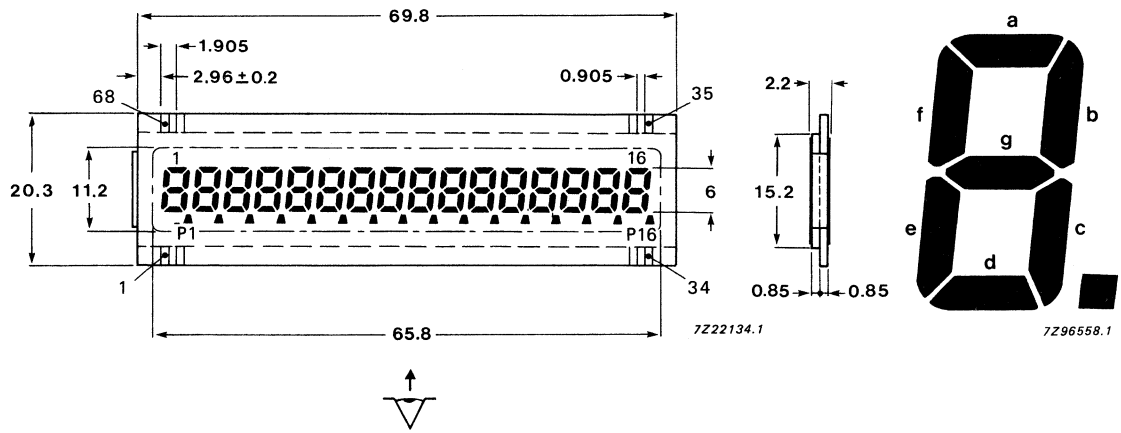


Fig.2 Display dimensions.

Liquid crystal display LTD233

PIN DESCRIPTION

PIN NO.	SEGMENTS ASSIGNED TO COMMON 1	SEGMENTS ASSIGNED TO COMMON 2
1	n.c.	comm 2
2	g1	e1
3	c1	d1
4	g2	e2
5	c2	d2
6	g3	e3
7	c3	d3
8	g4	e4
9	c4	d4
10	g5	e5
11	c5	d5
12	g6	e6
13	c6	d6
14	g7	e7
15	c7	d7
16	g8	e8
17	c8	d8
18	g9	e9
19	c9	d9
20	g10	e10
21	c10	d10
22	g11	e1
23	c11	d11
24	g12	e12
25	c12	d12
26	g13	e13
27	c13	d13
28	g14	e14
29	c14	d14
30	g15	e15
31	c15	d15
32	g16	e16
33	c16	d16
34	n.c.	comm 2

PIN NO.	SEGMENTS ASSIGNED TO COMMON 1	SEGMENTS ASSIGNED TO COMMON 2
35	comm 1	n.c.
36	b16	P16
37	a16	f16
38	b15	P15
39	a15	f15
40	b14	P14
41	a14	f14
42	b13	P13
43	a13	f13
44	b12	P12
45	a12	f12
46	b11	P11
47	a11	f11
48	b10	P10
49	a10	f10
50	b9	P9
51	a9	f9
52	b8	P8
53	a8	f8
54	b7	P7
55	a7	f7
56	b6	P6
57	a6	f6
58	b5	P5
59	a5	f5
60	b4	P4
61	a4	f4
62	b3	P3
63	a3	f3
64	b2	P2
65	a2	f2
66	b1	P1
67	a1	f1
68	comm 1	n.c.

Liquid crystal display LTD233

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections (see note)	V_{max}	15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	Low temperature storage T_{amb}/duration	High temperature storage T_{amb}/duration (dry)
LTD233R–11	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD234
Liquid Crystal Display

DEVICE DESCRIPTION

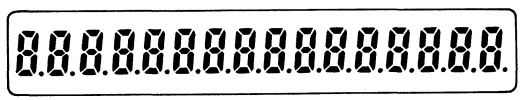
The LTD234 is a 16-digit, 7-segment display used for telephony.

QUICK REFERENCE DATA

Viewing area dimensions	65.8 x 11.2 mm
Overall glass dimensions	69.8 x 20.3 mm
Thickness	2.2 +/– 0.4 mm
Digit height	6.0 mm
Preferred viewing direction	6 o'clock
Driving method	MUX 1:4

DISPLAY MODE

scale 1:1



7Z22312

Fig.1 Telecom display.

TYPE DEPENDENT CHARACTERISTICS (1)

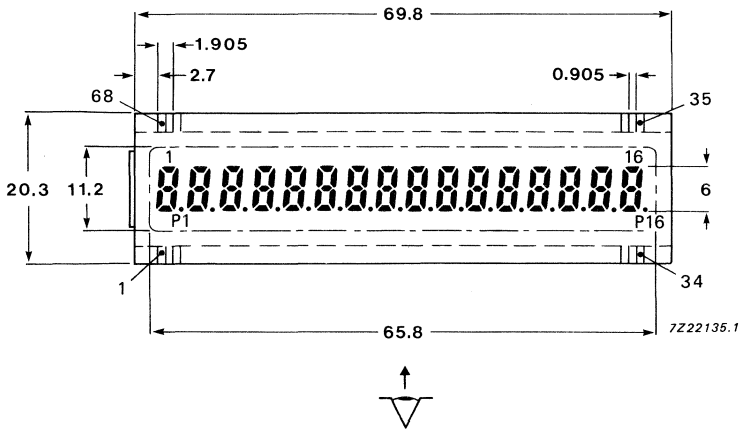
TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY CHARACTERISTICS (2)	OPERATING VOLTAGE (V)
LTD234R–21	reflective	for conductive rubber	extended	TR2	typ. 4.3

Note: (1) drive method = MUX 1:4
(2) see chapter "Family Characteristics" for complete speification

Liquid crystal display LTD234

MECHANICAL DATA

Dimensions in mm



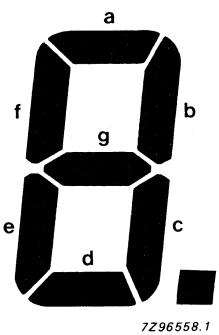


Fig.2 Display dimensions.

Liquid crystal display LTD234

PIN DESCRIPTION

PIN NO.	SEGMENTS ASSIGNED TO COMMON 1	SEGMENTS ASSIGNED TO COMMON 2	SEGMENTS ASSIGNED TO COMMON 3	SEGMENTS ASSIGNED TO COMMON 4
1	comm 1	n.c.	n.c.	n.c.
2	comm 1	n.c.	n.c.	n.c.
3	e1	d1	g1	f1
4	e2	d2	g2	f2
5	n.c.	n.c.	n.c.	n.c.
6	e3	d3	g3	f3
7	n.c.	n.c.	n.c.	n.c.
8	e4	d4	g4	f4
9	n.c.	n.c.	n.c.	n.c.
10	e5	d5	g5	f5
11	n.c.	n.c.	n.c.	n.c.
12	e6	d6	g6	f6
13	n.c.	n.c.	n.c.	n.c.
14	e7	d7	g7	f7
15	n.c.	n.c.	n.c.	n.c.
16	e8	d8	g8	f8
17	n.c.	n.c.	n.c.	n.c.
18	n.c.	n.c.	n.c.	n.c.
19	e9	d9	g9	f9
20	e10	d10	g10	f10
21	n.c.	n.c.	n.c.	n.c.
22	n.c.	n.c.	n.c.	n.c.
23	e11	d11	g11	f11
24	n.c.	n.c.	n.c.	n.c.
25	e12	d12	g12	f12
26	n.c.	n.c.	n.c.	n.c.
27	e13	d13	g13	f13
28	n.c.	n.c.	n.c.	n.c.
29	e14	d14	g14	f14
30	n.c.	n.c.	n.c.	n.c.
31	e15	d15	g15	f15
32	e16	d16	g16	f16
33	n.c.	comm 2	n.c.	n.c.
34	n.c.	comm 2	n.c.	n.c.

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections (see note) V_{max} 15 V RMS

Note: maximum DC component = 0.1 V

Liquid crystal display LTD234

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	Low temperature storage T_{amb}/duration	High temperature storage T_{amb}/duration (dry)
LTD234R–21	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD235
Liquid crystal display

DEVICE DESCRIPTION

The LTD235 is a 4-digit 7 segment multi-function LCD. The pointers are intended to be used with printed fixed text around the viewing area, i.e. not as a part of the LCD, allowing the display to be used in different languages. For applications which require a 12 o'clock viewing angle the LCD can be used upside down.

QUICK REFERENCE DATA

Viewing area dimensions	45.8 x 17.8 mm
Overall glass dimensions	50.8 x 30.4 mm
Thickness	2.7 +/– 0.4 mm
Digit height	12 mm
Preferred viewing direction	6 o'clock
Driving method	MUX 1:3

DISPLAY MODE

scale 1:1

Fig.1 Universal display.

TYPE DEPENDENT CHARACTERISTICS (1)

TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY CHARACTERISTICS (2)	OPERATING VOLTAGE (V)
LTD235R–12	reflective	with fixed pin	commercial	TR1	typ. 2.8

Note: (1) drive method = MUX 1:3
(2) see chapter "Family characteristics" for complete specification

Liquid crystal display LTD235

MECHANICAL DATA

Dimensions in mm

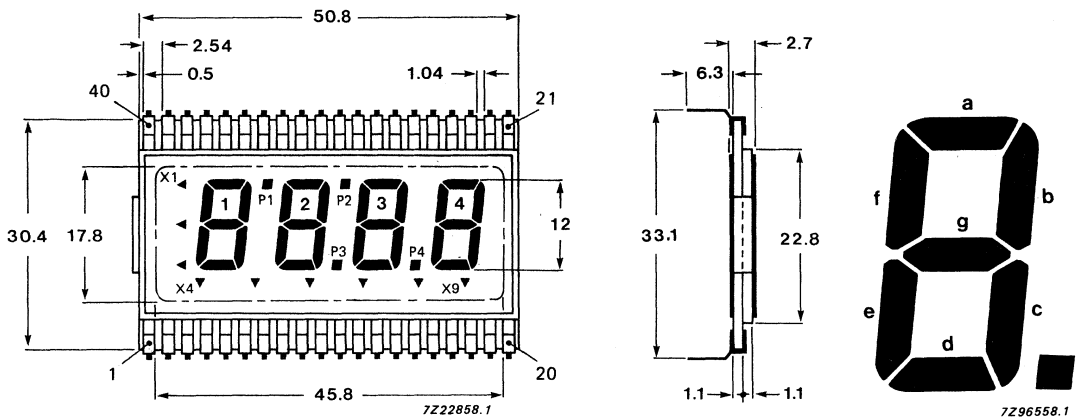


Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT ASSIGNED TO COMMON 1	SEGMENT ASSIGNED TO COMMON 2	SEGMENT ASSIGNED TO COMMON 3
1	comm 1	–	-
2	n.c.	n.c.	n.c.
3	n.c.	n.c.	n.c.
4	e1	x4	f1
5	n.c.	n.c.	n.c.
6	c1	x5	b1
7	n.c.	n.c.	n.c.
8	n.c.	n.c.	n.c.
9	c2	x6	b2
10	n.c.	n.c.	n.c.
11	n.c.	n.c.	n.c.
12	e3	x7	f3
13	n.c.	n.c.	n.c.
14	c3	p4	b3
15	e4	x8	f4
16	n.c.	n.c.	n.c.
17	n.c.	n.c.	n.c.
18	c4	x9	b4
19	n.c.	n.c.	n.c.
20	–	comm 2	-
21	n.c.	n.c.	n.c.
22	n.c.	n.c.	n.c.
23	g4	d4	a4
24	n.c.	n.c.	n.c.
25	n.c.	n.c.	n.c.
26	n.c.	n.c.	n.c.
27	g3	d3	a3
28	n.c.	n.c.	n.c.
29	p3	–	p2
30	n.c.	n.c.	n.c.
31	g2	d2	a2
32	e2	–	f2
33	n.c.	n.c.	n.c.
34	–	–	p1
35	n.c.	n.c.	n.c.
36	g1	d1	a1
37	n.c.	n.c.	n.c.
38	x2	x3	x1
39	n.c.	n.c.	n.c.
40	–	–	comm 3

Liquid crystal display LTD235

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections (see note)	V_{max}	10 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	**Low temperature storage T_{amb}/duration**	**High temperature storage T_{amb}/duration (dry)**
LTD235R–12	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD241
Liquid crystal display

DEVICE DESCRIPTION

The LTD241 is a 3 1/2-digit, 7-segment multi-function LCD with additional indicators. Typical applications include multimeters, panelmeters and industrial instruments requiring a large display.

QUICK REFERENCE DATA

Viewing area dimensions	65.8 x 26.0 mm
Overall glass dimensions	69.8 x 38.0 mm
Thickness	2.7 +/– 0.4 mm
Digit height	17.8 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive

DISPLAY MODE

scale 1:1

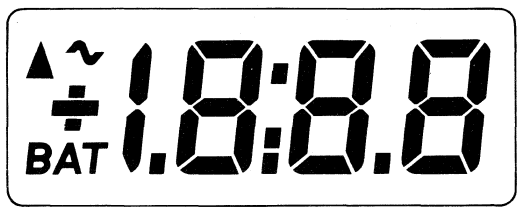


Fig.1 Multimeter display.

TYPE DEPENDENT CHARACTERISTICS (1)

TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY (2) CHARACTERISTICS	OPERATING VOLTAGE (V)
LTD241R–12	reflective	with fixed pins	commercial	TR0	3.5 – 6.5
LTD241R–22	reflective	with fixed pins	extended	TR2	3.5 – 6.5
LTD241F–22	transflective	with fixed pins	extended	TF2	3.5 – 6.5

Note: (1) drive method = direct drive for all types
(2) see chapter "Family Characteristics" for complete specification

Liquid crystal display LTD241

MECHANICAL DATA

Dimensions in mm

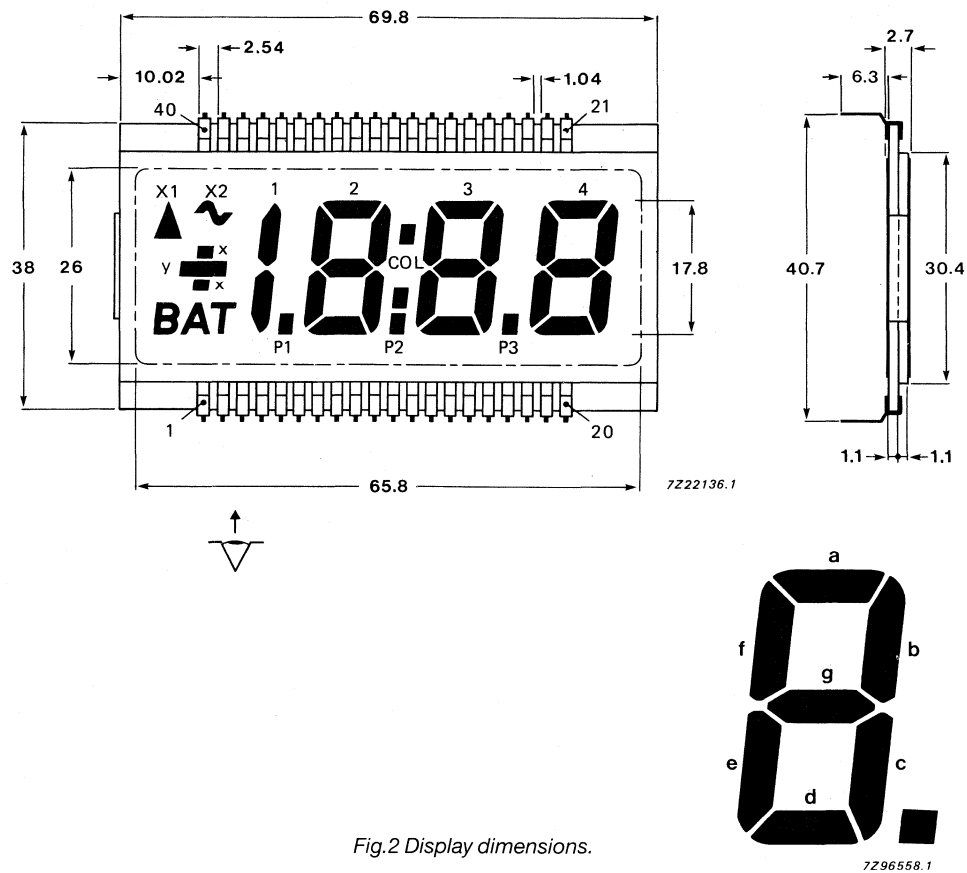


Fig.2 Display dimensions.

Liquid crystal display LTD241

PIN DESCRIPTION

PIN NO.	SEGMENT
1	comm
2	y
3	1
4	n.c.
5	n.c.
6	n.c.
7	n.c.
8	p1
9	e2
10	d2
11	c2
12	p2
13	e3
14	d3
15	c3
16	p3
17	e4
18	d4
19	c4
20	b4

PIN NO.	SEGMENT
21	a4
22	f4
23	g4
24	b3
25	a3
26	f3
27	g3
28	col
29	b2
30	a2
31	f2
32	g2
33	n.c.
34	n.c.
35	n.c.
36	n.c.
37	x2
38	x1
39	x
40	BAT

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two contacts (see note) V_{max} 15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	Low temperature storage T_{amb}/duration	High temperature storage T_{amb}/duration (dry)
LTD241R–12	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days
LTD241R–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days
LTD241F–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD242
Liquid crystal display

DEVICE DESCRIPTION

The LTD242 is a 4-digit, 7-segment multi-function LCD. Typical applications include 24 hr. clocks, counters and industrial instruments requiring a large display.

QUICK REFERENCE DATA

Viewing area dimensions	65.8 x 26.0 mm
Overall glass dimensions	69.8 x 38.0 mm
Thickness	2.7 +/– 0.4 mm
Digit height	17.8 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive

DISPLAY MODE

scale 1:1

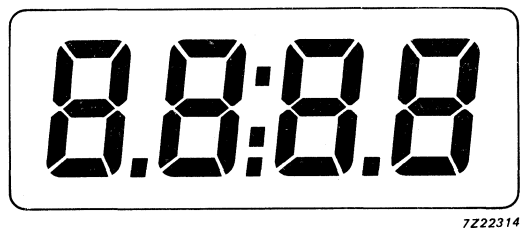


Fig.1 Multimeter display.

TYPE DEPENDENT CHARACTERISTICS (1)

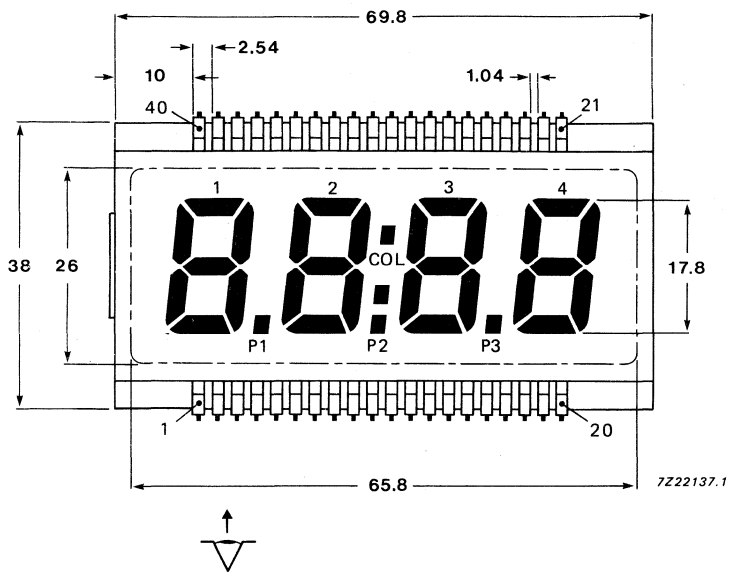
TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY (2) CHARACTERISTICS	OPERATING VOLTAGE (V)
LTD242R–12	reflective	with fixed pins	commercial	TR0	3.5 – 6.5
LTD242R–22	reflective	with fixed pins	extended	TR2	3.5 – 6.5
LTD242F–22	transflective	with fixed pins	extended	TF2	3.5 – 6.5

Note: (1) drive method = direct drive for all types
(2) see chapter "Family Characteristics" for complete specification

Liquid crystal display LTD242

MECHANICAL DATA

Dimensions in mm



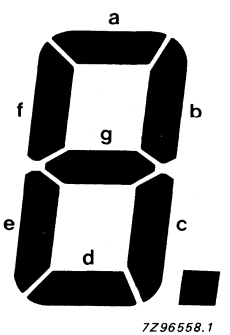


Fig.2 Display dimensions.

Liquid crystal display LTD242

PIN DESCRIPTION

PIN NO.	SEGMENT
1	comm
2	n.c.
3	n.c.
4	n.c.
5	e1
6	d1
7	c1
8	p1
9	e2
10	d2
11	c2
12	p2
13	e3
14	d3
15	c3
16	p3
17	e4
18	d4
19	c4
20	b4

PIN NO.	SEGMENT
21	a4
22	f4
23	g4
24	b3
25	a3
26	f3
27	g3
28	col
29	b2
30	a2
31	f2
32	g2
33	nc
34	b1
35	a1
36	f1
37	g1
38	n.c.
39	n.c.
40	n.c.

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two contacts (see note) V_{max} 15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	Low temperature storage T_{amb}/duration	High temperature storage T_{amb}/duration (dry)
LTD242R–12	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days
LTD242R–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days
LTD242F–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD261
Liquid crystal display

DEVICE DESCRIPTION

The LTD261 is a 1-digit, 7-segment multi-function LCD. It can be combined to form large clock displays and displays requiring a wide viewing distance.

QUICK REFERENCE DATA

Viewing area dimensions	71.2 x 89.0 mm
Overall glass dimensions	76.2 x 101.6 mm
Thickness	2.7 +/– 0.4 mm
Digit height	76.0 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive

DISPLAY MODE

scale 1:1

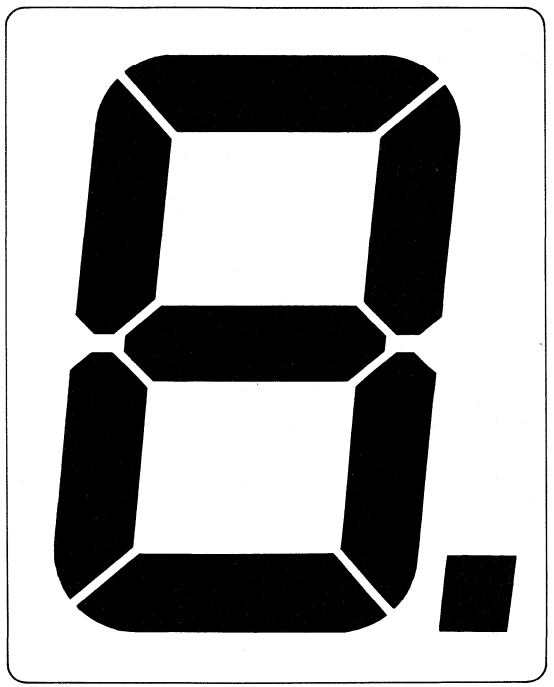


Fig.1 Universal display.

Liquid crystal display LTD261

MECHANICAL DATA

Dimensions in mm

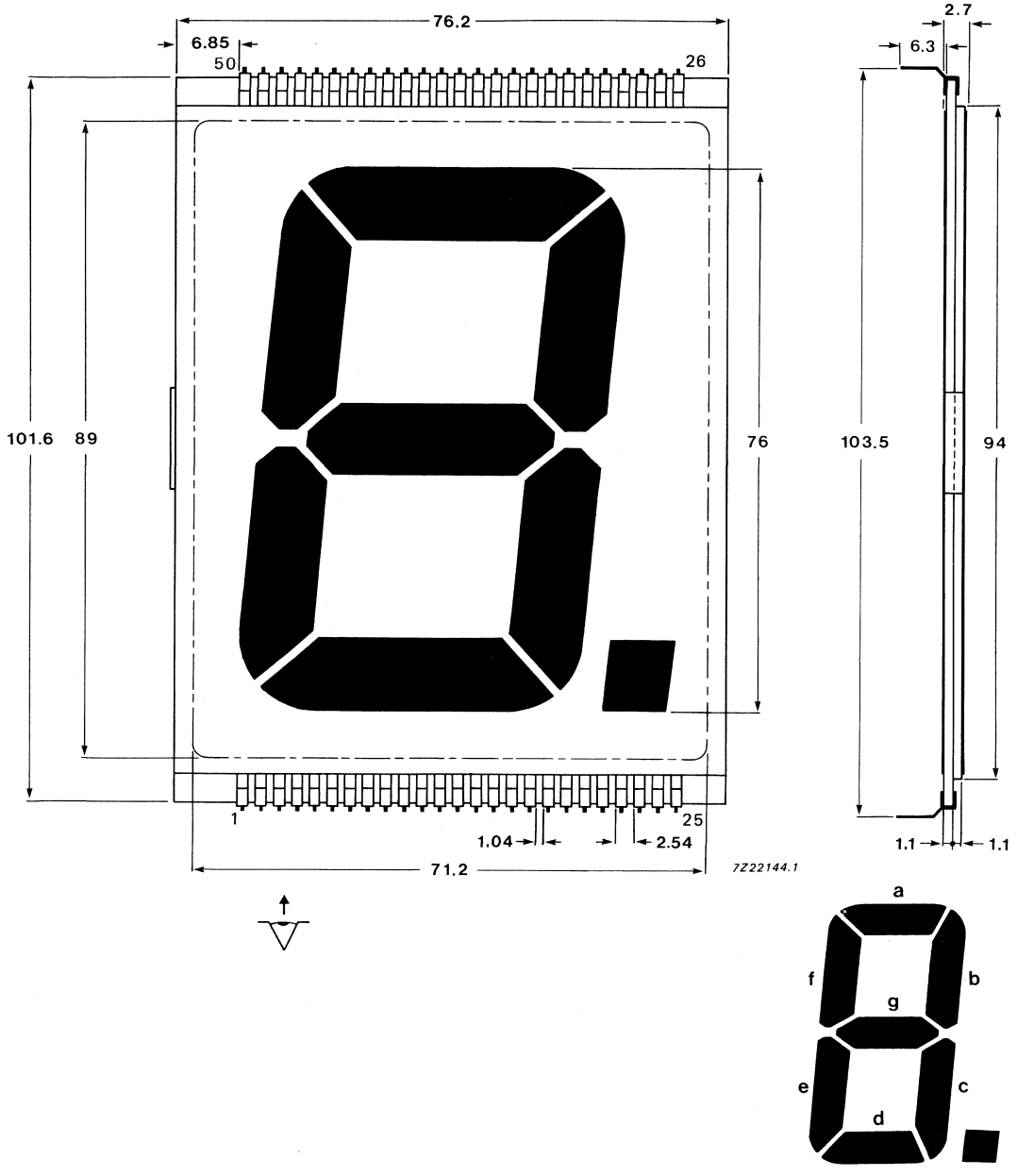


Fig.2 Display dimensions.

Liquid crystal display LTD261

TYPE DEPENDENT CHARACTERISTICS (1)

TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY (2) CHARACTERISTICS	OPERATING VOLTAGE (V)
LTD261R–12	reflective	with fixed pins	commercial	TR0	3.5 – 6.5
LTD261R–22	reflective	with fixed pins	extended	TR2	3.5 – 6.5
LTD261F–22	transflective	with fixed pins	extended	TF2	3.5 – 6.5

Note: (1) drive method = direct drive for all types
(2) see chapter "Family Characteristics" for complete specification

PIN DESCRIPTION

PIN NO.	SEGMENT
1–5	comm
6–10	e
11–15	d
16–20	c
21–25	p1

PIN NO.	SEGMENT
26–30	g
31–35	b
36–40	n.c.
41–45	a
46–50	f

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)
Maximum voltage between any two contacts (see note) V_{max} 15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	Low temperature storage T_{amb}/duration	High temperature storage T_{amb}/duration (dry)
LTD261R–12	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days
LTD261R–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days
LTD261F–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD262
Liquid crystal display

DEVICE DESCRIPTION

The LTD262 is an 8-digit, 7-segment multi-function LCD. Typical applications include timers, counters, and instruments requiring a large display.

QUICK REFERENCE DATA

Viewing area dimensions	89.8 x 18.4 mm
Overall glass dimensions	93.8 x 30.4 mm
Thickness	2.7 +/– 0.4 mm
Digit height	12.7 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive

DISPLAY MODE

scale 1:1

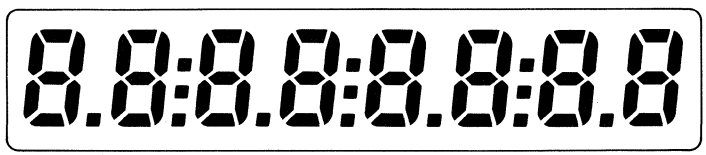


Fig.1 Universal display.

TYPE DEPENDENT CHARACTERISTICS (1)

TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY (2) CHARACTERISTICS	OPERATING VOLTAGE (V)
LTD262R–12	reflective	with fixed pins	commercial	TR0	3.5 – 6.5
LTD262R–22	reflective	with fixed pins	extended	TR2	3.5 – 6.5
LTD262F–22	transflective	with fixed pins	extended	TF2	3.5 – 6.5

Note: (1) drive method = direct drive for all types
(2) see chapter "Family Characteristics" for complete specification

MECHANICAL DATA

Dimensions in mm

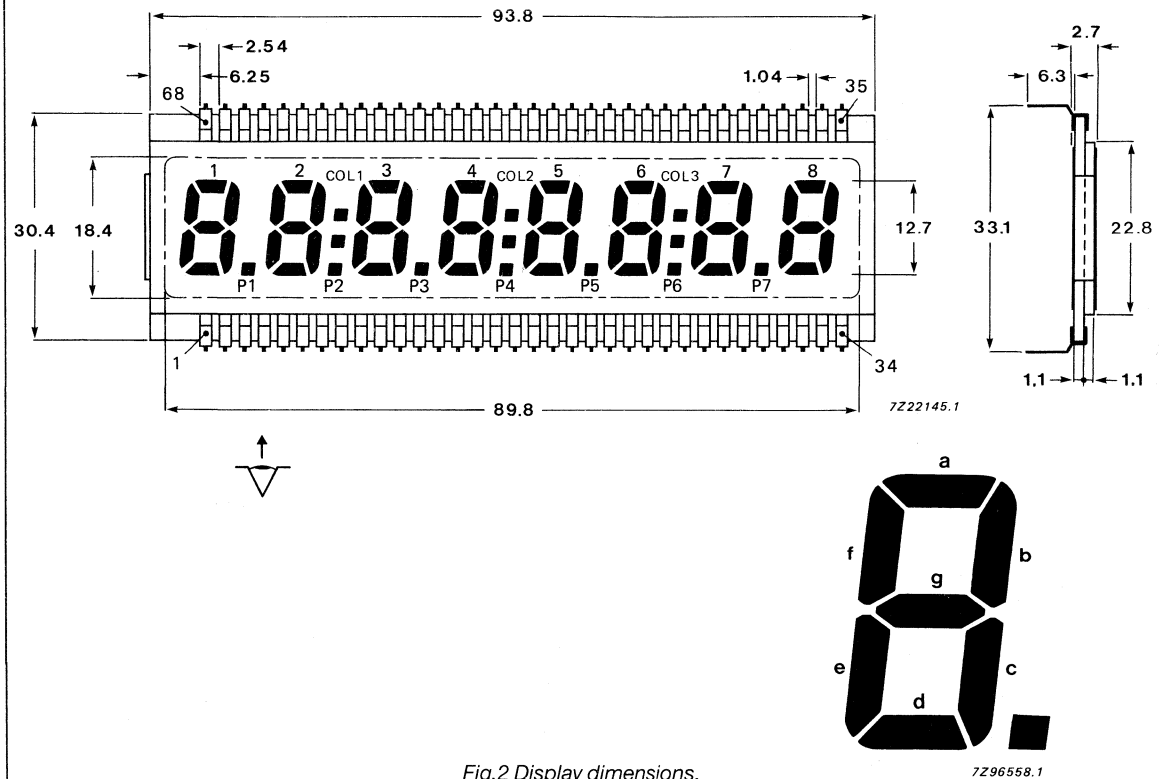


Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT	PIN NO.	SEGMENT
1	comm	35	a8
2	e1	36	f8
3	d1	37	g8
4	c1	38	b7
5	p1	39	a7
6	e2	40	f7
7	d2	41	g7
8	c2	42	col3
9	p2	43	b6
10	n.c.	44	a6
11	e3	45	f6
12	d3	46	g6
13	c3	47	b5
14	p3	48	a5
15	e4	49	f5
16	d4	50	g5
17	c4	51	col2
18	p4	52	b4
19	e5	53	a4
20	d5	54	f4
21	c5	55	g4
22	p5	56	b3
23	e6	57	a3
24	d6	58	f3
25	c6	59	g3
26	p6	60	col1
27	e7	61	b2
28	d7	62	a2
29	c7	63	f2
30	p7	64	g2
31	e8	65	b1
32	d8	66	a1
33	c8	67	f1
34	b8	68	g1

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two contacts (see note)	V_{max}	15 V RMS

Note: maximum DC component = 0.1 V

Liquid crystal display LTD262

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	**Low temperature storage T_{amb}/duration**	**High temperature storage T_{amb}/duration (dry)**
LTD262R–12	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days
LTD262R–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days
LTD262F–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD263
Liquid crystal display

DEVICE DESCRIPTION

The LTD263 is a 6-digit, 7-segment multi-function LCD. Typical applications include 24 hr. clocks with a seconds display, counters, and industrial instruments requiring a large display.

QUICK REFERENCE DATA

Viewing area dimensions	88.8 x 25.4 mm
Overall glass dimensions	93.8 x 38.0 mm
Thickness	2.7 +/– 0.4 mm
Digit height	17.8 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive

DISPLAY MODE

scale 1:1

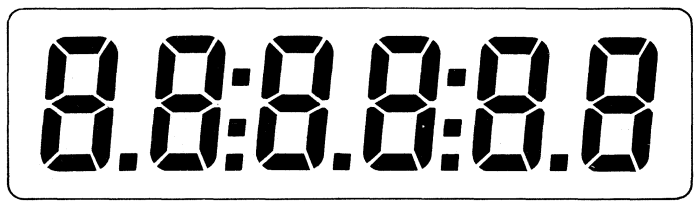


Fig.1 Universal display.

TYPE DEPENDENT CHARACTERISTICS (1)

TYPE	ILLUNINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY (2) CHARACTERISTICS	OPERATING VOLTAGE (V)
LTD263R–12	reflective	with fixed pins	commercial	TR0	3.5 – 6.5
LTD263R–22	reflective	with fixed pins	extended	TR2	3.5 – 6.5

Note: (1) drive method = direct drive for all types
(2) see chapter"Family Characteristics" for complete specification

Liquid crystal display LTD263

MECHANICAL DATA

Dimensions in mm

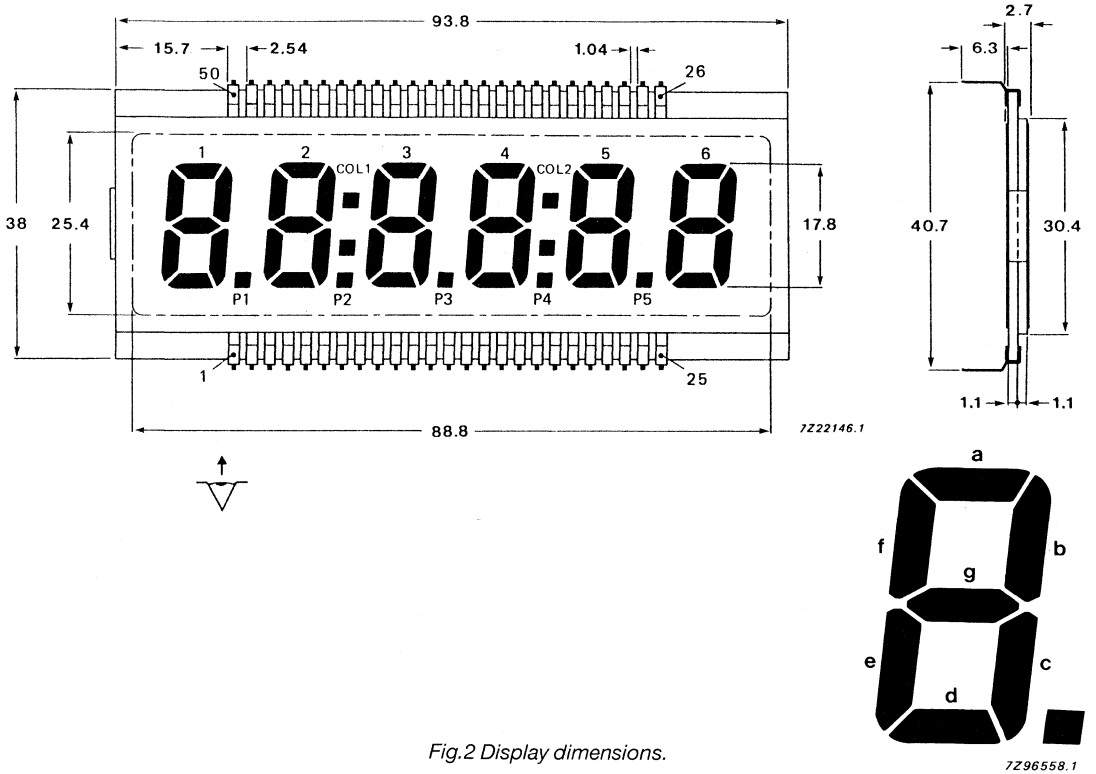


Fig.2 Display dimensions.

Liquid crystal display LTD263

PIN DESCRIPTION

PIN NO.	SEGMENT	PIN NO.	SEGMENT
1	comm	26	a1
2	e6	27	f1
3	d6	28	g1
4	c6	29	b2
5	p1	30	a2
6	e5	31	f2
7	d5	32	g2
8	c5	33	col2
9	p2	34	b3
10	e4	35	a3
11	d4	36	f3
12	c4	37	g3
13	p3	38	b4
14	e3	39	a4
15	d3	40	f4
16	c3	41	g4
17	p4	42	col1
18	e2	43	b5
19	d2	44	a5
20	c2	45	f5
21	p5	46	g5
22	e1	47	b6
23	d1	48	a6
24	c1	49	f6
25	b1	50	g6

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two contacts (see note) V_{max} 15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	Low temperature storage T_{amb}/duration	High temperature storage T_{amb}/duration (dry)
LTD263R–12	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days
LTD263R–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD264
Liquid crystal display

DEVICE DESCRIPTION

The LTD264 is a 5-digit, 7-segment point of sales display.

QUICK REFERENCE DATA

Viewing area dimensions	109.0 x 33.4 mm
Overall glass dimensions	114.0 x 46.0 mm
Thickness	2.7 +/– 0.4 mm
Digit height	25.0 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive

DISPLAY MODE

scale 1:1

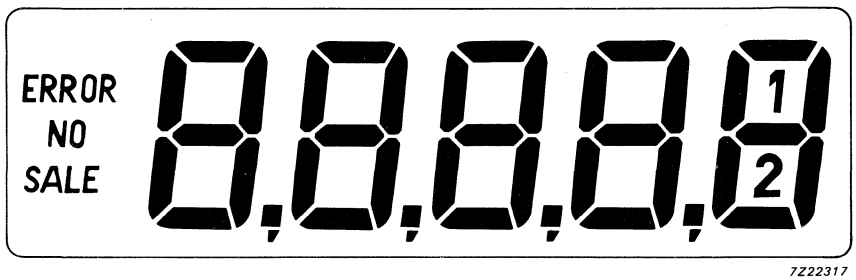


Fig. 1 Till display.

TYPE DEPENDENT CHARACTERISTICS (1)

TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY (2) CHARACTERISTICS	OPERATING VOLTAGE (V)
LTD264R–22	reflective	with fixed pins	extended	TR2	3.5 – 6.5
LTD264F–22	transflective	with fixed pins	extended	TF2	3.5 – 6.5

Note: (1) drive method = direct drive for all types
(2) see chapter "Family Characteristics" for complete specification

Liquid crystal display LTD264

MECHANICAL DATA

Dimensions in mm

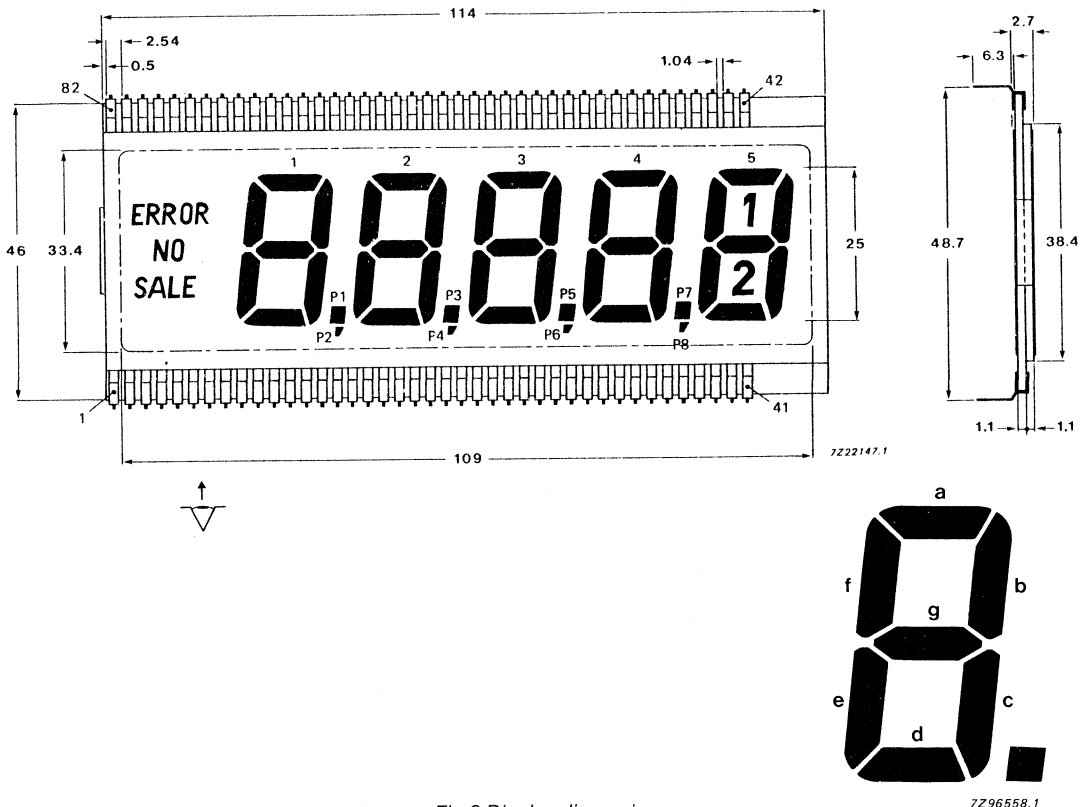


Fig.2 Display dimensions.

Liquid crystal display LTD264

PIN DESCRIPTION

PIN NO.	SEGMENT
1	comm
2	comm
3	comm
4	no sale
5	n.c.
6	n.c.
7	e1
8	d1
9	c1
10	n.c.
11	n.c.
12	n.c.
13	p1
14	p2
15	n.c.
16	n.c.
17	e2
18	d2
19	c2
20	n.c.
21	p3
22	p4
23	n.c.
24	e3
25	d3
26	c3
27	n.c.
28	p5
29	p6
30	n.c.
31	e4
32	d4
33	c4
34	n.c.
35	p7
36	p8
37	n.c.
38	e5
39	d5
40	2
41	c5

PIN NO.	SEGMENT
42	b5
43	1
44	a5
45	f5
46	g5
47	b4
48	af
49	f4
50	g4
51	n.c.
52	n.c.
53	n.c.
54	b3
55	a3
56	f3
57	g3
58	n.c.
59	n.c.
60	n.c.
61	b2
62	a2
63	f2
64	g2
65	n.c.
66	n.c.
67	n.c.
68	n.c.
69	n.c.
70	b1
71	a1
72	f1
73	g1
74	n.c.
75	n.c.
76	n.c.
77	n.c.
78	n.c.
79	error
80	n.c.
81	n.c.
82	n.c.

Liquid crystal display LTD264

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two contacts (see note)	V_{max}	15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	**Low temperature storage T_{amb}/duration**	**High temperature storage T_{amb}/duration (dry)**
LTD264R–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days
LTD264F–22	+80 °C/90%/21 days	–40 °C/21 days	+85 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD321
Liquid Crystal Display

DEVICE DESCRIPTION

The LTD321 is a bargraph display. Typical applications include panelmeters and general purpose bargraphs.

QUICK REFERENCE DATA

Viewing area dimensions	64.8 x 17.8 mm
Overall glass dimensions	69.8 x 30.4 mm
Thickness	2.7 +/– 0.4 mm
Digit height	5.0 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive

DISPLAY MODE

scale 1:1

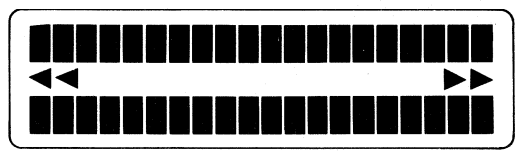


Fig.1 Universal bargraph display.

TYPE DEPENDENT CHARACTERISTICS (1)

TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY (2) CHARACTERISTICS	OPERATING VOLTAGE (V)
LTD321R–12	reflective	with fixed pins	commercial	TR0	3.5 – 6.5

Note: (1) drive method = direct drive
(2) see chapter "Family Characterstics" for complete specification

Liquid crystal display LTD321

MECHANICAL DATA

Dimensions in mm

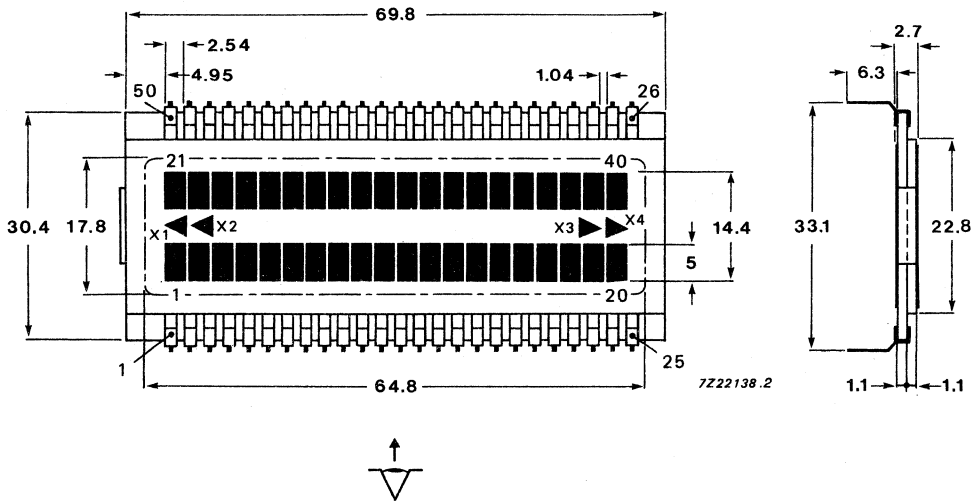


Fig.2 Display dimensions.

Liquid crystal display LTD321

PIN DESCRIPTION

PIN NO.	SEGMENT ASSIGNED TO COMMON 1	PIN NO.	SEGMENT ASSIGNED TO COMMON 2
1	comm 1	26	n.c.
2	1	27	n.c.
3	2	28	x4
4	3	29	x3
5	4	30	40
6	5	31	39
7	6	32	38
8	7	33	37
9	8	34	36
10	9	35	35
11	10	36	34
12	11	37	33
13	12	38	32
14	13	39	31
15	14	40	30
16	15	41	29
17	16	42	28
18	17	43	27
19	18	44	26
20	19	45	25
21	20	46	24
22	x1	47	23
23	x2	48	22
24	n.c.	49	21
25	n.c.	50	comm 2

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections (see note)	V_{max}	15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	Low temperature storage T_{amb}/duration	High temperature storage T_{amb}/duration (dry)
LTD321R–12	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTD351
Liquid Crystal Display

DEVICE DESCRIPTION

The LTD351 is a bargraph display. Typical applications include panelmeters and general purpose bargraph displays. For applications requiring a 9 o'clock viewing angle, the LCD can be used upside down.

QUICK REFERENCE DATA

Viewing area dimensions	109.0 x 16.0 mm
Overall glass dimensions	114.0 x 26.0 mm
Thickness	2.7 +/– 0.4 mm
Digit height	5.0 mm
Preferred viewing direction	3 o'clock
Driving method	MUX 1:2

DISPLAY MODE

scale 1:1

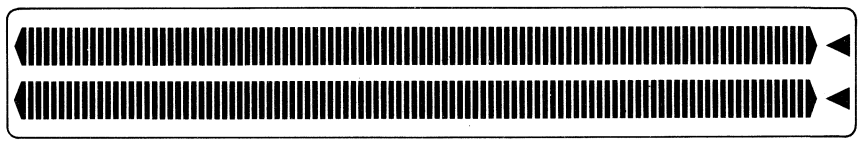


Fig.1 Universal bargraph display.

TYPE DEPENDENT CHARACTERISTICS (1)

TYPE	ILLUMINATION MODE	CONNECTION METHOD	RELIABILITY GRADE	FAMILY CHARACTERISTICS (2)	OPERATING VOLTAGE (V)
LTD351R–11	reflective	with fixed pins	commercial	TR1	typ. 2.6

Note: (1) drive method = MUX 1:2
(2) see chapter "Family Characteristics" for complete specification

Liquid crystal display

LTD351

MECHANICAL DATA

Dimensions in mm

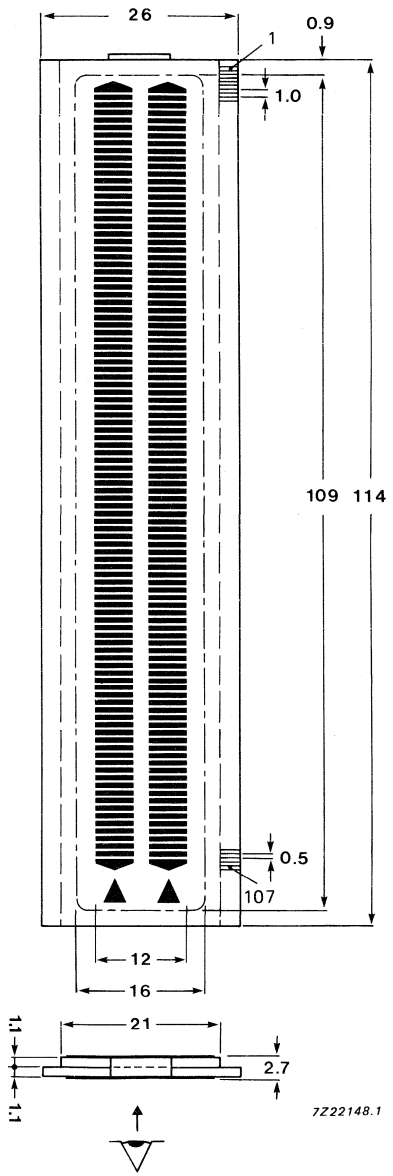


Fig.2 Display dimensions.

Liquid crystal display LTD351

PIN DESCRIPTION

PIN NO.	SEGMENT ASSIGNED TO COMMON 1
1	comm 1
2	n.c.
3	n.c.
4	x1
.	.
.	.
.	.
107	x104

PIN NO.	SEGMENT ASSIGNED TO COMMON 2
1	n.c.
2	comm 2
3	comm 2
4	y1
.	.
.	.
.	.
107	y104

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections (see note) V_{max} 15 V RMS

Note: maximum DC component = 0.1 V

TYPE	RELIABILITY TESTS		
	Damp heat steady state T_{amb}/R.H./duration	Low temperature storage T_{amb}/duration	High temperature storage T_{amb}/duration (dry)
LTD351R–11	+40 °C/90%/21 days	–25 °C/21 days	+70 °C/21 days

LCD modules

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTM233
Liquid crystal display

MODULE DESCRIPTION

The LTM233 is a 16-digit, 1-line segment LCD module with a 1:2 multiplex drive ratio. It is driven by two PCF2111 LCD drivers which are contained within the module housing. An external microcomputer can be programmed to supply display data of 16 numeric characters with some alphabetic characters possible.

QUICK REFERENCE DATA

Outline dimensions	92.5 x 25 x 10.5 mm
Viewing area	65.8 x 11.2 mm
Character size	3.2 x 6 mm
Mass	≈ 21 g
Drive method	MUX 1:2
Supply voltage	+2.6 V
Supply current	30 μA
Illumination mode	reflective
Front surface	glossy
Character generator	external
Data interface	serial (C-bus)

DISPLAY MODE

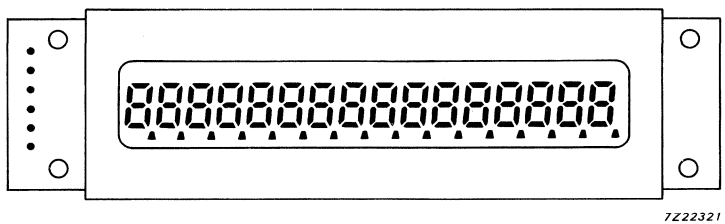


Fig.1 16-digit, universal LCD module.

TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	VIEWING DIRECTION
LTM233R-10	reflective	6 o'clock

Liquid crystal display LTM233

MECHANICAL DATA

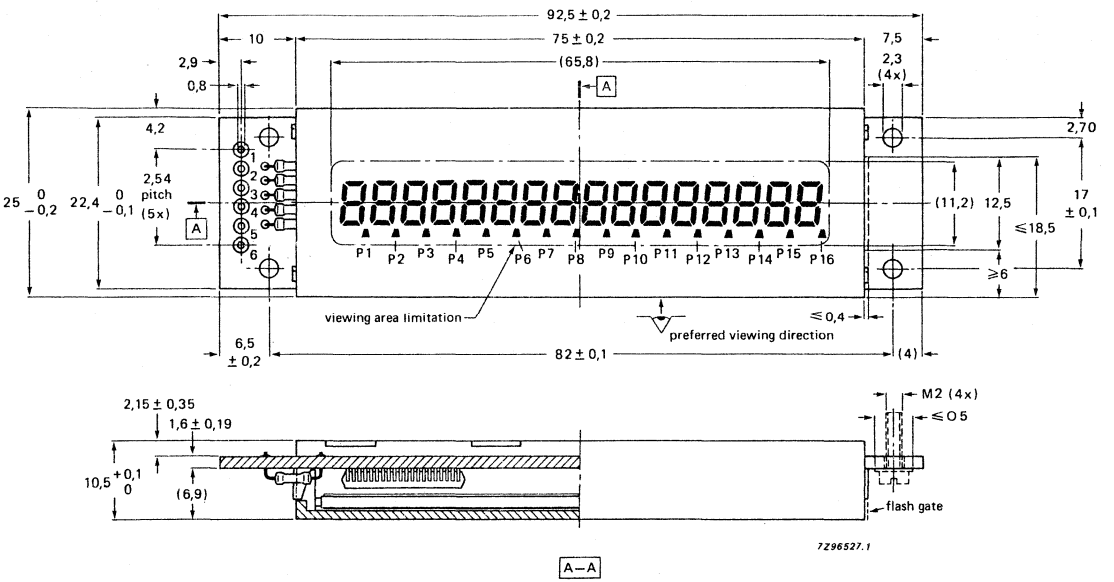


Fig.2 Outline dimensions.

PIN DESCRIPTION

1	2	3	4	5	6
DLEN 1	DATA	DLEN 2	CLB	V_{DD}	GND

Liquid crystal display LTM233

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{DD}	0.3	-	8.0	V
Input voltage on any pin	V_I	0.3	-	V_{DD}+0.3	V
Storage temperature	T_{stg}	25	-	+60	°C
Operating ambient temperature	T_{amb}	10	-	+55	°C

OPERATING CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating voltage	V_{DD}	-	2.6	-	V
LOW level input voltage	V_{IL}	0.3	-	0.6	V
HIGH level input voltage	V_{IH}	2.2	-	V_{DD}	V

TIMING CHARACTERISTICS

T_{amb} = 0 to 50 °C, V_{DD} = 5 V +/- 5%, unless otherwise specified.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
CLB pulse width HIGH	t_{WH}	3	-	-	µs
CLB pulse width LOW	t_{WL}	10	-	-	µs
Data set-up time DATA to CLB	t_{SUDA}	10	-	-	µs
Data hold time DATA to CLB	t_{HDDA}	10	-	-	µs
Enable set-up time DLEN to CLB	t_{SUEN}	3	-	-	µs
Disable set-up time CLB to DLEN	t_{SUDI}	10	-	-	µs
Set-up time load pulse DLEN to CLB	t_{SULD}	10	-	-	µs
Busy-time from load pulse to next start of transmission	t_{BUSY}	10	-	-	µs
Set-up time leading zero DATA to CLB	t_{SULZ}	10	-	-	µs

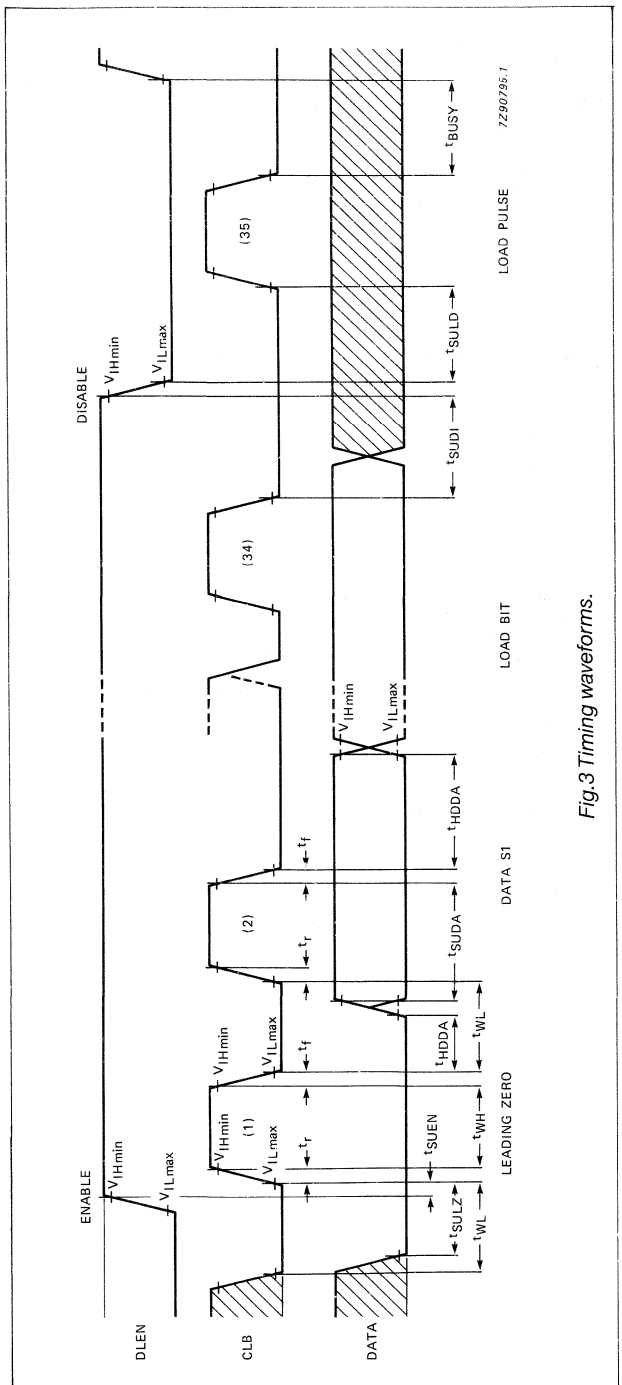


Fig.3 Timing waveforms.

Correspondence between IC-outputs and LCD-segments

Output	IC	S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Segment	BP 1		f	e	p	d	f	e	p	d	f	e	p	d	f	e	p	d	f	e	p	d	f	e	p	d	f	e	p	d	f	e	p	d
	BP 2		a	g	b	c	a	g	b	c	a	g	b	c	a	g	b	c	a	g	b	c	a	g	b	c	a	g	b	c	a	g	b	c
Digit	IC 1		1	1	1	1	2	2	2	2	3	3	3	3	4	4	4	4	5	5	5	5	6	6	6	6	7	7	7	7	8	8	8	8
	IC 2		9	9	9	9	10	10	10	10	11	11	11	11	12	12	12	12	13	13	13	13	14	14	14	14	15	15	15	15	16	16	16	16

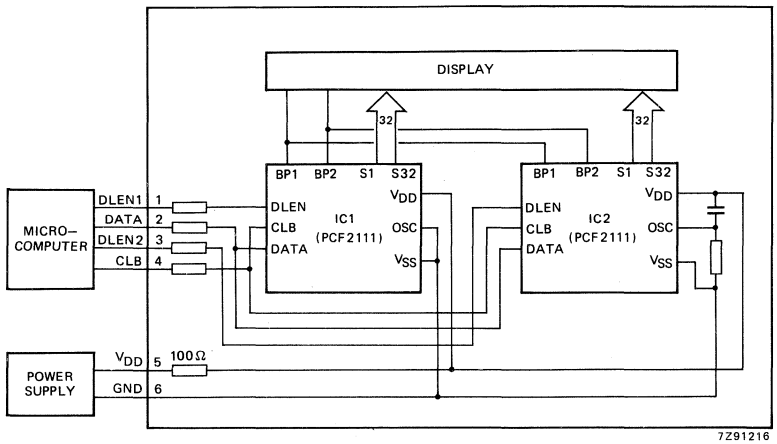


Fig.4 Functional block diagram.

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTN111
Liquid crystal display

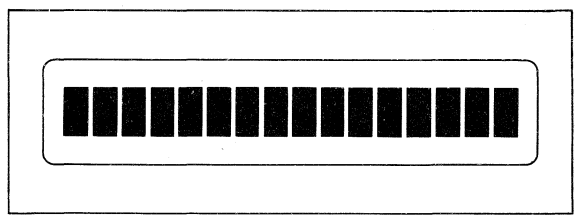
MODULE DESCRIPTION

The LTN111 is a 5 x 7 dot, 16-character, 1-line dot matrix LCD module, with driver and controller LSI IC mounted on a single printed circuit board. The LSI controller incorporates a ROM-based character generator with a 160 characters and RAM display data with 8 characters. The module is capable of generating 160 fixed and 8 write by programme characters. The LTN111 operates from an extensive instruction set: display clear, cursor home, display ON/OFF, cursor ON/OFF, character blink, cursor shift and display shift.

QUICK REFERENCE DATA

Outline dimensions	80 x 36 x 12 mm
Viewing area	64.5 x 13.8 mm
Character format	5 x 7 dots and cursor
Character size	3.07 x 6.56 mm
Dot size (spacing 0.08 mm)	0.55 x 0.75 mm
Mass	≈ 25 g
Drive method	MUX 1:16
Supply voltage	+5 V
Power consumption	7.5 mW
Illumination mode	reflective/trans-flective
Front surface	glossy
Character generator	built in
Data interface	parallel 4 or 8 bits

DISPLAY MODE



7Z22322

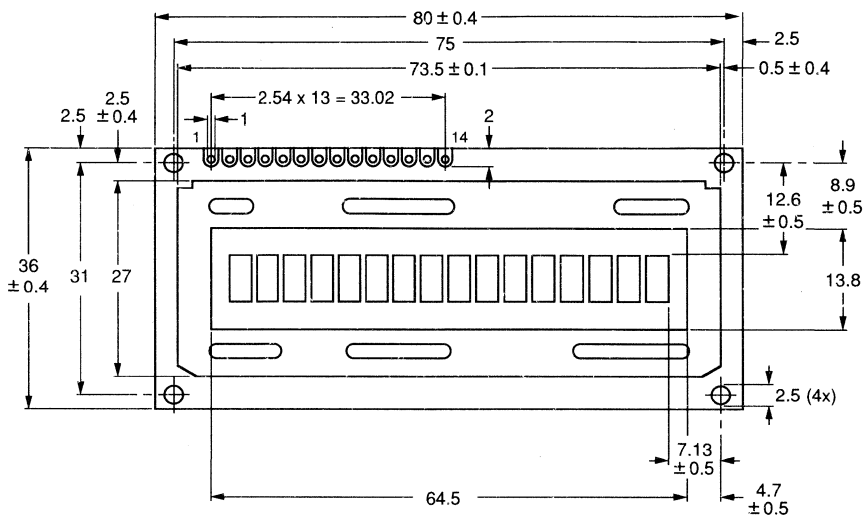
Fig.1 16-character, 1-line LCD module.

TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	VIEWING DIRECTION	TO BE USED WITH EL BACKLIGHT
LTN111R-10	reflective	6 o'clock	–
LTN111F-10	transflective	6 o'clock	LXL111-G
LTN111R-50	reflective	12 o'clock	–
LTN111F-50	transflective	12 o'clock	LXL111-G

Liquid crystal display LTN111

MECHANICAL DATA



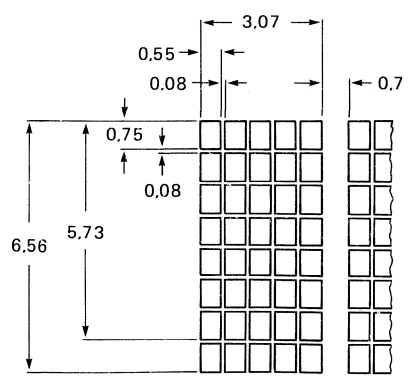


Fig.2 Outline dimensions.

Liquid crystal display LTN111

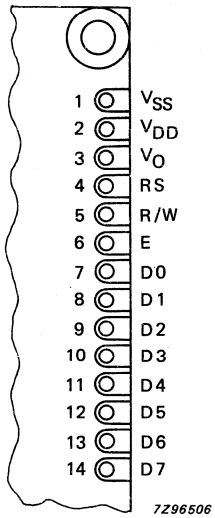


Fig.3 Pin configuration.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	V_{SS}	ground
2	V_{DD}	power supply (logic)
3	V_O	contrast adjustment voltage
4	RS	register select
5	R/W	read/write
6	E	enable
7	D0	I/O data LSB
8	D1	I/O data 2nd bit
9	D2	I/O data 3rd bit
10	D3	I/O data 4th bit
11	D4	I/O data 5th bit
12	D5	I/O data 6th bit
13	D6	I/O data 7th bit
14	D7	I/O data MSB

Notes to pin description

1. Contrast is adjusted by varying the voltage V_O between 0 and 5 V.
2. D7 doubles as busy flag.
3. When the module is interfaced with a microprocessor with 4-bit parallel outputs, pins D0 to D3 are not used.

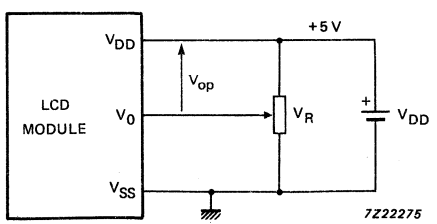


Fig.4 Power supply.

Liquid crystal display LTN111

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{DD}	−0.3	−	7.0	V
LCD drive voltage (V_{DD}-V_O)	V_{op}	0	−	9.0	V
Input voltage	V_I	−0.3	−	V_{DD}+0.3	V
Storage temperature	T_{stg}	−25	−	+70	°C
Operating ambient temperature	T_{amb}	0	−	+50	°C

OPERATING CHARACTERISTICS

T_{amb} = 25 °C; V_{DD} = 5 V; all voltages refer to V_{SS}; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (logic)	V_{DD}-V_{SS}	4.75	5.0	5.25	V
Contrast adjustment voltage	V_O	−	0.6	−	V
Temperature compensation of V_O	TC	−	−14	−	mV/°C
LOW level input voltage	V_{IL}	−0.3	−	0.6	V
HIGH level input voltage	V_{IH}	2.2	−	V_{DD}	V
LOW level output voltage -I_{OL} = 1.2 mA	V_{OL}	−	−	0.4	V
HIGH level output voltage -I_{OH} = 0.205 mA	V_{OH}	2.4	−	−	V
Input leakage current	I_I	−	−	1.0	µA
Internal oscillating frequency	f_{OSC}	−	250	−	kHz
Supply current (logic)	I_{DD}	−	1.5	2.0	mA
Power dissipation	P_d	−	7.5	10.0	mW

TIMING CHARACTERISTICS

T_{amb} = 0 to 50 °C, V_{DD} = 5 V+/− 5%, unless otherwise specified.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Enable cycle time	t_{cyc}	1000	−	−	ns
Enable pulse width	t_W	450	−	−	ns
Rise time	t_r	−	−	25	ns
Fall time	t_f	−	−	25	ns
Register select set-up time	t_{rsu}	140	−	−	ns
Read and write set-up time	t_{su}	140	−	−	ns
Data set-up time	t_{dsu}	195	−	−	ns
Data delay time	t_d	−	−	320	ns
Address hold time	t_{AH}	10	−	−	ns
Data hold time write	t_{WH}	10	−	−	ns
Data hold time read	t_{RH}	20	−	−	ns

ELECTRO-OPTICAL CHARACTERISTICS

T_{amb} = 25 °C, $V_{DD} = V_{DD\ typ}$, α = 10°, $\phi = \phi_o pt$, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	TYP.	MAX.	UNIT
Response times	t_{on}	T_{amb} = 0 °C T_{amb} = 25 °C T_{amb} = 50 °C	380 110 45	760 220 90	ms ms ms
	t_{off}	T_{amb} = 0 °C T_{amb} = 25 °C Tamb = 50 °C	470 110 45	940 220 90	ms ms ms
Viewing Angles (contrast ratio CR > 3)	α_{opt} α_2-α_1	reflective types	30 30	– –	o o
	α_{opt} α_2-α_1	transflective types reflective operation	30 25	– –	o o
	α_2-α_1	transflective types transmissive operation	30 20	– –	o o

For definitions of response times, viewing angles and contrast ratio refer to notes 1 to 3

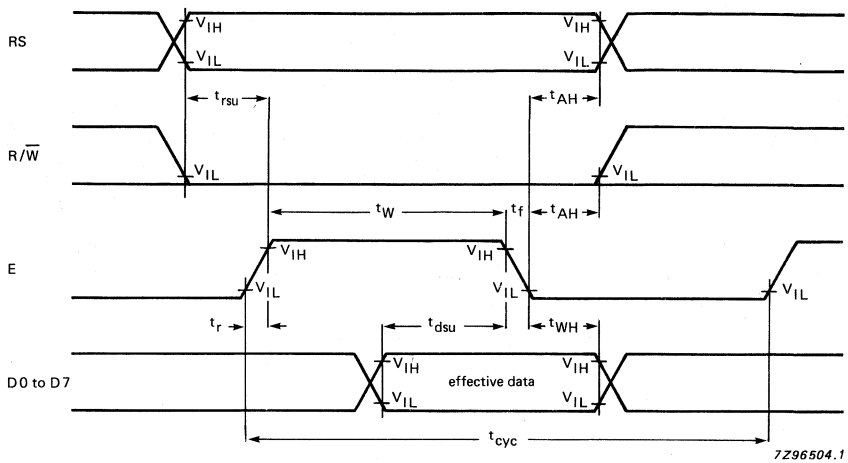


Fig.5 Timing waveforms (write operation).

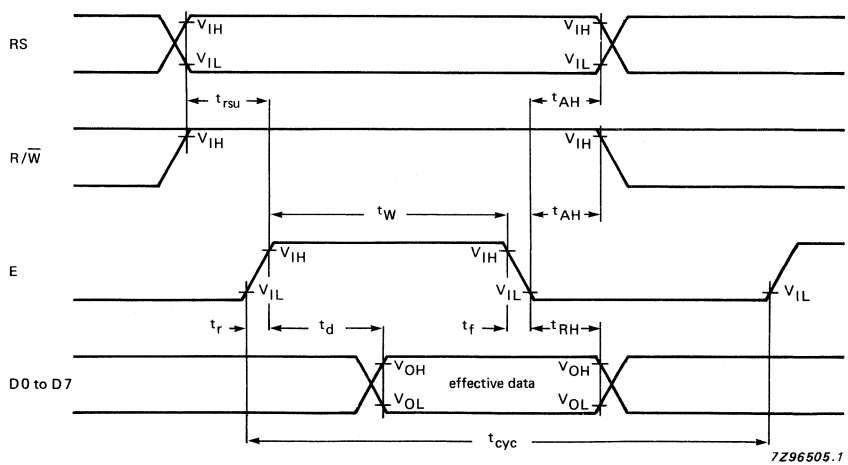


Fig.6 Timing waveforms (read operation).

Table 1 Instruction set

INSTRUCTION \ ADDRESSES	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Display clear	0	0	0	0	0	0	0	0	0	1
Cursor home	0	0	0	0	0	0	0	0	1	*
Entry mode set	0	0	0	0	0	0	0	1	I/D	S
Display on/off control	0	0	0	0	0	0	1	D	C	B
Cursor display shift	0	0	0	0	0	1	S/C	R/L	*	*
Function set	0	0	0	0	1	DL	1	0	*	*
CG RAM address set	0	0	0	1	A_{CG}					
DD RAM address set	0	0	1	A_{DD}						
Busy flag/address read	0	1	BF	AC						
CG RAM/DD RAM data write	1	0	write data							
CG RAM/DD RAM data read	1	1	read data							

Notes:

I/D	= 1:increment	I/D	= 0:decrement
S	= 1:display shift	S	= 0:display freeze
D	= 1:display on	D	= 0:display off
C	= 1:cursor on	C	= 0:cursor off
B	= 1:character at cursor position blinks	B	= 0:character at cursor position does not blink
S/C	= 1:display shift	S/C	= 0:cursor move
R/L	= 1:right shift	R/L	= 0:left shift
DL	= 1:8 bits	DL	= 0:4 bits
BF	= 1:during internal operation	BF	= 0:end of internal operation

Table 2 Display position and DD RAM address (HEX)

Digit

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
00_H	01_H	02_H	03_H	04_H	05_H	06_H	07_H	40_H	41_H	42_H	43_H	44_H	45_H	46_H	47_H

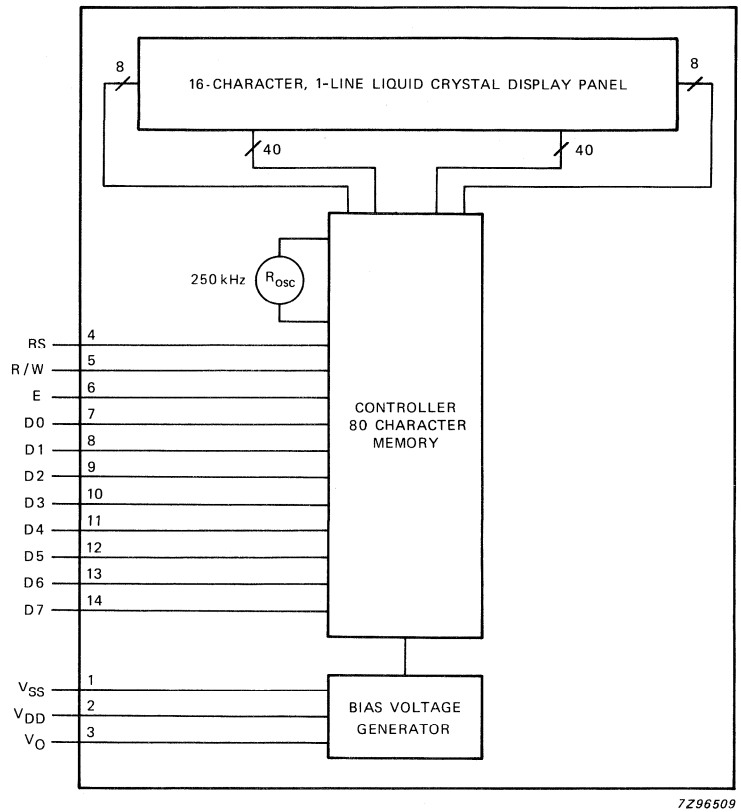
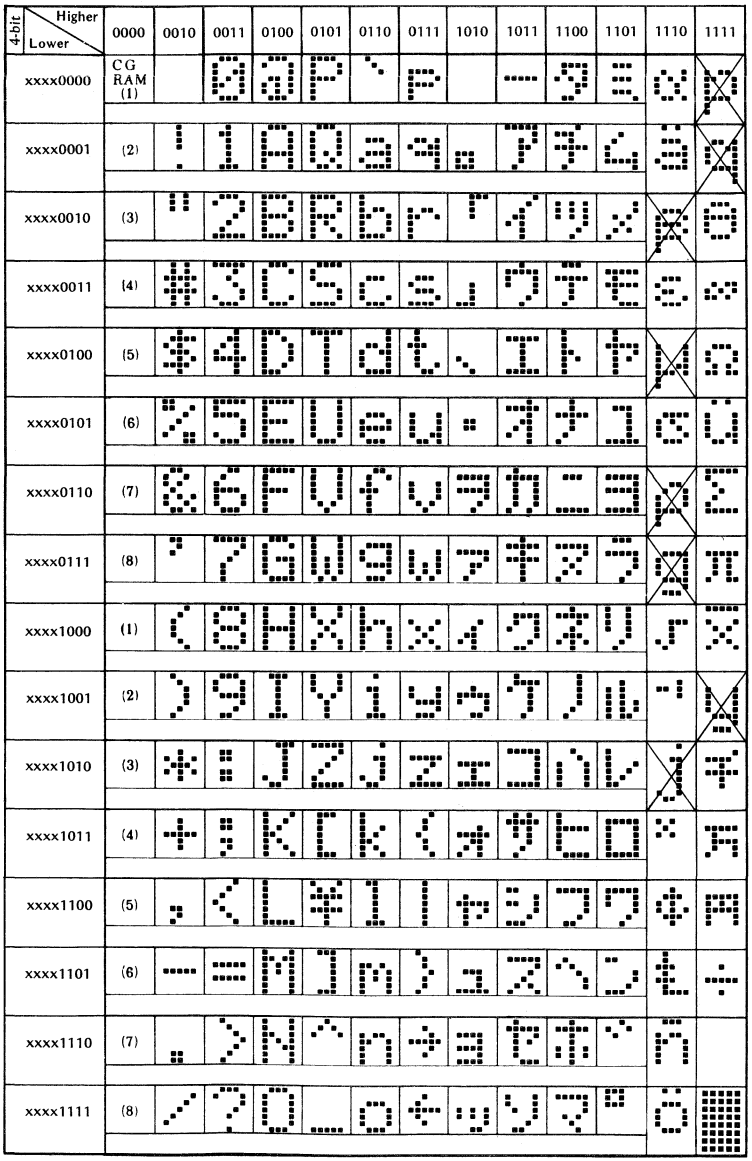


Fig.7 Functional block diagram.

Table 3 Input codes vs character pattern



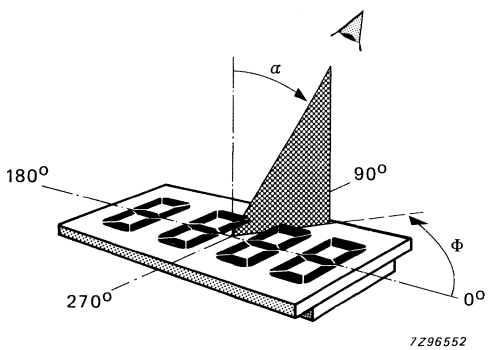
Note 1 Definition of contrast ratio (CR).

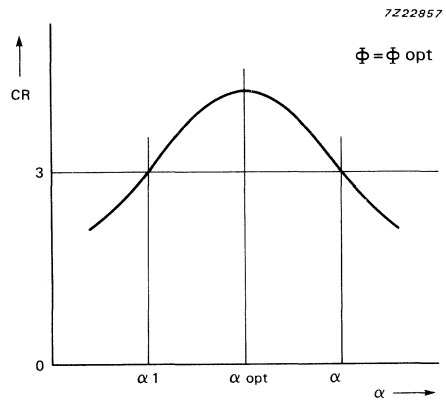
$$\text{in positive image mode: } CR = \frac{B_{off}}{B_{on}}$$

$$\text{in negative image mode: } CR = \frac{B_{on}}{B_{off}}$$

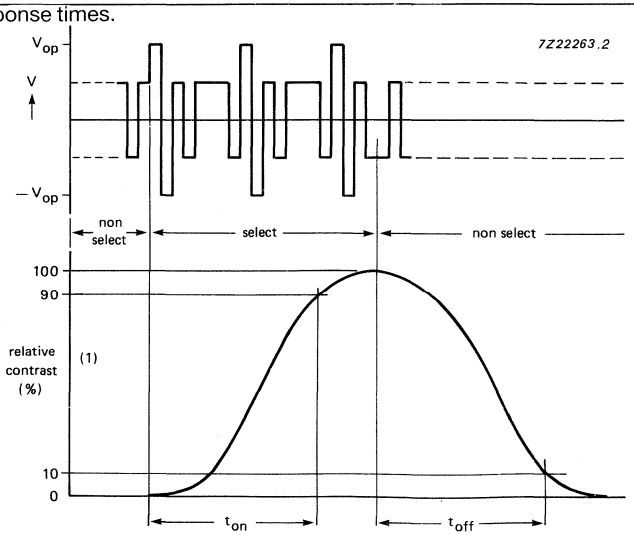
B_{on} is the brightness of selected segments
B_{off} is the brightness of non-selected segments

Note 2 Definition of viewing angles α and ϕ.





Note 3 Definition of response times.



1) measured at $\alpha = 10°$

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTN211
Liquid crystal display

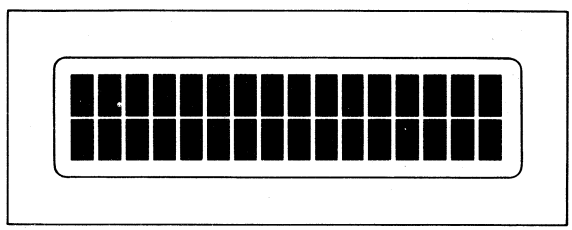
MODULE DESCRIPTION

The LTN211 is a 5 x 7 dot, 16-character, 2-line dot matrix LCD module, with driver and controller LSI IC mounted on a single printed circuit board. The LSI controller incorporates a ROM-based character generator with a 160 characters and RAM display data with 8 characters. The module is capable of generating 160 fixed and 8 write by programme characters. The LTN211 operates from an extensive instruction set: display clear, cursor home, display ON/OFF, cursor ON/OFF, character blink, cursor shift and display shift.

QUICK REFERENCE DATA

Outline dimensions	84 x 44 x 12 mm
Viewing area	61.0 x 15.8 mm
Character format	5 x 7 dots and cursor
Character size	2.96 x 5.56 mm
Dot size (spacing 0.04 mm)	0.56 x 0.66 mm
Mass	≈ 25 g
Drive method	MUX 1:16
Supply voltage	+5 V
Power consumption	7.5 mW
Illumination mode	reflective/trans-flective
Front surface	glossy
Character generator	built in
Data interface	parallel 4 or 8 bits

DISPLAY MODE



7Z22324

Fig.1 16-character, 2-line LCD module.

TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	VIEWING DIRECTION	TO BE USED WITH EL BACKLIGHT
LTN211R-10	reflective	6 o'clock	-
LTN211F-10	transflective	6 o'clock	LXL211-G
LTN211R-50	reflective	12 o'clock	-
LTN211F-50	transflective	12 o'clock	LXL211-G

MECHANICAL DATA

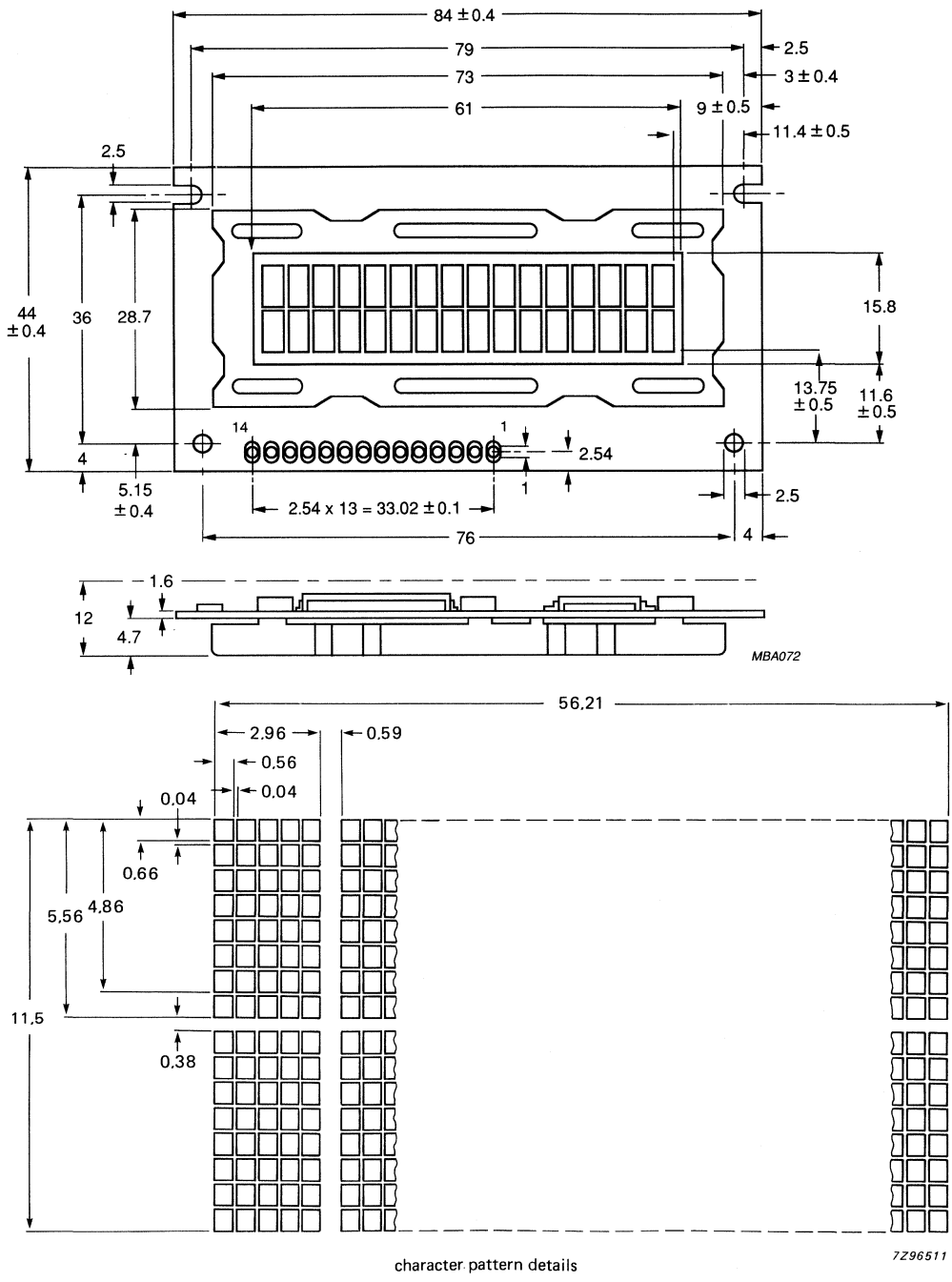


Fig.2 Outline dimensions.

Liquid crystal display

LTN211

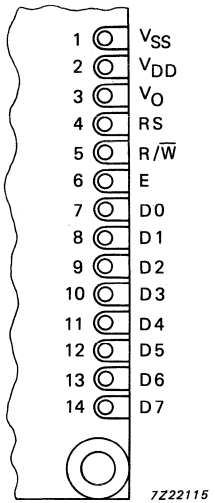


Fig.3 Pin configuration.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	V_{SS}	ground
2	V_{DD}	power supply (logic)
3	V_O	contrast adjustment voltage
4	RS	register select
5	R/W	read/write
6	E	enable
7	D0	I/O data LSB
8	D1	I/O data 2nd bit
9	D2	I/O data 3rd bit
10	D3	I/O data 4th bit
11	D4	I/O data 5th bit
12	D5	I/O data 6th bit
13	D6	I/O data 7th bit
14	D7	I/O data MSB

Notes to pin description

1. Contrast is adjusted by varying the voltage V_O between 0 and 5 V.
2. D7 doubles as busy flag.
3. When the module is interfaced with a microprocessor with 4-bit parallel outputs, pins D0 to D3 are not used.

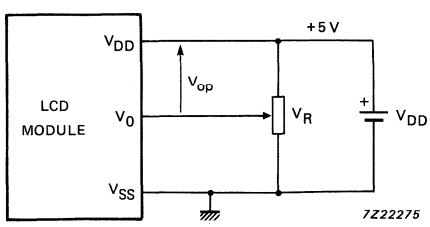


Fig.4 Power supply.

Liquid crystal display LTN211

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{DD}	−0.3	–	7.0	V
LCD drive voltage (V_{DD}-V_O)	V_{op}	0	–	9.0	V
Input voltage	V_I	−0.3	–	V_{DD}+0.3	V
Storage temperature	T_{stg}	−25	–	+70	°C
Operating ambient temperature	T_{amb}	0	–	+50	°C

OPERATING CHARACTERISTICS

T_{amb} = 25 °C; V_{DD} = 5 V; all voltages refer to V_{SS}; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (logic)	V_{DD}-V_{SS}	4.75	5.0	5.25	V
Contrast adjustment voltage	V_O	–	0.6	–	V
Temperature compensation of V_O	TC	–	−14	–	mV/°C
LOW level input voltage	V_{IL}	−0.3	–	0.6	V
HIGH level input voltage	V_{IH}	2.2	–	V_{DD}	V
LOW level output voltage -I_{OL} = 1.2 mA	V_{OL}	–	–	0.4	V
HIGH level output voltage -I_{OH} = 0.205 mA	V_{OH}	2.4	–	–	V
Input leakage current	I_I	–	–	1.0	µA
Internal oscillating frequency	f_{OSC}	–	250	–	kHz
Supply current (logic)	I_{DD}	–	1.5	2.2	mA
Power dissipation	P_d	–	7.5	11.0	mW

TIMING CHARACTERISTICS

T_{amb} = 0 to 50 °C, V_{DD} = 5 V +/− 5%, unless otherwise specified.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Enable cycle time	t_{cyc}	1000	–	–	ns
Enable pulse width	t_W	450	–	–	ns
Rise time	t_r	–	–	25	ns
Fall time	t_f	–	–	25	ns
Register select set-up time	t_{rsu}	140	–	–	ns
Read and write set-up time	t_{su}	140	–	–	ns
Data set-up time	t_{dsu}	195	–	–	ns
Data delay time	t_d	–	–	320	ns
Address hold time	t_{AH}	10	–	–	ns
Data hold time write	t_{WH}	10	–	–	ns
Data hold time read	t_{RH}	20	–	–	ns

ELECTRO-OPTICAL CHARACTERISTICS

T_{amb} = 25 °C, $V_{DD} = V_{DD\ typ}$, α = 10°, $\phi = \phi_{opt}$, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	TYP.	MAX.	UNIT
Response times	t_{on}	T_{amb} = 0 °C T_{amb} = 25 °C T_{amb} = 50 °C	380 110 45	760 220 90	ms ms ms
	t_{off}	T_{amb} = 0 °C T_{amb} = 25 °C T_{amb} = 50 °C	470 110 45	940 220 90	ms ms ms
Viewing Angles (contrast ratio CR > 3)	α_{opt} α_2-α_1	reflective types	30 30	– –	° °
	α_{opt} α_2-α_1	transflective types reflective operation	30 25	– –	° °
	α_{opt} α_2-α_1	transflective types transmissive operation	30 20	– –	° °

For definitions of response times, viewing angles and contrast ratio refer to notes 1 to 3

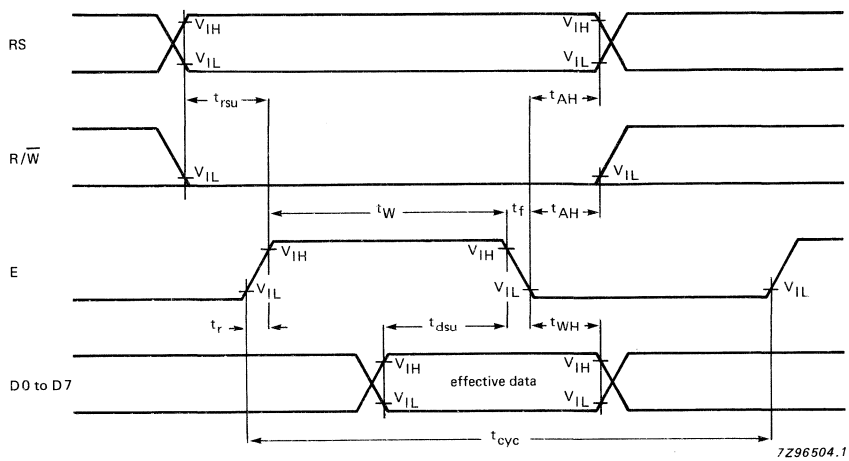


Fig.5 Timing waveforms (write operation).

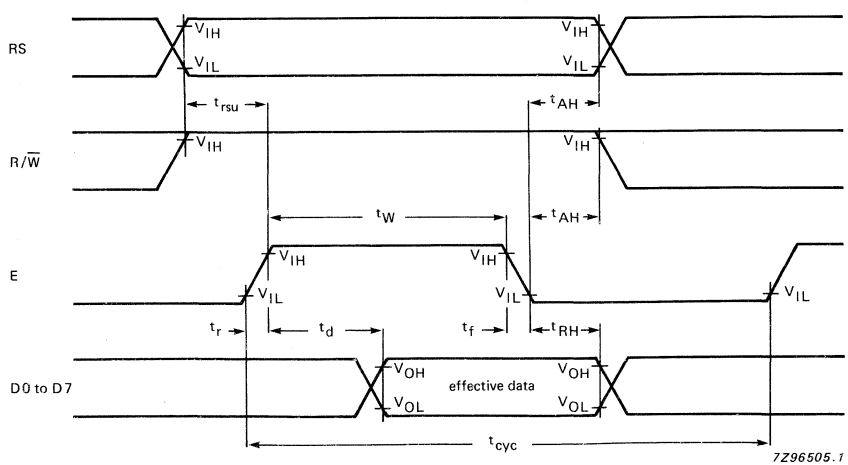


Fig.6 Timing waveforms (read operation).

Liquid crystal display LTN211

Table 1 Instruction set

INSTRUCTION \ ADDRESSES	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Display clear	0	0	0	0	0	0	0	0	0	1
Cursor home	0	0	0	0	0	0	0	0	1	*
Entry mode set	0	0	0	0	0	0	0	1	I/D	S
Display on/off control	0	0	0	0	0	0	1	D	C	B
Cursor display shift	0	0	0	0	0	1	S/C	R/L	*	*
Function set	0	0	0	0	1	DL	1	0	*	*
CG RAM address set	0	0	0	1	A_{CG}					
DD RAM address set	0	0	1	A_{DD}						
Busy flag/address read	0	1	BF	AC						
CG RAM/DD RAM data write	1	0	write data							
CG RAM/DD RAM data read	1	1	read data							

Notes:

I/D	= 1:increment	I/D	= 0:decrement
S	= 1:display shift	S	= 0:display freeze
D	= 1:display on	D	= 0:display off
C	= 1:cursor on	C	= 0:cursor off
B	= 1:character at cursor position blinks	B	= 0:character at cursor position does not blink
S/C	= 1:display shift	S/C	= 0:cursor move
R/L	= 1:right shift	R/L	= 0:left shift
DL	= 1:8 bits	DL	= 0:4 bits
BF	= 1:during internal operation	BF	= 0:end of internal operation

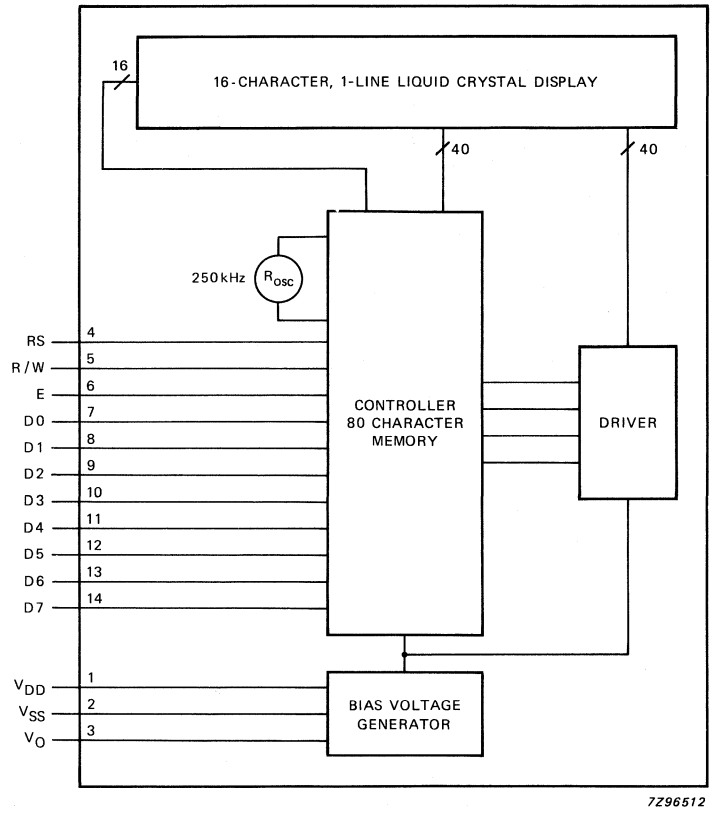
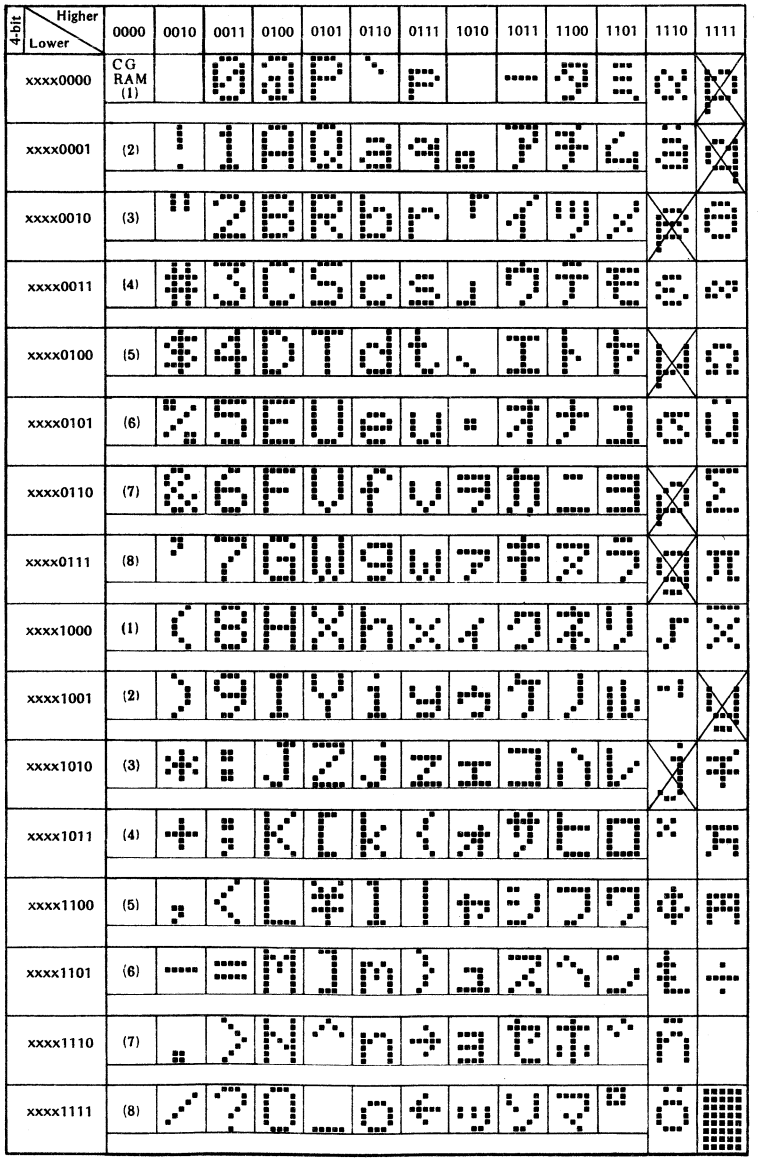


Fig.7 Functional block diagram.

Table 2 Display position and DD RAM address (HEX)

Digit	1	2	3	4	5	6	7	8	9		16
Line 1	00_H	01_H	02_H	03_H	04_H	05_H	06_H	07_H	08_H	.....	$0F_H$
Line 2	40_H	41_H	42_H	43_H	44_H	45_H	46_H	47_H	48_H	.....	$4F_H$

Table 3 Input codes vs character pattern



Liquid crystal display | LTN211

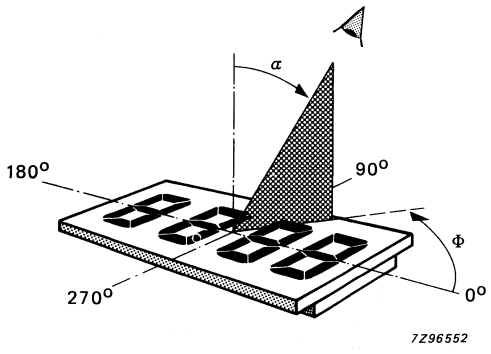
Note 1 Definition of contrast ratio (C_R).

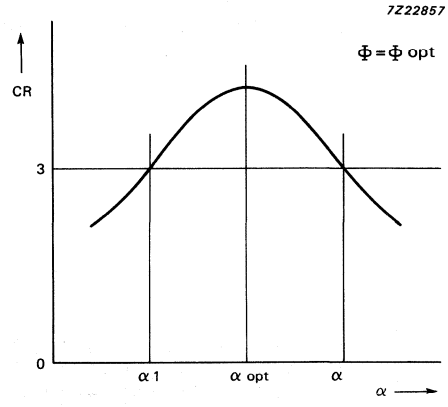
$$\text{in positive image mode: } CR = \frac{B_{off}}{B_{on}}$$

$$\text{in negative image mode: } CR = \frac{B_{on}}{B_{off}}$$

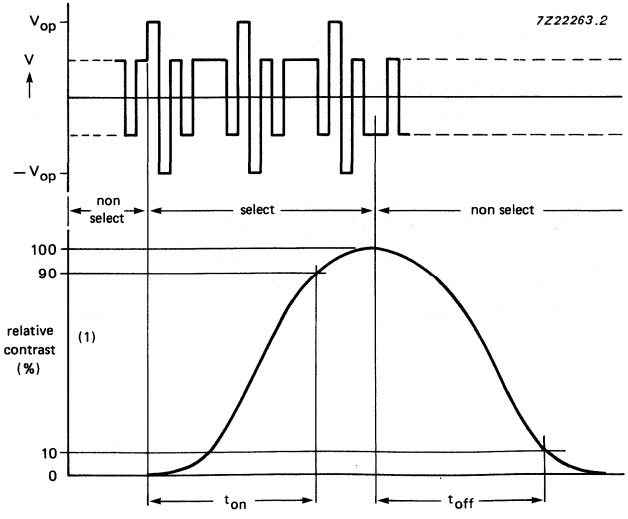
B_{on} is the brightness of selected segments
B_{off} is the brightness of non-selected segments

Note 2 Definition of viewing angles α and ϕ.





Note 3 Definition of response times.



1) measured at $\alpha = 10°$

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTN221
Liquid crystal display

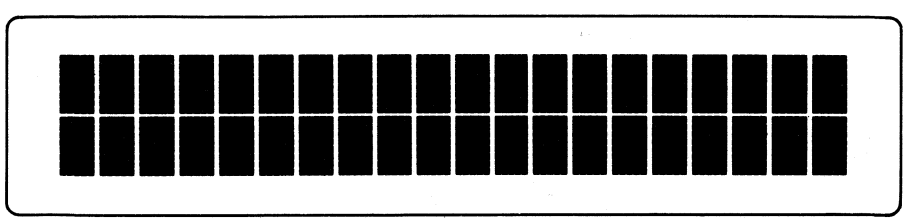
MODULE DESCRIPTION

The LTN221 is a 5 x 7 dot, 20-character, 2-line dot matrix LCD module, with driver and controller LSI IC mounted on a single printed circuit board. The LSI controller incorporates a ROM-based character generator with a 160 characters and RAM display data with 8 characters. The module is capable of generating 160 fixed and 8 write by programme characters. The LTN221 operates from an extensive instruction set: display clear, cursor home, display ON/OFF, cursor ON/OFF, character blink, cursor shift and display shift.

QUICK REFERENCE DATA

Outline dimensions	116 x 37 x 11 mm
Viewing area	83.0 x 18.6 mm
Character format	5 x 7 dots and cursor
Character size	3.2 x 5.55 mm
Dot size (spacing 0.05 mm)	0.6 x 0.65 mm
Mass	≈ 25 g
Drive method	MUX 1:16
Supply voltage	+5 V
Power consumption	7.5 mW
Illumination mode	reflective/trans-flective
Front surface	glossy
Character generator	built in
Data interface	parallel 4 or 8 bits

DISPLAY MODE



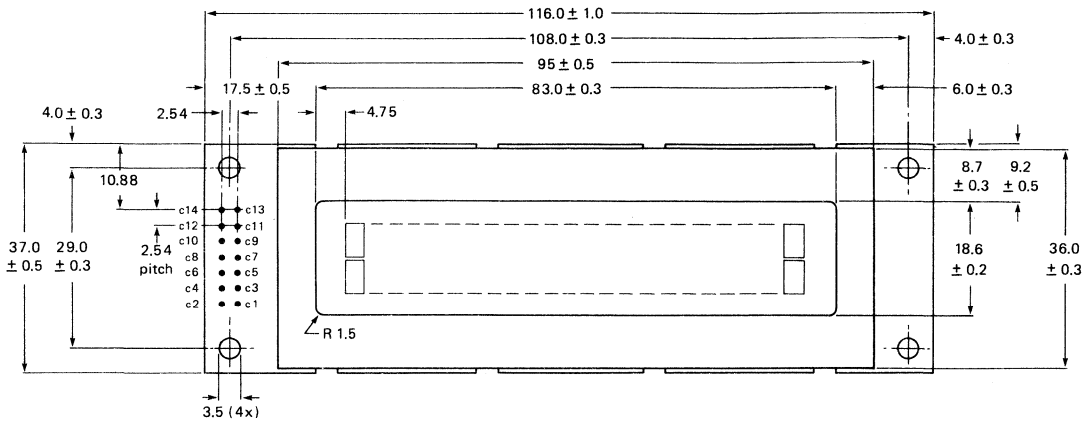
7Z22277

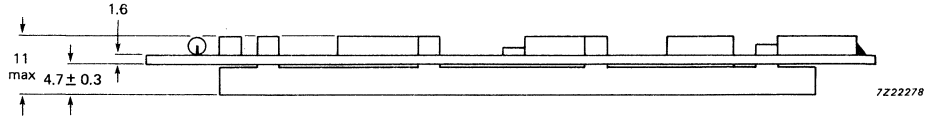
Fig.1 20-character, 2-line LCD module.

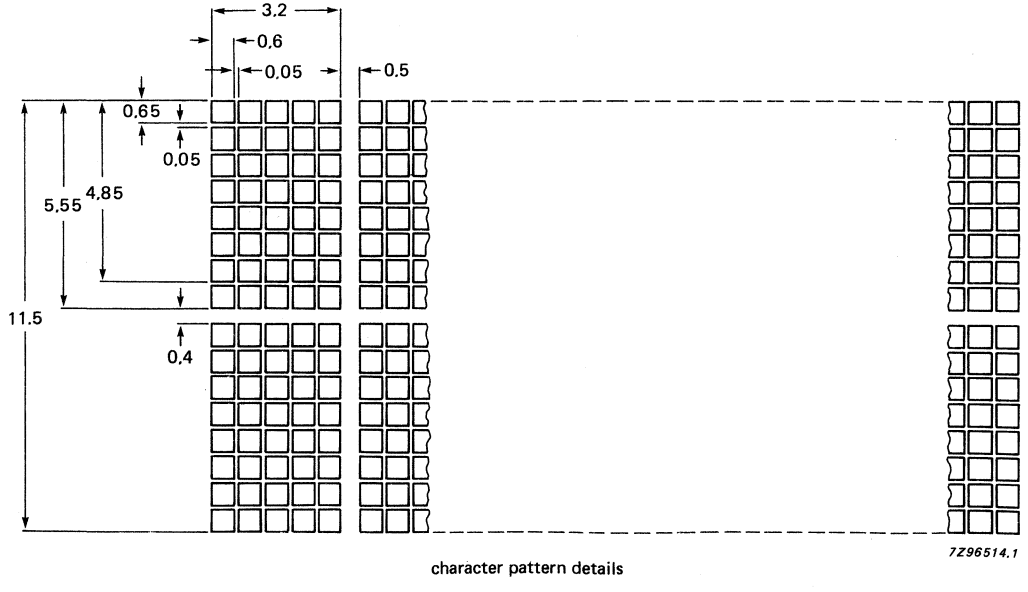
TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	VIEWING DIRECTION	TO BE USED WITH EL BACKLIGHT
LTN221R-10	reflective	6 o'clock	–
LTN221F-10	transflective	6 o'clock	LXL221-G

MECHANICAL DATA







character pattern details

Fig.2 Outline dimensions.

Liquid crystal display LTN221

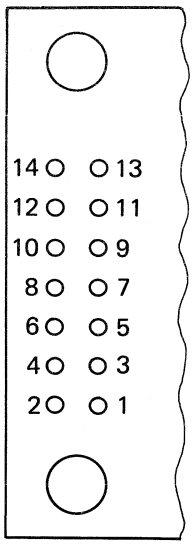


Fig.3 Pin configuration.

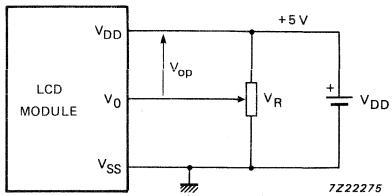


Fig.4 Power supply.

Notes to pin description

1. Contrast is adjusted by varying the voltage V_O between 0 and 5 V.
2. D7 doubles as busy flag.
3. When the module is interfaced with a microprocessor with 4-bit parallel outputs, pins D0 to D3 are not used.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	V_{SS}	ground
2	V_{DD}	power supply (logic)
3	V_O	contrast adjustment voltage
4	RS	register select
5	R/W	read/write
6	E	enable
7	D0	I/O data LSB
8	D1	I/O data 2nd bit
9	D2	I/O data 3rd bit
10	D3	I/O data 4th bit
11	D4	I/O data 5th bit
12	D5	I/O data 6th bit
13	D6	I/O data 7th bit
14	D7	I/O data MSB

Liquid crystal display LTN221

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{DD}	−0.3	–	7.0	V
LCD drive voltage (V_{DD}-V_O)	V_{op}	0	–	9.0	V
Input voltage	V_I	−0.3	–	V_{DD}+0.3	V
Storage temperature	T_{stg}	−25	–	+70	°C
Operating ambient temperature	T_{amb}	0	–	+50	°C

OPERATING CHARACTERISTICS

T_{amb} = 25 °C; V_{DD} = 5 V; all voltages refer to V_{SS}; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (logic)	V_{DD}-V_{SS}	4.75	5.0	5.25	V
Contrast adjustment voltage	V_O	–	0.0	–	V
Temperature compensation of V_O	TC	–	−14	–	mV/°C
LOW level input voltage	V_{IL}	−0.3	–	0.6	V
HIGH level input voltage	V_{IH}	2.2	–	V_{DD}	V
LOW level output voltage -I_{OL} = 1.2 mA	V_{OL}	–	–	0.4	V
HIGH level output voltage -I_{OH} = 0.205 mA	V_{OH}	2.4	–	–	V
Input leakage current	I_I	–	–	1.0	µA
Internal oscillating frequency	f_{OSC}	–	250	–	kHz
Supply current (logic)	I_{DD}	–	1.5	2.4	mA
Power dissipation	P_d	–	7.5	12.0	mW

TIMING CHARACTERISTICS

T_{amb} = 0 to 50 °C, V_{DD} = 5 V +/− 5%, unless otherwise specified.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Enable cycle time	t_{cyc}	1000	–	–	ns
Enable pulse width	t_W	450	–	–	ns
Rise time	t_r	–	–	25	ns
Fall time	t_f	–	–	25	ns
Register select set-up time	t_{rsu}	140	–	–	ns
Read and write set-up time	t_{su}	140	–	–	ns
Data set-up time	t_{dsu}	195	–	–	ns
Data delay time	t_d	–	–	320	ns
Address hold time	t_{AH}	10	–	–	ns
Data hold time write	t_{WH}	10	–	–	ns
Data hold time read	t_{RH}	20	–	–	ns

ELECTRO-OPTICAL CHARACTERISTICS

T_{amb} = 25 °C, $V_{DD} = V_{DD\ typ}$, α = 10°, $\phi = \phi_{opt}$, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	TYP.	MAX.	UNIT
Response times	t_{on}	T_{amb} = 0 °C T_{amb} = 25 °C T_{amb} = 50 °C	380 110 45	760 220 90	ms ms ms
	t_{off}	T_{amb} = 0 °C T_{amb} = 25 °C T_{amb} = 50 °C	470 110 45	940 220 90	ms ms ms
Viewing Angles (contrast ratio CR > 3)	α_{opt} α_2-α_1	reflective types	30 30	– –	° °
	α_{opt} α_2-α_1	transflective types reflective operation	30 25	– –	° °
	α_{opt} α_2-α_1	transflective types transmissive operation	30 20	– –	° °

For definitions of response times, viewing angles and contrast ratio refer to notes 1 to 3

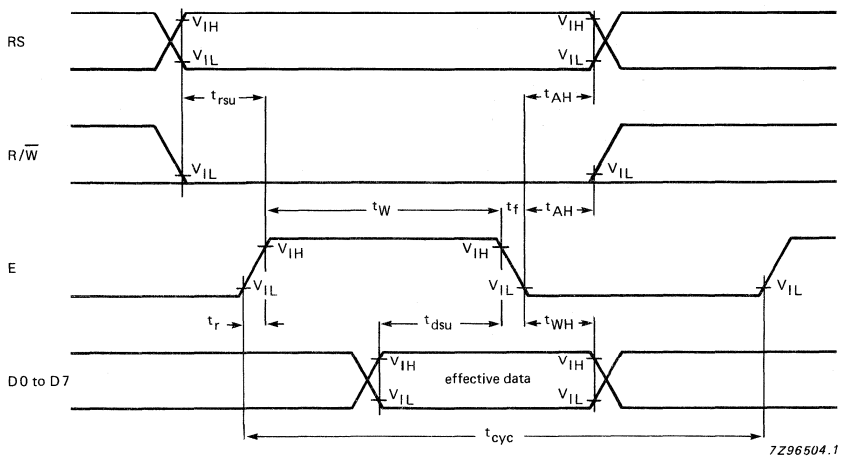


Fig.5 Timing waveforms (write operation).

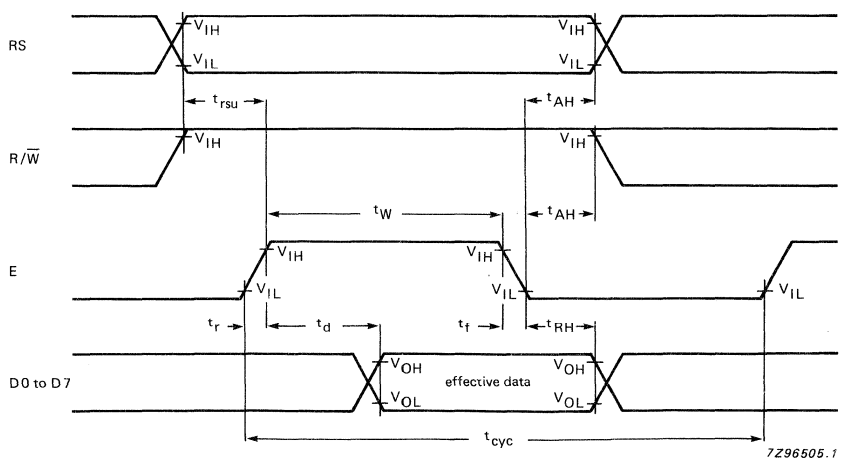


Fig.6 Timing waveforms (read operation).

Table 1 Instruction set

INSTRUCTION \ ADDRESSES	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Display clear	0	0	0	0	0	0	0	0	0	1
Cursor home	0	0	0	0	0	0	0	0	1	*
Entry mode set	0	0	0	0	0	0	0	1	I/D	S
Display on/off control	0	0	0	0	0	0	1	D	C	B
Cursor display shift	0	0	0	0	0	1	S/C	R/L	*	*
Function set	0	0	0	0	1	DL	1	0	*	*
CG RAM address set	0	0	0	1	A_{CG}					
DD RAM address set	0	0	1	A_{DD}						
Busy flag/address read	0	1	BF	AC						
CG RAM/DD RAM data write	1	0	write data							
CG RAM/DD RAM data read	1	1	read data							

Notes:

I/D	= 1:increment		I/D	= 0:decrement
S	= 1:display shift		S	= 0:display freeze
D	= 1:display on		D	= 0:display off
C	= 1:cursor on		C	= 0:cursor off
B	= 1:character at cursor position blinks		B	= 0:character at cursor position does not blink
S/C	= 1:display shift		S/C	= 0:cursor move
R/L	= 1:right shift		R/L	= 0:left shift
DL	= 1:8 bits		DL	= 0:4 bits
BF	= 1:during internal operation		BF	= 0:end of internal operation

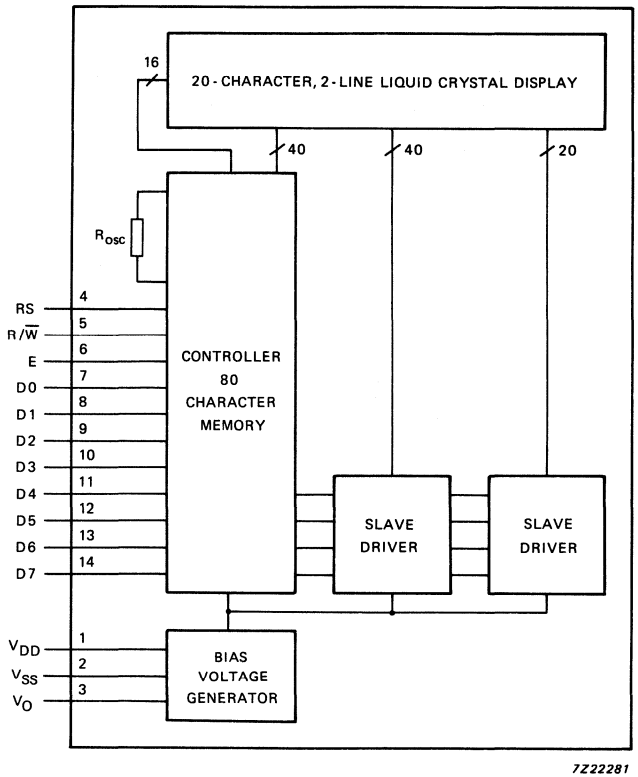


Fig. 7 Functional block diagram.

Table 2 Display position and DD RAM address (HEX)

	display position												
digit	1	2	3	4	5	6	7	8	9			19	20
line 1	00_H	01_H	02_H	03_H	04_H	05_H	06_H	07_H	08_H			12_H	13_H
line 2	40_H	41_H	42_H	43_H	44_H	45_H	46_H	47_H	48_H			52_H	53_H

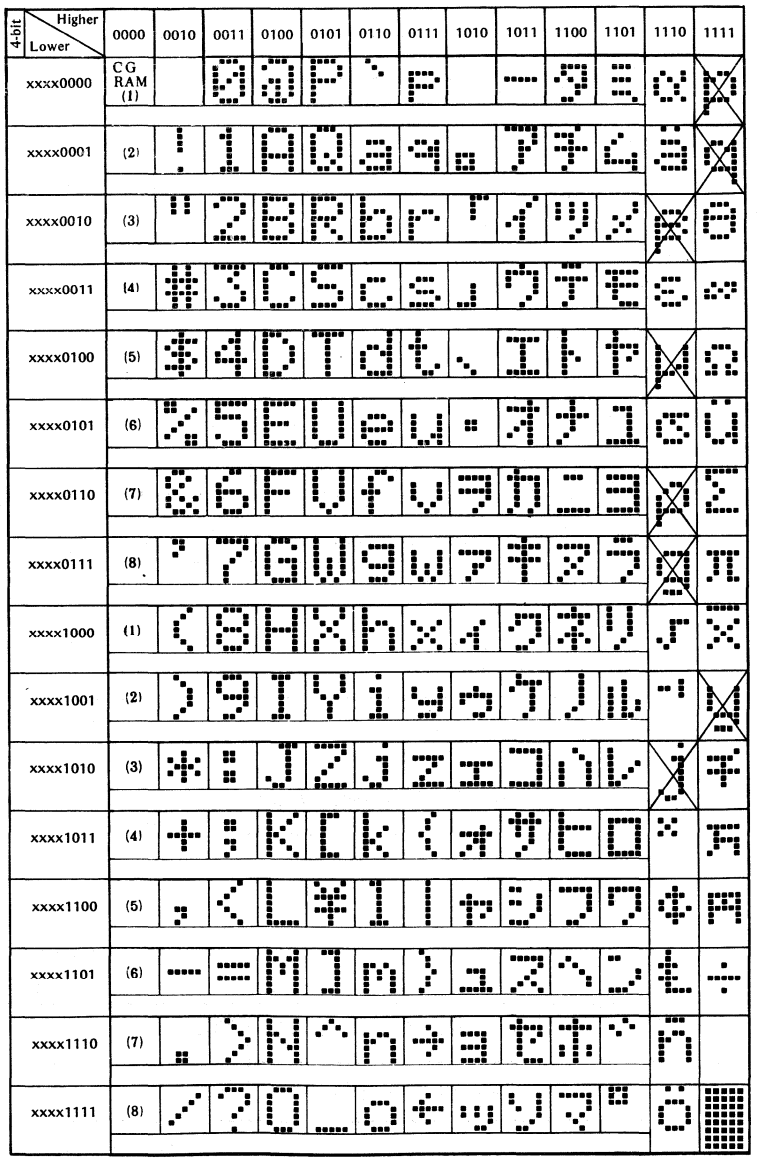
7Z22280

DD RAM address (HEX)

Liquid crystal display

LTN221

Table 3 Input codes vs character pattern



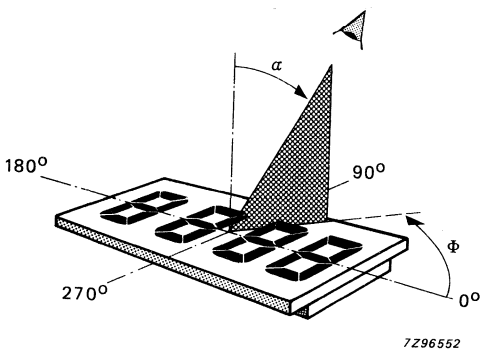
Note 1 Definition of contrast ratio (C_R).

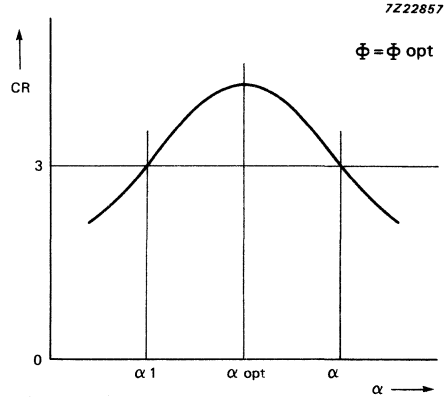
$$\text{in positive image mode: } CR = \frac{B_{off}}{B_{on}}$$

$$\text{in negative image mode: } CR = \frac{B_{on}}{B_{off}}$$

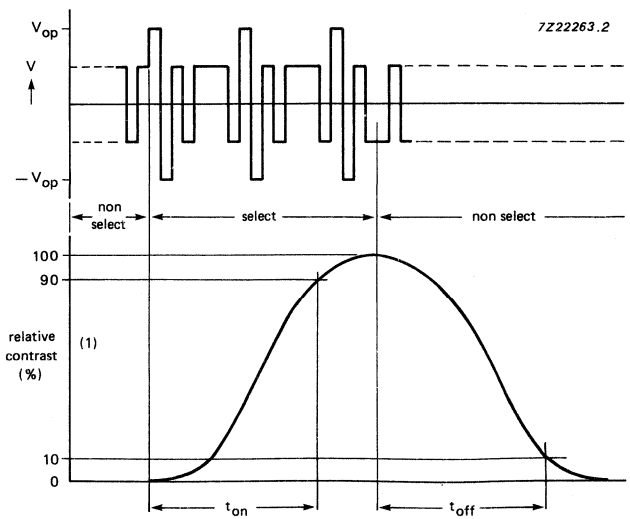
B_{on} is the brightness of selected segments
B_{off} is the brightness of non-selected segments

Note 2 Definition of viewing angles α and ϕ.





Note 3 Definition of response times.



1) measured at $\alpha = 10°$

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTN222
Liquid crystal display

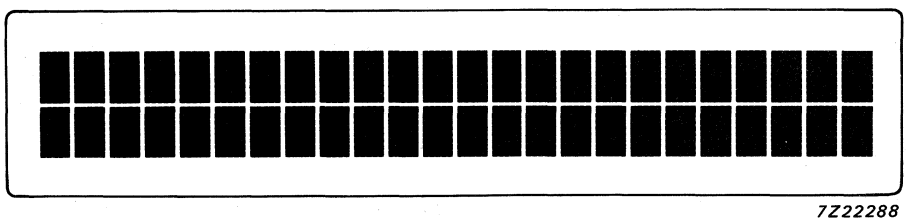
MODULE DESCRIPTION

The LTN222 is a 5 x 7 dot, 24-character, 2-line dot matrix LCD module, with driver and controller LSI IC mounted on a single printed circuit board. The LSI controller incorporates a ROM-based character generator with a 160 characters and RAM display data with 8 characters. The module is capable of generating 160 fixed and 8 write by programme characters. The LTN222 operates from an extensive instruction set: display clear, cursor home, display ON/OFF, cursor ON/OFF, character blink, cursor shift and display shift.

QUICK REFERENCE DATA

Outline dimensions	116 x 37 x 11 mm
Viewing area	83.0 x 18.6 mm
Character format	5 x 7 dots and cursor
Character size	2.7 x 5.55 mm
Dot size (spacing 0.05 mm)	0.5 x 0.65 mm
Mass	≈ 50 g
Drive method	MUX 1:16
Supply voltage	+5 V
Power consumption	7.5 mW
Illumination mode	reflective/trans-flective
Front surface	glossy
Character generator	built in
Data interface	parallel 4 or 8 bits

DISPLAY MODE



7Z22288

Fig.1 24-character, 2-line LCD module.

TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	VIEWING DIRECTION	TO BE USED WITH EL BACKLIGHT
LTN222R-10	reflective	6 o'clock	–
LTN222F-10	transflective	6 o'clock	LXL221-G

MECHANICAL DATA

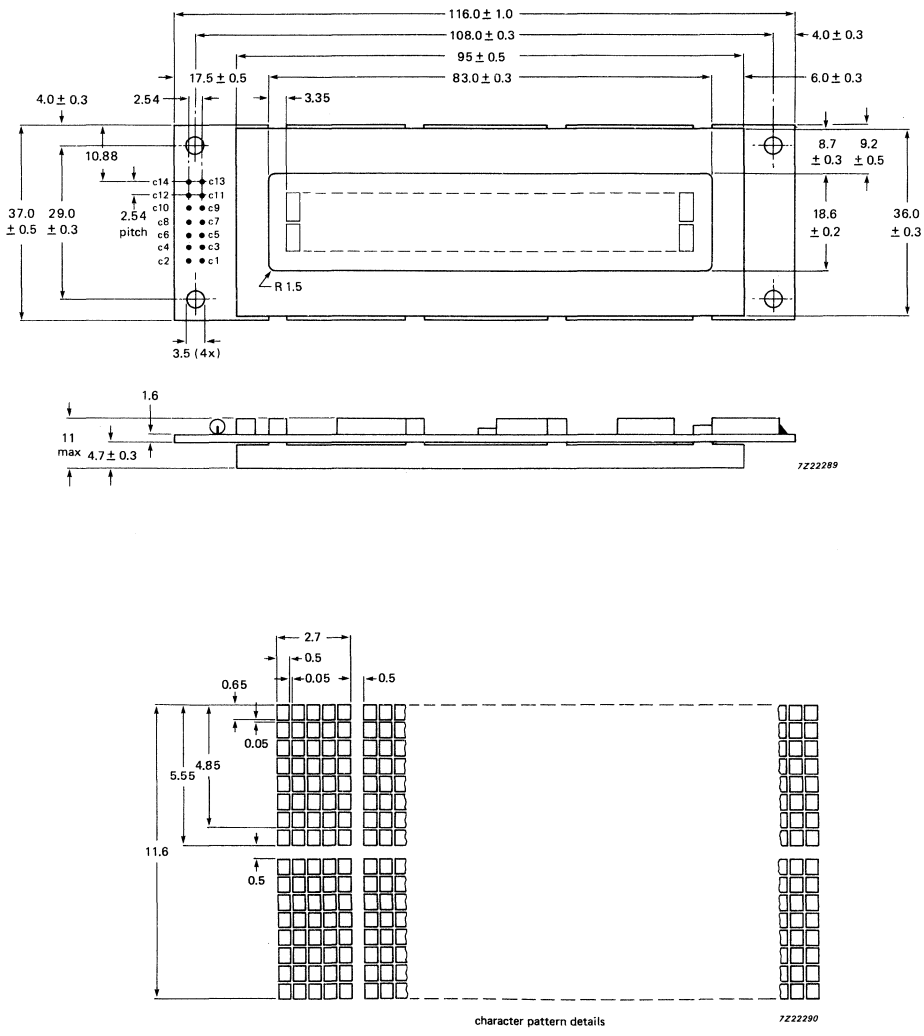


Fig.2 Outline dimensions.

Liquid crystal display LTN222

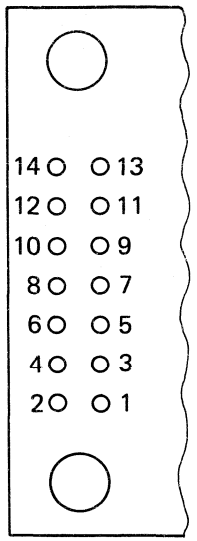


Fig.3 Pin configuration.

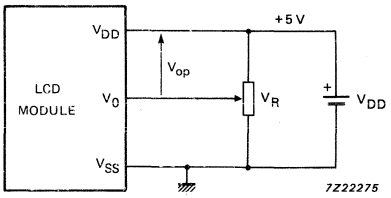


Fig.4 Power supply.

Notes to pin description

1. Contrast is adjusted by varying the voltage V_O between 0 and 5 V.
2. D7 doubles as busy flag.
3. When the module is interfaced with a microprocessor with 4-bit parallel outputs, pins D0 to D3 are not used.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	V_{SS}	ground
2	V_{DD}	power supply (logic)
3	V_O	contrast adjustment voltage
4	RS	register select
5	R/W	read/write
6	E	enable
7	D0	I/O data LSB
8	D1	I/O data 2nd bit
9	D2	I/O data 3rd bit
10	D3	I/O data 4th bit
11	D4	I/O data 5th bit
12	D5	I/O data 6th bit
13	D6	I/O data 7th bit
14	D7	I/O data MSB

Liquid crystal display LTN222

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{DD}	−0.3	–	7.0	V
LCD drive voltage (V_{DD}-V_O)	V_{op}	0	–	9.0	V
Input voltage	V_I	−0.3	–	V_{DD}+0.3	V
Storage temperature	T_{stg}	−25	–	+70	°C
Operating ambient temperature	T_{amb}	0	–	+50	°C

OPERATING CHARACTERISTICS

T_{amb} = 25 °C; V_{DD} = 5 V; all voltages refer to V_{SS}; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (logic)	V_{DD}-V_{SS}	4.75	5.0	5.25	V
Contrast adjustment voltage	V_O	–	0.0	–	V
Temperature compensation of V_O	TC	–	−14	–	mV/°C
LOW level input voltage	V_{IL}	−0.3	–	0.6	V
HIGH level input voltage	V_{IH}	2.2	–	V_{DD}	V
LOW level output voltage -I_{OL} = 1.2 mA	V_{OL}	–	–	0.4	V
HIGH level output voltage -I_{OH} = 0.205 mA	V_{OH}	2.4	–	–	V
Input leakage current	I_I	–	–	1.0	μA
Internal oscillating frequency	f_{OSC}	–	250	–	kHz
Supply current (logic)	I_{DD}	–	1.5	2.4	mA
Power dissipation	P_d	–	7.5	12.0	mW

TIMING CHARACTERISTICS

T_{amb} = 0 to 50 °C, V_{DD} = 5 V +/− 5%, unless otherwise specified.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Enable cycle time	t_{cyc}	1000	–	–	ns
Enable pulse width	t_W	450	–	–	ns
Rise time	t_r	–	–	25	ns
Fall time	t_f	–	–	25	ns
Register select set-up time	t_{rsu}	140	–	–	ns
Read and write set-up time	t_{su}	140	–	–	ns
Data set-up time	t_{dsu}	195	–	–	ns
Data delay time	t_d	–	–	320	ns
Address hold time	t_{AH}	10	–	–	ns
Data hold time write	t_{WH}	10	–	–	ns
Data hold time read	t_{RH}	20	–	–	ns

ELECTRO-OPTICAL CHARACTERISTICS

T_{amb} = 25 °C, $V_{DD} = V_{DD\ typ}$, α = 10°, $\phi = \phi_{opt}$, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	TYP.	MAX.	UNIT
Response times	t_{on}	T_{amb} = 0 °C T_{amb} = 25 °C T_{amb} = 50 °C	380 110 45	760 220 90	ms ms ms
	t_{off}	T_{amb} = 0 °C T_{amb} = 25 °C T_{amb} = 50 °C	470 110 45	940 220 90	ms ms ms
Viewing Angles (contrast ratio CR > 3)	α_{opt} α_2-α_1	reflective types	30 30	– –	° °
	α_{opt} α_2-α_1	transflective types reflective operation	30 25	– –	° °
	α_{opt} α_2-α_1	transflective types transmissive operation	30 20	– –	° °

For definitions of response times, viewing angles and contrast ratio refer to notes 1 to 3

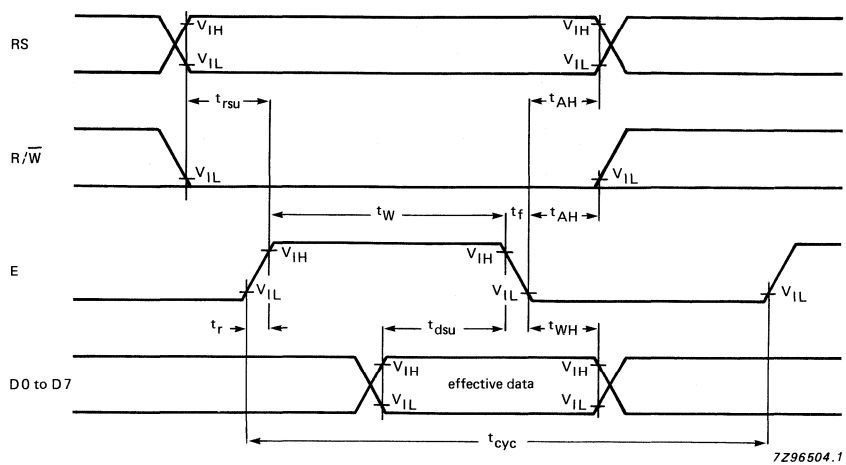


Fig.5 Timing waveforms (write operation).

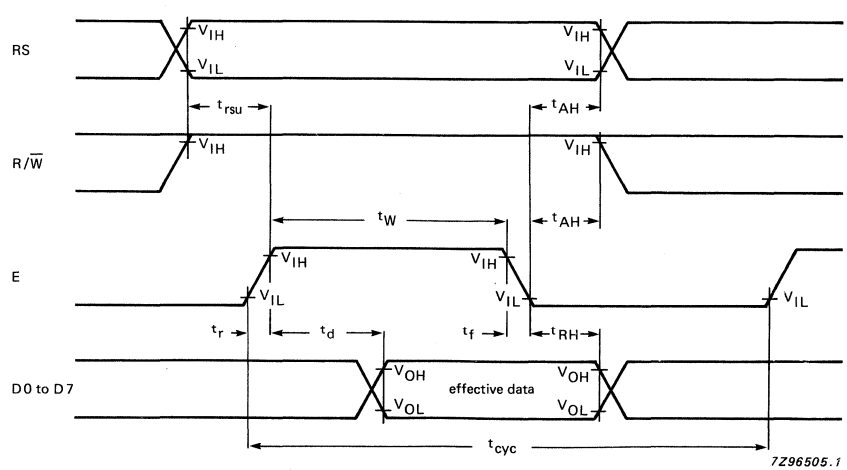


Fig.6 Timing waveforms (read operation).

Liquid crystal display LTN222

INSTRUCTION \ ADDRESSES	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Display clear	0	0	0	0	0	0	0	0	0	1
Cursor home	0	0	0	0	0	0	0	0	1	*
Entry mode set	0	0	0	0	0	0	0	1	I/D	S
Display on/off control	0	0	0	0	0	0	1	D	C	B
Cursor display shift	0	0	0	0	0	1	S/C	R/L	*	*
Function set	0	0	0	0	1	DL	1	0	*	*
CG RAM address set	0	0	0	1	A_{CG}					
DD RAM address set	0	0	1	A_{DD}						
Busy flag/address read	0	1	BF	AC						
CG RAM/DD RAM data write	1	0	write data							
CG RAM/DD RAM data read	1	1	read data							

Notes:

I/D	= 1:increment		I/D	= 0:decrement
S	= 1:display shift		S	= 0:display freeze
D	= 1:display on		D	= 0:display off
C	= 1:cursor on		C	= 0:cursor off
B	= 1:character at cursor position blinks		B	= 0:character at cursor position does not blink
S/C	= 1:display shift		S/C	= 0:cursor move
R/L	= 1:right shift		R/L	= 0:left shift
DL	= 1:8 bits		DL	= 0:4 bits
BF	= 1:during internal operation		BF	= 0:end of internal operation

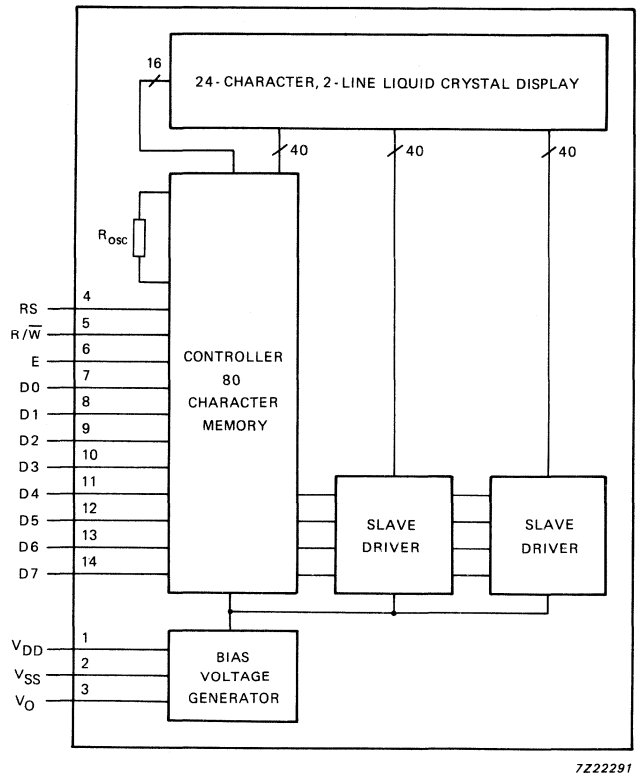


Fig.7 Functional block diagram.

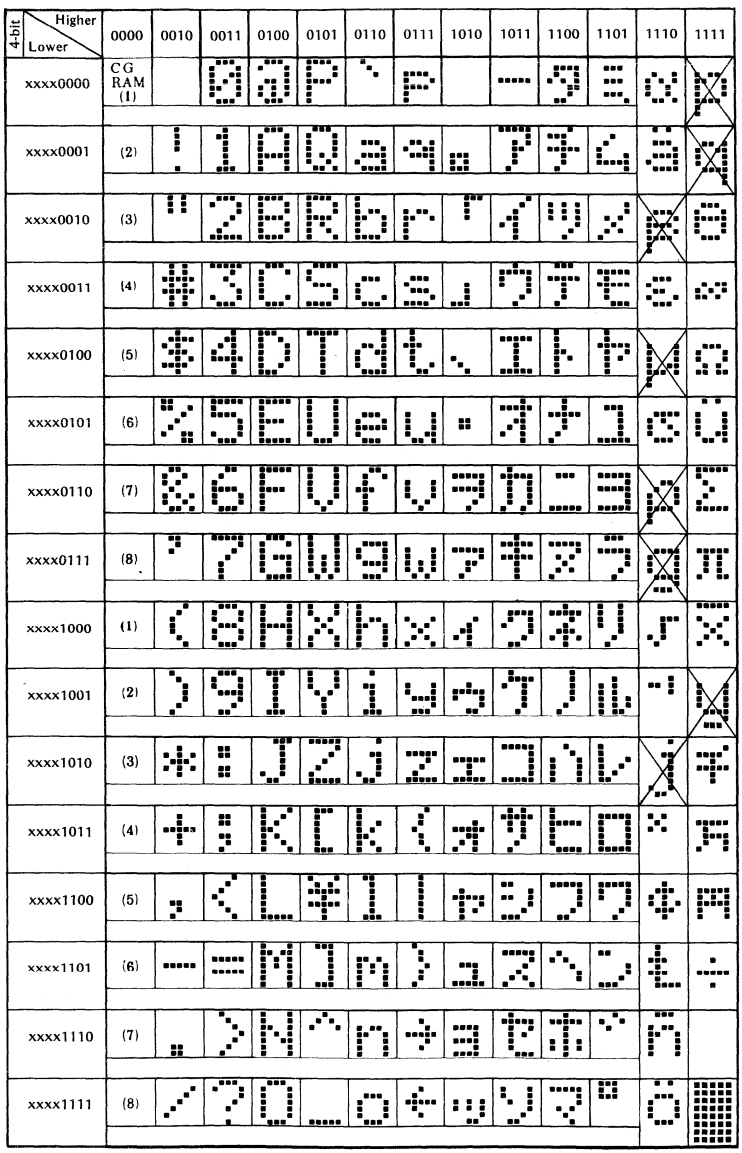
Table 2 Display position and DD RAM address (HEX)

	display position												
digit	1	2	3	4	5	6	7	8	9			23	24
line 1	00_H	01_H	02_H	03_H	04_H	05_H	06_H	07_H	08_H			16_H	17_H
line 2	40_H	41_H	42_H	43_H	44_H	45_H	46_H	47_H	48_H			56_H	57_H

7Z22292 DD RAM address (HEX)

Liquid crystal display LTN222

Table 3 Input codes vs character pattern



Liquid crystal display | LTN222

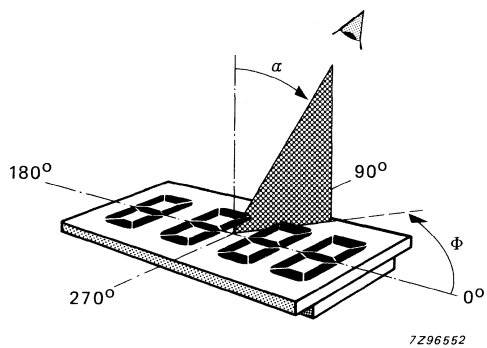
Note 1 Definition of contrast ratio (C_R).

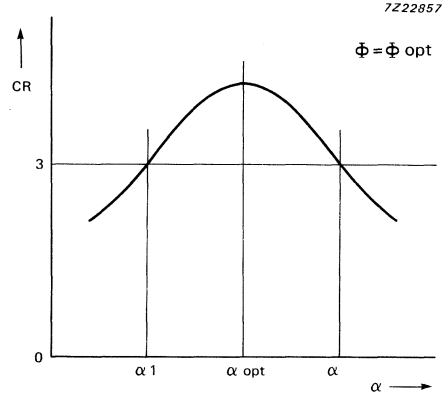
$$\text{in positive image mode: } CR = \frac{B_{off}}{B_{on}}$$

$$\text{in negative image mode: } CR = \frac{B_{on}}{B_{off}}$$

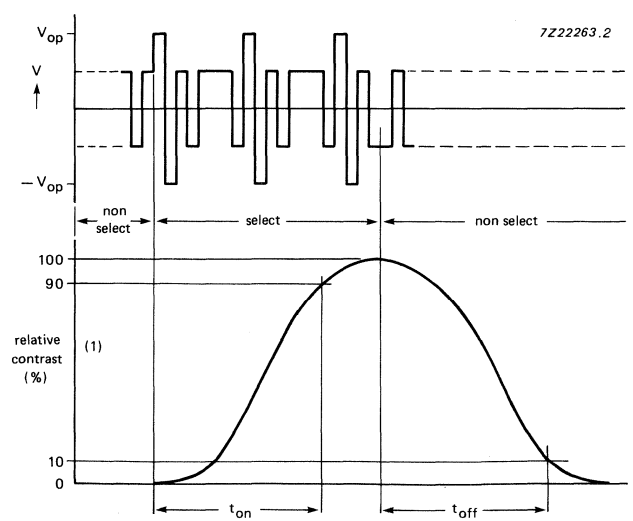
B_{on} is the brightness of selected segments
B_{off} is the brightness of non-selected segments

Note 2 Definition of viewing angles α and ϕ.





Note 3 Definition of response times.



1) measured at $\alpha = 10°$

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LTN243
Liquid crystal display

MODULE DESCRIPTION

The LTN243 is a 5 x 7 dot, 40-character, 2-line dot matrix LCD module, with driver and controller LSI IC mounted on a single printed circuit board. The LSI controller incorporates a ROM-based character generator with a 160 characters and RAM display data with 8 characters. The module is capable of generating 160 fixed and 8 write by programme characters. The LTN243 operates from an extensive instruction set: display clear, cursor home, display ON/OFF, cursor ON/OFF, character blink, cursor shift and display shift.

QUICK REFERENCE DATA

Outline dimensions	182 x 33.5 x 11 mm
Viewing area	154.4 x 15.8 mm
Character format	5 x 7 dots and cursor
Character size	3.2 x 5.55 mm
Dot size (spacing 0.05 mm)	0.6 x 0.65 mm
Mass	~ 65 g
Drive method	MUX 1:16
Supply voltage	+5 V
Power consumption	11 mW
Illumination mode	reflective/trans-flective
Front surface	glossy
Character generator	built in
Data interface	parallel 4 or 8 bits

DISPLAY MODE

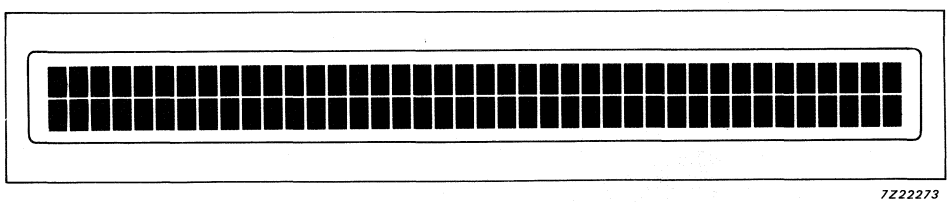
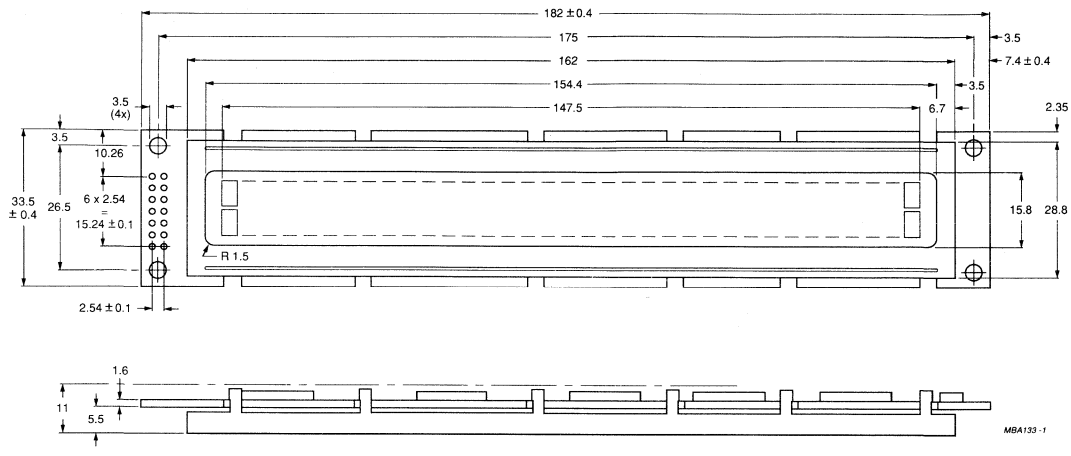


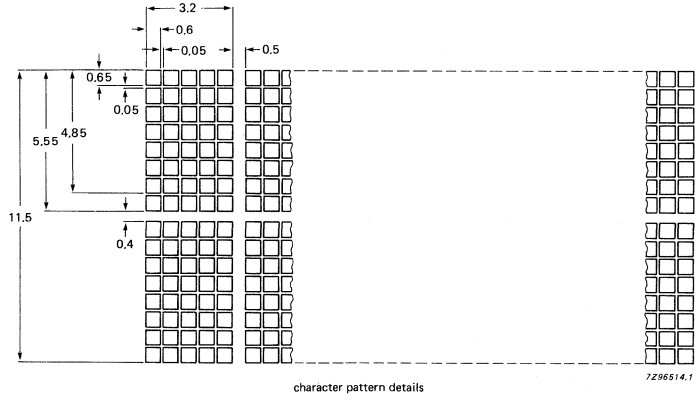
Fig.1 40-character, 2-line LCD module.

TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	VIEWING DIRECTION	TO BE USED WITH EL BACKLIGHT
LTN243R-10	reflective	6 o'clock	–
LTN243F-10	transflective	6 o'clock	LXL242-G
LTN243R-50	reflective	12 o'clock	–

MECHANICAL DATA





character pattern details

Fig.2 Outline dimensions.

Liquid crystal display LTN243

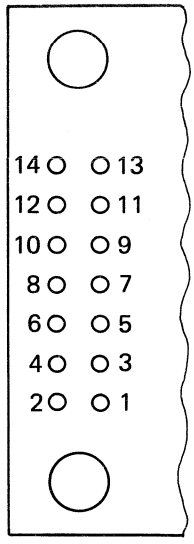


Fig.3 Pin configuration.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	V_{SS}	ground
2	V_{DD}	power supply (logic)
3	V_O	contrast adjustment voltage
4	RS	register select
5	R/W	read/write
6	E	enable
7	D0	I/O data LSB
8	D1	I/O data 2nd bit
9	D2	I/O data 3rd bit
10	D3	I/O data 4th bit
11	D4	I/O data 5th bit
12	D5	I/O data 6th bit
13	D6	I/O data 7th bit
14	D7	I/O data MSB

Notes to pin description

1. Contrast is adjusted by varying the voltage V_O between 0 and 5 V.
2. D7 doubles as busy flag.
3. When the module is interfaced with a microprocessor with 4-bit parallel outputs, pins D0 to D3 are not used.

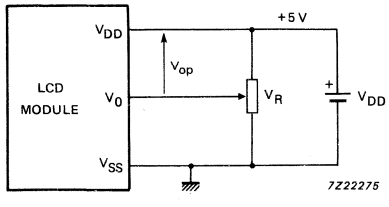


Fig.4 Power supply.

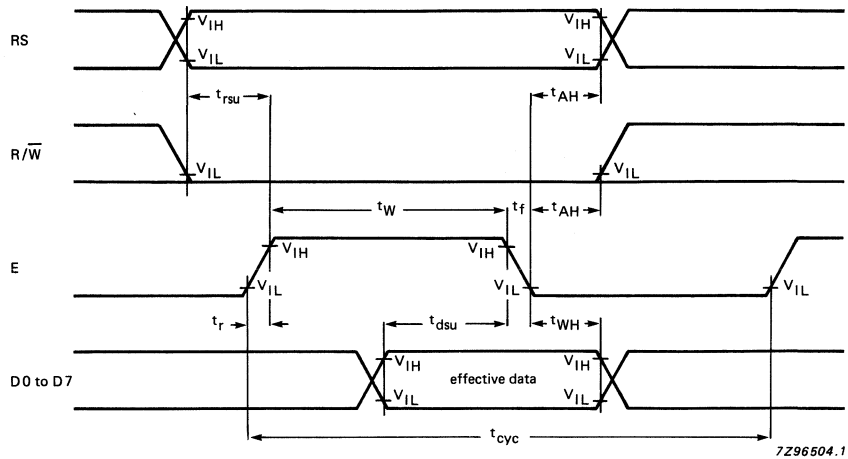


Fig.5 Timing waveforms (write operation).

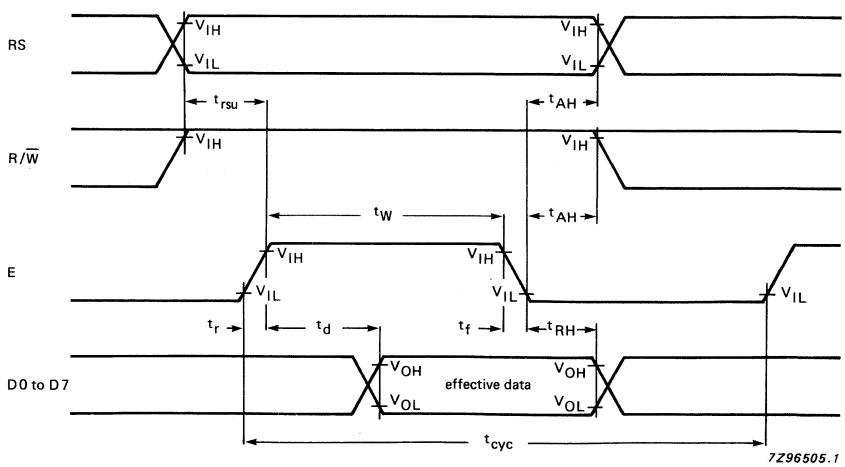


Fig.6 Timing waveforms (read operation).

Liquid crystal display LTN243

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{DD}	−0.3	–	7.0	V
LCD drive voltage (V_{DD}-V_O)	V_{op}	0	–	9.0	V
Input voltage	V_I	−0.3	–	V_{DD}+0.3	V
Storage temperature	T_{stg}	−25	–	+70	°C
Operating ambient temperature	T_{amb}	0	–	+50	°C

OPERATING CHARACTERISTICS

T_{amb} = 25 °C; V_{DD} = 5 V; all voltages refer to V_{SS}; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (logic)	V_{DD}-V_{SS}	4.75	5.0	5.25	V
Contrast adjustment voltage	V_O	–	0.6	–	V
Temperature compensation of V_O	TC	–	−14	–	mV/°C
LOW level input voltage	V_{IL}	−0.3	–	0.6	V
HIGH level input voltage	V_{IH}	2.2	–	V_{DD}	V
LOW level output voltage -I_{OL} = 1.2 mA	V_{OL}	–	–	0.4	V
HIGH level output voltage -I_{OH} = 0.205 mA	V_{OH}	2.4	–	–	V
Input leakage current	I_I	–	–	1.0	µA
Internal oscillating frequency	f_{OSC}	–	140	–	kHz
Supply current (logic)	I_{DD}	–	2.2	4	mA
Power dissipation	P_d	–	11	20	mW

TIMING CHARACTERISTICS

T_{amb} = 0 to 50 °C, V_{DD} = 5 V +/− 5%, unless otherwise specified.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Enable cycle time	t_{cyc}	1000	–	–	ns
Enable pulse width	t_W	450	–	–	ns
Rise time	t_r	–	–	25	ns
Fall time	t_f	–	–	25	ns
Register select set-up time	t_{rsu}	140	–	–	ns
Read and write set-up time	t_{su}	140	–	–	ns
Data set-up time	t_{dsu}	195	–	–	ns
Data delay time	t_d	–	–	320	ns
Address hold time	t_{AH}	10	–	–	ns
Data hold time write	t_{WH}	10	–	–	ns
Data hold time read	t_{RH}	20	–	–	ns

ELECTRO-OPTICAL CHARACTERISTICS

T_{amb} = 25 °C, $V_{DD} = V_{DD\ typ}$, α = 10°, $\phi = \phi_{opt}$, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	TYP.	MAX.	UNIT
Response times	t_{on}	T_{amb} = 0 °C T_{amb} = 25 °C T_{amb} = 50 °C	380 110 45	760 220 90	ms ms ms
	t_{off}	T_{amb} = 0 °C T_{amb} = 25 °C T_{amb} = 50 °C	470 110 45	940 220 90	ms ms ms
Viewing Angles (contrast ratio CR > 3)	α_{opt} α_2-α_1	reflective types LTN243R/F	35 25	– –	° °
	α_{opt} α_2-α_1	transmissive types LTN243F	35 20	– –	° °

For definitions of response times, viewing angles and contrast ratio refer to notes 1 to 3

Table 1 Instruction set

INSTRUCTION \ ADDRESSES	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Display clear	0	0	0	0	0	0	0	0	0	1
Cursor home	0	0	0	0	0	0	0	0	1	*
Entry mode set	0	0	0	0	0	0	0	1	I/D	S
Display on/off control	0	0	0	0	0	0	1	D	C	B
Cursor display shift	0	0	0	0	0	1	S/C	R/L	*	*
Function set	0	0	0	0	1	DL	1	0	*	*
CG RAM address set	0	0	0	1	A_{CG}					
DD RAM address set	0	0	1	A_{DD}						
Busy flag/address read	0	1	BF	AC						
CG RAM/DD RAM data write	1	0	write data							
CG RAM/DD RAM data read	1	1	read data							

Notes:

I/D	= 1:increment	I/D	= 0:decrement
S	= 1:display shift	S	= 0:display freeze
D	= 1:display on	D	= 0:display off
C	= 1:cursor on	C	= 0:cursor off
B	= 1:character at cursor position blinks	B	= 0:character at cursor position does not blink
S/C	= 1:display shift	S/C	= 0:cursor move
R/L	= 1:right shift	R/L	= 0:left shift
DL	= 1:8 bits	DL	= 0:4 bits
BF	= 1:during internal operation	BF	= 0:end of internal operation

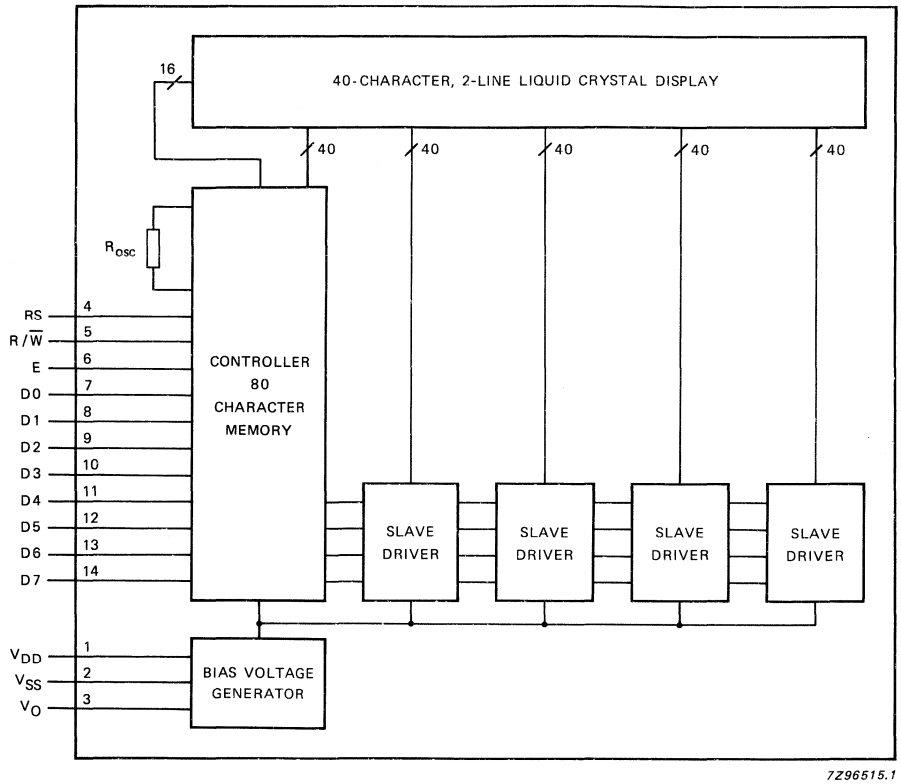


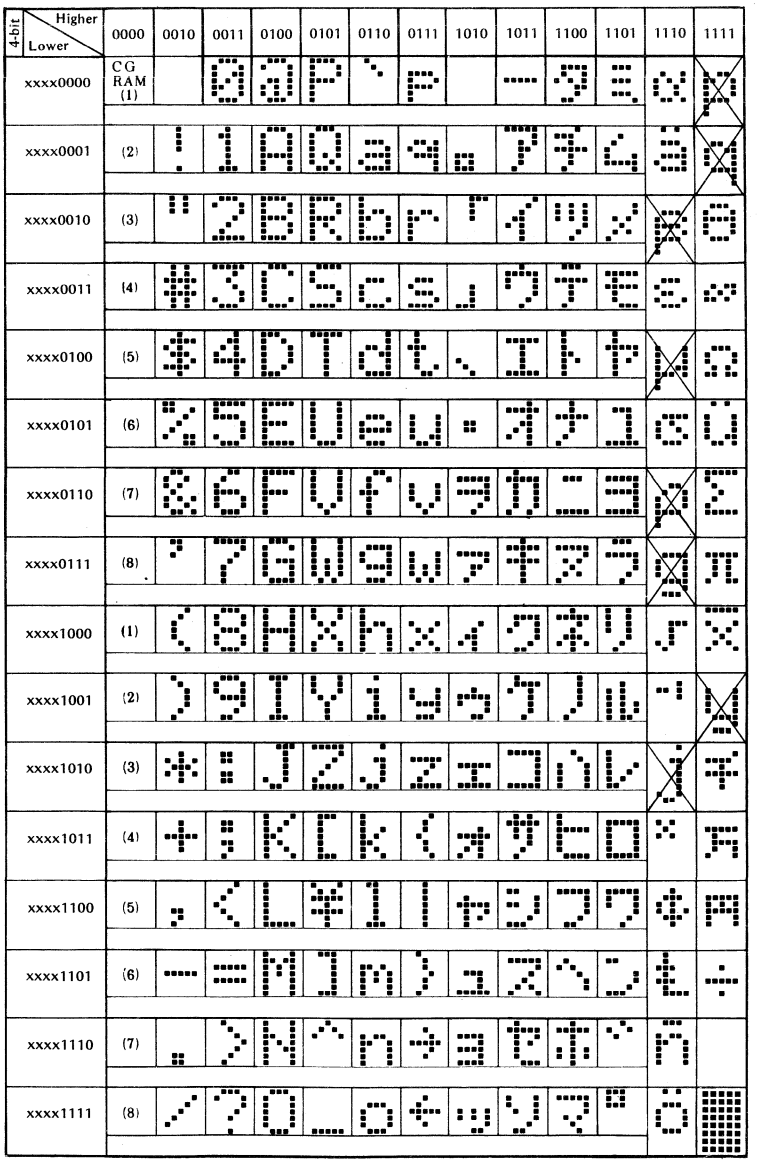
Fig.7 Functional block diagram.

Table 2 Display position and DD RAM address (HEX)

	display position										
digit	1	2	3	4	5	6	7	8	9	39	40
line 1	00_H	01_H	02_H	03_H	04_H	05_H	06_H	07_H	08_H	26_H	27_H
line 2	40_H	41_H	42_H	43_H	44_H	45_H	46_H	47_H	48_H	66_H	67_H

7Z22276 DD RAM address (HEX)

Table 3 Input codes vs character pattern



Liquid crystal display LTN243

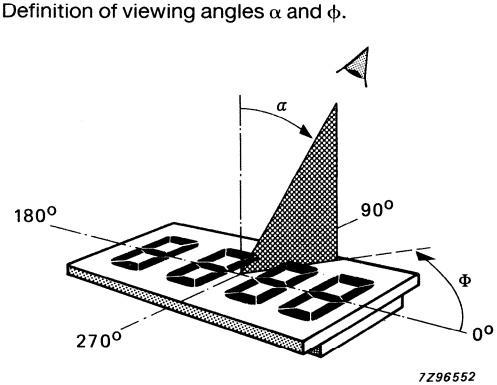
Note 1 Definition of contrast ratio (C_R).

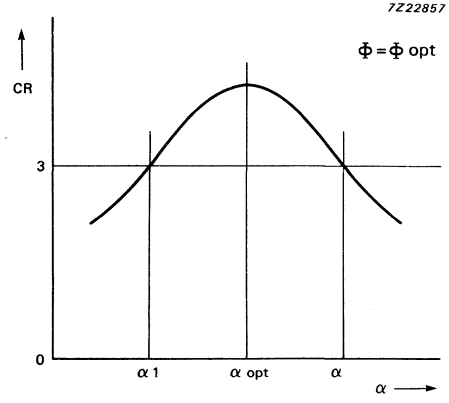
in positive image mode: $CR = \frac{B_{off}}{B_{on}}$

in negative image mode: $CR = \frac{B_{on}}{B_{off}}$

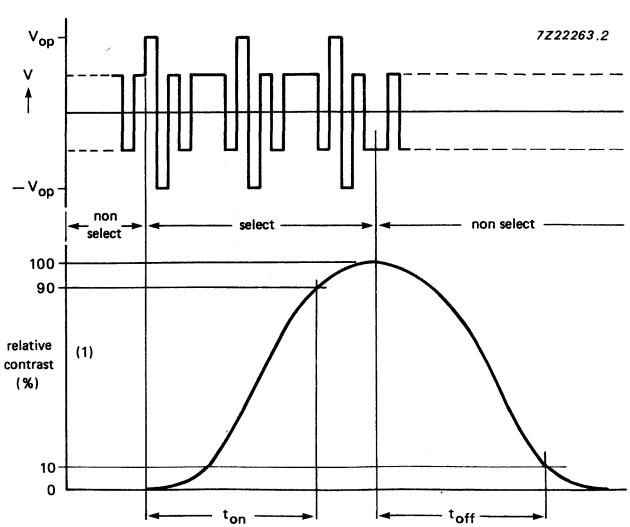
B_{on} is the brightness of selected segments
B_{off} is the brightness of non-selected segments

Note 2 Definition of viewing angles α and ϕ.





Note 3 Definition of response times.



1) measured at $\alpha = 10°$

EL backlights

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LXL111-G
Electro-luminescent backlight panel

DEVICE DESCRIPTION

The LXL111-G is an electro-luminescent backlight panel which has to be used in the LTN111 module. The emitted colour is green.

QUICK REFERENCE DATA

Lit area dimensions	11.5 x 62 mm
Supply voltage	110 V RMS
Supply frequency	500 Hz
Colour	green
Connection	solderable leads

MECHANICAL DATA

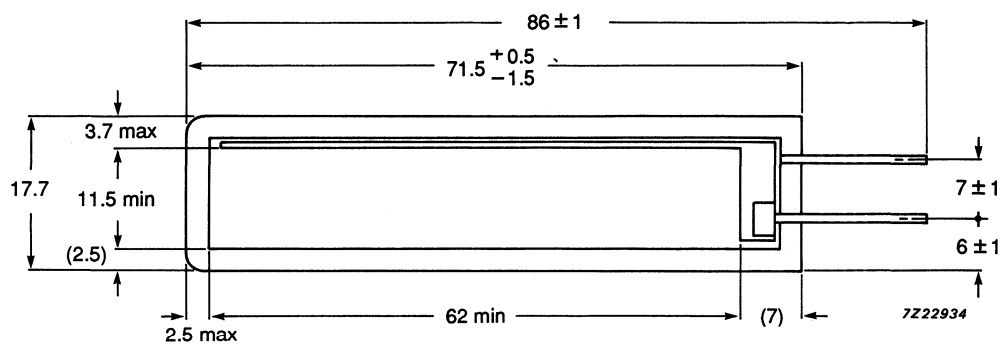


Fig.1 Panel outline.

Pin connections

The device should be soldered onto the PC-board of the module.

Electro-luminescent backlight panel LXL111-G

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Supply voltage, t = 60 s max.	V_S	max.	130	V RMS
Frequency				
V_S = 100 V RMS, t = 60 s max.	F	max.	1500	Hz
Isolation voltage				
pin to film, t = 60 s max.	V_{IS}	max.	1000	V
Storage temperature range				
note 1	T_{stg}		−20 to +40	°C
note 2	T_{stg}		+40 to +60	°C
Ambient operating temperature range				
note 1	T_{amb}		0 to +40	°C
note 2	T_{amb}		+40 to +50	°C

CHARACTERISTICS

T_{amb} = 25 °C, V_S = 110 V RMS, f = 500 Hz, in dark room, unless otherwise specified

Luminance	L	typ.	90	cd/m^2
Supply current	I_S	typ.	2	mA
Chromaticity (colour = green)	X	typ.	0.21	
	Y	typ.	0.51	

Notes:

1. Condition: relative humidity < 95%
2. Condition: absolute humidity < T_{amb} = 40 °C, 95% RH

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LXL211-G

Electro-luminescent backlight panel

DEVICE DESCRIPTION

The LXL211-G is an electro-luminescent backlight panel which has to be used in the LTN211 module. The emitted colour is green.

QUICK REFERENCE DATA

Lit area dimensions	13.3 x 63.5 mm
Supply voltage	110 V RMS
Supply frequency	500 Hz
Colour	green
Connection	solderable leads

MECHANICAL DATA

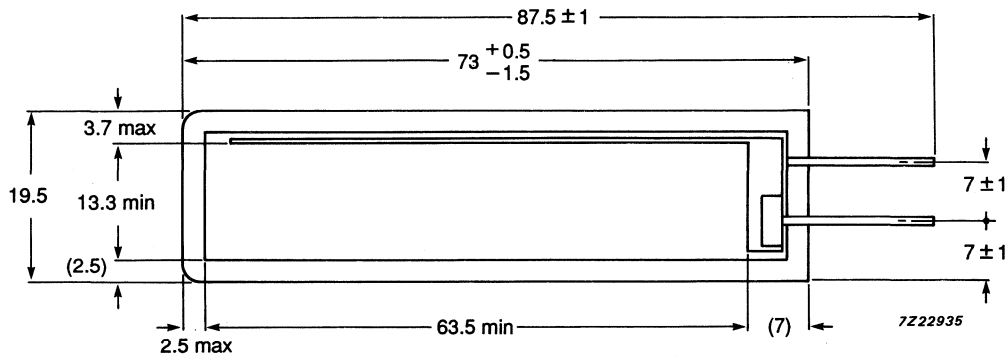


Fig.1 Panel outline.

Pin connections

The device should be soldered onto the PC-board of the module.

Electro-luminescent backlight panel LXL211-G

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Supply voltage, t = 60 s max.	V_S	max.	130	V RMS
Frequency				
V_S = 100 V RMS, t = 60 s max.	F	max.	1500	Hz
Isolation voltage				
pin to film, t = 60 s max.	V_{IS}	max.	1000	V
Storage temperature range				
note 1	T_{stg}		−20 to +40	°C
note 2	T_{stg}		+40 to +60	°C
Ambient operating temperature range				
note 1	T_{amb}		0 to +40	°C
note 2	T_{amb}		+40 to +50	°C

CHARACTERISTICS

T_{amb} = 25 °C, V_S = 110 V RMS, f = 500 Hz, in dark room, unless otherwise specified

Luminance	L	typ.	90	cd/m^2
Supply current	I_S	typ.	2.2	mA
Chromaticity (colour = green)	X	typ.	0.21	
	Y	typ.	0.51	

Notes:

1. Condition: relative humidity < 95%
2. Condition: absolute humidity < T_{amb} = 40 °C, 95% RH

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LXL221-G
Electro-luminescent backlight panel

DEVICE DESCRIPTION

The LXL221-G is an electro-luminescent backlight panel which has to be used in the LTN221/LTN222 modules. The emitted colour is green.

QUICK REFERENCE DATA

Lit area dimensions	22 x 85 mm
Supply voltage	110 V RMS
Supply frequency	500 Hz
Colour	green
Connection	solderable leads

MECHANICAL DATA

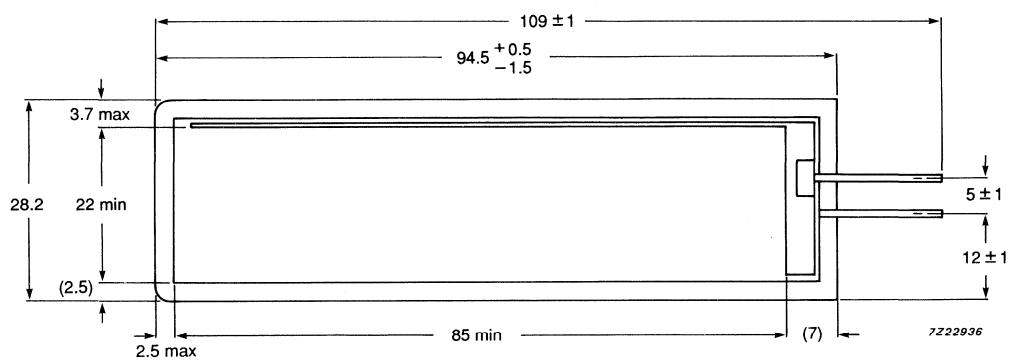


Fig.1 Panel outline.

Pin connections

The device should be soldered onto the PC-board of the module.

Electro-luminescent backlight panel LXL221-G

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Supply voltage, t = 60 s max.	V_S	max.	130	V RMS
Frequency				
V_S = 100 V RMS, t = 60 s max.	F	max.	1500	Hz
Isolation voltage				
pin to film, t = 60 s max.	V_{IS}	max.	1000	V
Storage temperature range				
note 1	T_{stg}		−20 to +40	°C
note 2			+40 to +60	°C
Ambient operating temperature range				
note 1	T_{amb}		0 to +40	°C
note 2	T_{amb}		+40 to +50	°C

CHARACTERISTICS

T_{amb} = 25 °C, V_S = 110 V RMS, f = 500 Hz, in dark room, unless otherwise specified

Luminance	L	typ.	90	cd/m²
Supply current	I_S	typ.	4.3	mA
Chromaticity (colour = green)	X	typ.	0.21	
	Y	typ.	0.51	

Notes:

1. Condition: relative humidity < 95%
2. Condition: absolute humidity < T_{amb} = 40 °C, 95% RH

Philips Components

Data sheet	
status	Product specification
date of issue	July 1990

LXL242-G
Electro-luminescent backlight panel

DEVICE DESCRIPTION

The LXL242-G is an electro-luminescent backlight panel which has to be used in the LTN242 module. The emitted colour is green.

QUICK REFERENCE DATA

Lit area dimensions	15 x 153 mm
Supply voltage	110 V RMS
Supply frequency	500 Hz
Colour	green
Connection	solderable leads

MECHANICAL DATA

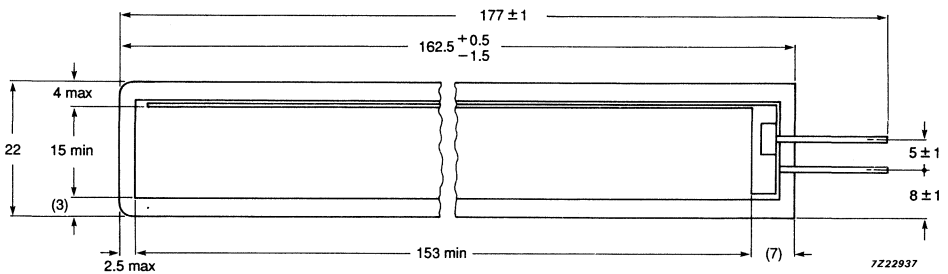


Fig.1 Panel outline.

Pin connections

The device should be soldered onto the PC-board of the module.

Electro-luminescent backlight panel LXL242-G

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Supply voltage, t = 60 s max.	V_S	max.	130	V RMS
Frequency				
V_S = 100 V RMS, t = 60 s max.	F	max.	1500	Hz
Isolation voltage				
pin to film, t = 60 s max.	V_{IS}	max.	1000	V
Storage temperature range				
note 1	T_{stg}		−20 to +40	°C
note 2	T_{stg}		+40 to +60	°C
Ambient operating temperature range				
note 1	T_{amb}		0 to +40	°C
note 2	T_{amb}		+40 to +50	°C

CHARACTERISTICS

T_{amb} = 25 °C, V_S = 110 V RMS, f = 500 Hz, in dark room, unless otherwise specified

Luminance	L	typ.	90	cd/m²
Supply current	I_S	typ.	5.1	mA
Chromaticity (colour = green)	X	typ.	0.21	
	Y	typ.	0.51	

Notes:

1. Condition: relative humidity < 95%
2. Condition: absolute humidity < T_{amb} = 40 °C, 95% RH

Driver IC's for LCD

Driver IC's for LCD's — Type number survey

Driver ICs for LCD

TYPE NUMBER	DESCRIPTION	PAGE
PCF2100	C bus control, 40-segments	271
PCF2110	C bus control, 60-segments	271
PCF2111	C bus control, 64-segments	271
PCF2112	C bus control, 32-segments	271
PCF8566	I^2C bus control, 1:2 to 1:4 MUX ratios (24-segments)	287
PCF8576	I^2C bus control, 1:2 to 1:4 MUX ratios (40-segments)	321
PCF8577	I^2C bus control, direct drive (32-segments) MUX 1:2 (64-segments)	361
PCF2201	flat panel ROW/COLUMN driver	383
PCF8578	flat panel ROW/COLUMN driver	405
PCF8579	flat panel ROW/COLUMN driver	443
PCF1303T	18-segment bargraph display driver with analog input	477
HEF4754V	18-segment bargraph display driver	483
PC74HC4543	BCD to 7-segment latch/decoder/driver for LCD	489
PC74HCT4543	BCD to 7-segment latch/decoder/driver for LCD	489
HEF4543B	BCD to 7-segment latch/decoder/driver for LCD and LED	499

LCD DRIVER

GENERAL DESCRIPTION

The members of the PCF21XX family are single chip, silicon gate CMOS circuits. A three-line bus (CBUS) structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- Supply voltage 2,25 to 6,5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possibility
- Power-on reset clear

	PCF2100	PCF2110	PCF2111	PCF2112
• LCD segments	40	60	64	32
• LED segments	–	2	–	–
• Multiplex rate	1:2	1:2	1:2	1:1
• Word length	22 bit	34 bit	34 bit	34 bit

PACKAGE OUTLINES

PCF2100P: 28-lead DIL; plastic (SOT117).

PCF2110P:
PCF2111P: 40-lead DIL; plastic (SOT129).
PCF2112P:

PCF2100T: 28-lead mini-pack; plastic (SO28; SOT136A).

PCF2110T:
PCF2111T: 40-lead mini-pack; plastic (VSO40; SOT158A).
PCF2112T:

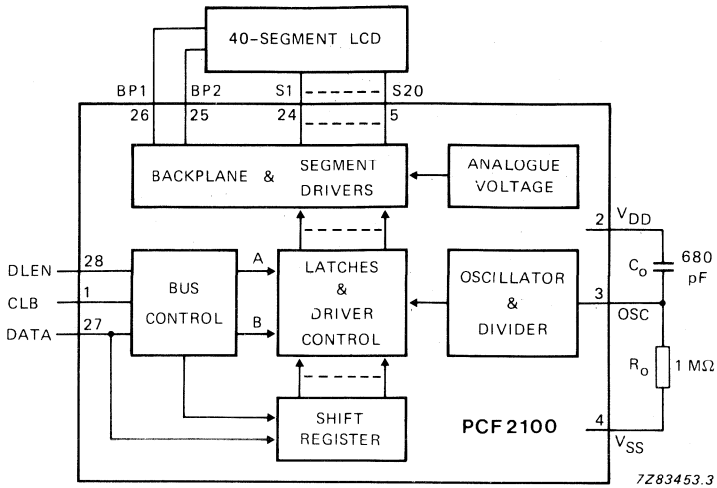


Fig. 1 Block diagram; PCF2100

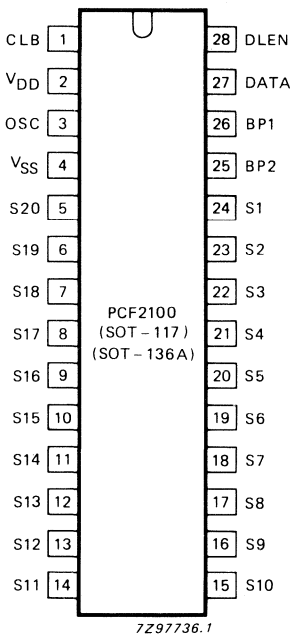


Fig. 2 Pinning diagram; PCF2100

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)	
3	OSC	oscillator input	
27	DATA	data line	CBUS
28	DLEN	data line enable	CBUS

Outputs

5 to 24	S20 to S1	LCD driver outputs
25	BP2	backplane drivers (commons of LCD)
26	BP1	backplane drivers (commons of LCD)

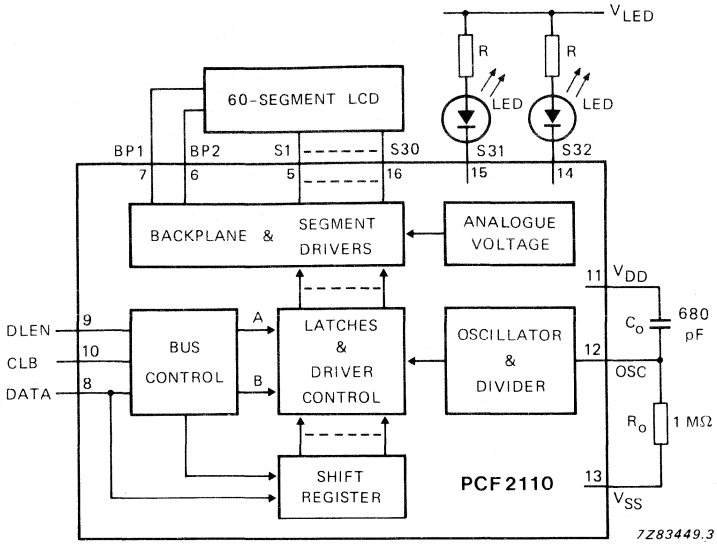


Fig. 3 Block diagram; PCF2110 (SOT-129).

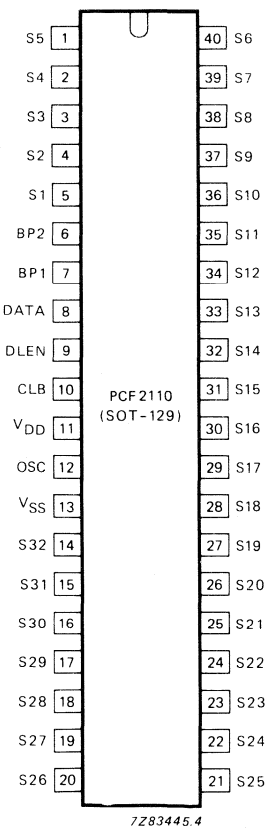


Fig. 4 Pinning diagram; PCF2110

DEVELOPMENT DATA

PINNING (SOT-129)

Supply

11	V_{DD}	positive supply
13	V_{SS}	negative supply

Inputs

8	DATA	data line	CBUS
9	DLEN	data line enable	CBUS
10	CLB	clock burst	CBUS
12	OSC	oscillator input	

Outputs

1 to 5	S5 to S1	LCD driver outputs
6	BP2	backplane drivers (commons of LCD)
7	BP1	backplane drivers (commons of LCD)
14	S32	LED driver outputs
15	S31	LED driver outputs
16 to 40	S30 to S6	LCD driver outputs

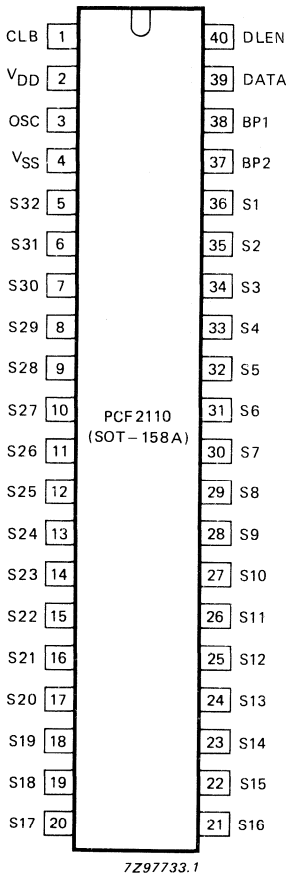


Fig. 5 Pinning diagram; PCF2110

PINNING (SOT-158A)

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)
3	OSC	oscillator input
39	DATA	data line (CBUS)
40	DLEN	data line enable (CBUS)

Outputs

5	S32	LED driver outputs
6	S31	LED driver outputs
7 to 36	S30 to S1	LCD driver outputs
37	BP2	backplane drivers (commons of LCD)
38	BP1	backplane drivers (commons of LCD)

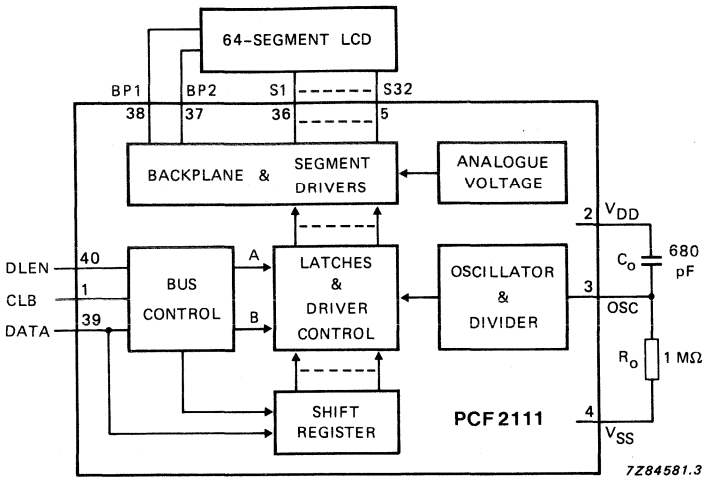


Fig. 6 Block diagram; PCF2111

DEVELOPMENT DATA

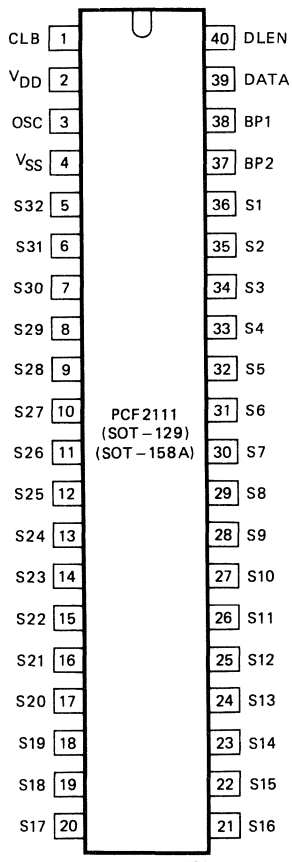


Fig. 7 Pinning diagram; PCF2111

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)	
3	OSC	oscillator input	
39	DATA	data line	CBUS
40	DLEN	data line enable	CBUS

Outputs

5 to 36	S32 to S1	LCD driver outputs
38	BP1	backplane drivers (commons of LCD)
37	BP2	backplane drivers (commons of LCD)

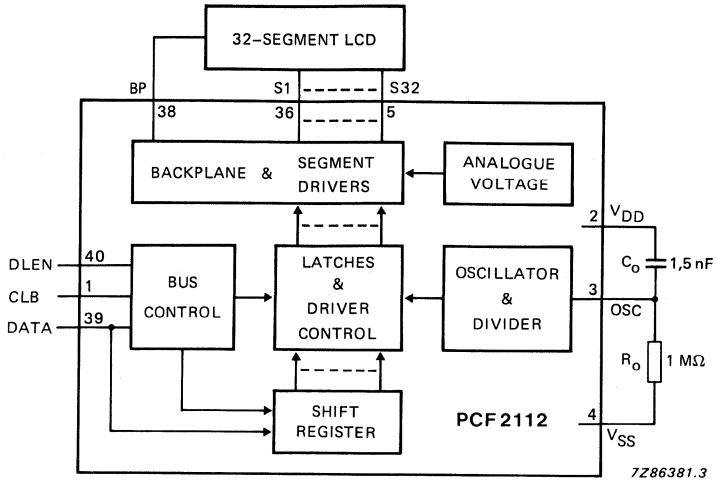


Fig. 8 Block diagram; PCF2112

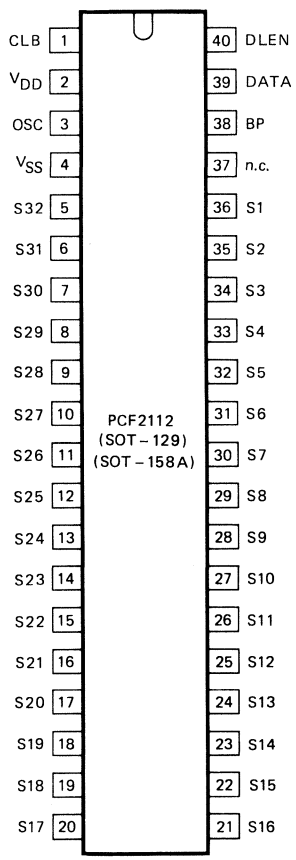


Fig. 9 Pinning diagram; PCF2112

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)	
3	OSC	oscillator input	
39	DATA	data line	CBUS
40	DLEN	data line enable	CBUS

Outputs

5 to 36	S32 to S1	LCD driver outputs
38	BP	backplane driver (common of LCD)
37	n.c.	not connected

FUNCTIONAL DESCRIPTION

An LCD segment or LED output is activated when the corresponding DATA-bit is HIGH.

PCF2100

When DATA-bit 21 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 21 LOW, the B-latches (BP2) are loaded. CLB-pulse 23 transfers data from the shift register to the selected latches.

PCF2110

When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. Bits 31 and 32 contain the LED output information. With DATA-bit 33 LOW, the B-latches (BP2) are loaded and bits 31 and 32 are ignored. CLB-pulse 35 transfers data from the shift register to the selected latches.

PCF2111

When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 33 LOW, the B-latches (BP2) are loaded. CLB-pulse 35 transfers data from the shift register to the selected latches.

PCF2112

When DATA-bit 33 is HIGH, the latches are loaded. CLB-pulse 35 transfers data from the shift register to the selected latches.

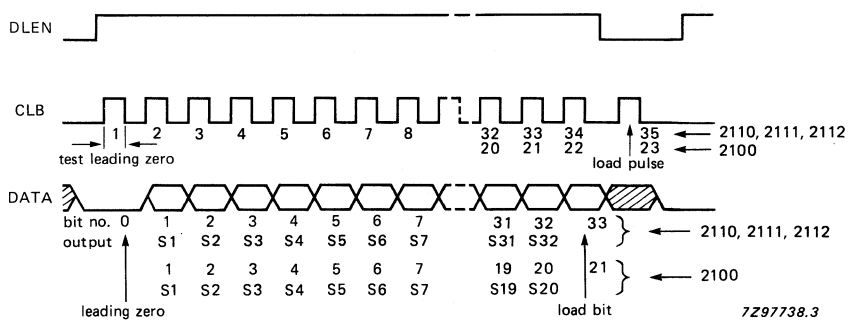


Fig. 10 CBUS data format.

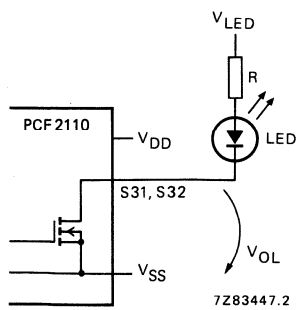


Fig. 11 LED driver circuitry.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN LOW) and the driver is ready to receive new data.

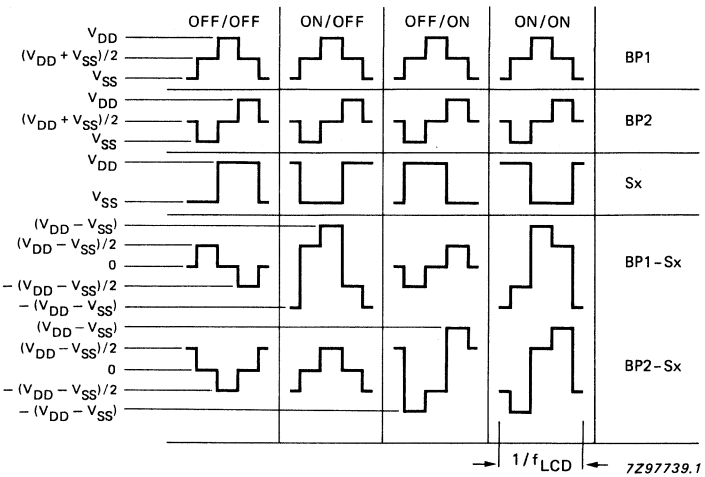


Fig. 12 Timing diagram (except PCF2112).

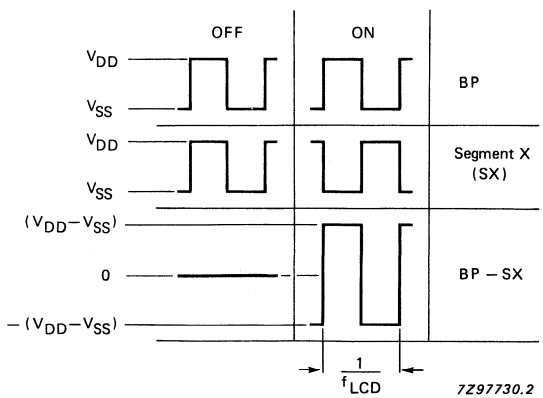


Fig. 13 Timing diagram for PCF2112.

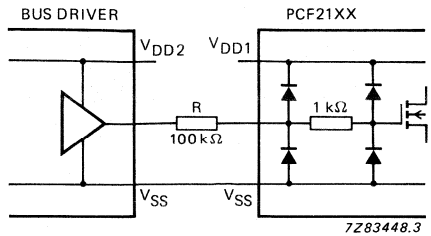
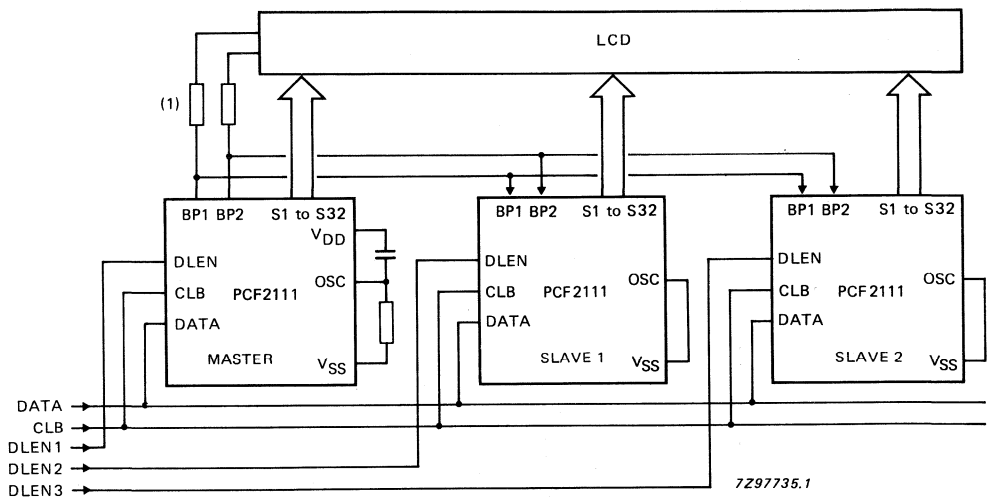


Fig. 14 Input circuitry.

Note to Fig. 14

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0{,}5$ V, a resistor should be inserted to reduce the current flowing through the input protection. Maximum input current $\leqslant 40\,\mu$A.



(1) In the slave mode, the serial resistors between BP1 and BP2 of the PCF2111 and the backplane of the LCD must be $> 2{,}7$ kΩ. In most applications the resistance of the interconnection to the LCD already has a higher value.

Fig. 15 Diagram showing expansion possibility (using PCF2111).

Note to Fig. 15

By connecting OSC to V_{SS} the BP-pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several members of the PCF21XX family up to the BP drive capability of the master. The PCF2112 can only function as a master for other PCF2112s.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0,5	9,0	V
Input voltage range DLEN, CLB, DATA and OSC		V_I	V_{SS}−0,5	V_{DD}+0,5	V
Output voltage range BP1, BP2 and S1 to S32		V_O	V_{SS}−0,5	V_{DD}+0,5	V
Supply current		$\pm I_{DD}$, $\pm I_{SS}$	−	50	mA
DC input current		$\pm I_I$	−	20	mA
DC output current		$\pm I_O$	−	25	mA
Total power dissipation per package	note 1	P_{tot}	−	500	mW
Power dissipation per output		P_O	−	100	mW
Storage temperature range		T_{stg}	−65	+150	°C

Note to the ratings

1. Derate by 7,7 mW/°C when $T_{amb} > 60$ °C.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2,25 to 6,5 V; T_{amb} = −40 to + 85 °C; R_O = 1 MΩ; C_O = 680 pF; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	2,25	–	6,5	V
Supply current	note 1	I_{DD1}	–	20	50	μA
Supply current	note 1; T_{amb} = −25 to + 85 °C	I_{DD2}	–	20	30	μA
Power-on reset level	note 2	V_{POR}	–	1,0	1,4	V
Inputs CLB, DATA DLEN						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,0	–	–	V
Leakage current	$V_I = V_{SS}$ or V_{DD}	$\pm I_I$	–	–	1	μA
Input capacitance	note 3	C_I	–	–	10	pF
Input OSC						
Oscillator start-up current	$V_I = V_{SS}$	I_{OSC}	0,5	1,2	5,0	μA
LCD outputs						
DC component of backplane drivers		$\pm V_{BP}$	–	20	–	mV
Backplane driver output impedance	note 4; V_{DD} = 5 V	R_{BP}	–	0,5	5	kΩ
Segment driver output impedance	note 4; V_{DD} = 5 V	R_S	–	1	7	kΩ
LED outputs (S31 and S32 in PCF2110)						
Output current LOW	V_{OL}=0,4 V; V_{DD}=5 V	I_{OL}	8	14	–	mA
Output leakage current	$V_O = V_{DD}$	$\pm I_O$	–	–	1	μA
Load current		I_{LED}	–	–	20	mA

DEVELOPMENT DATA

AC CHARACTERISTICS (note 5)

V_{SS} = 0 V; V_{DD} = 2,25 to 6,5 V; T_{amb} = −40 to + 85 °C; R_O = 1 MΩ; C_O = 680 pF; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs CLB, DATA DLEN						
Data set-up time		t_{SUDA}	3	–	–	μs
Data hold time		t_{HDDA}	3	–	–	μs
Leading zero set-up time		t_{SULZ}	3	–	–	μs
Enable set-up time		t_{SUEN}	1	–	–	μs
Disable set-up time		t_{SUDI}	2	–	–	μs
Load pulse set-up time		t_{SULD}	2,5	–	–	μs
Busy time		t_{BUSY}	3	–	–	μs
CLB HIGH time		t_{WH}	1	–	–	μs
CLB LOW time		t_{WL}	5	–	–	μs
CLB period		t_{CLB}	10	–	–	μs
Rise and fall times		t_r, t_f	–	–	10	μs
LCD timing						
LCD frame frequency		f_{LCD}	60	75	100	Hz
LCD frame frequency for PCF2112	C_O = 1,5 nF	f_{LCD}	30	35	50	Hz
Transfer time with test loads	V_{DD} = 5 V	t_{BS}	–	20	100	μs
Driver delay with test loads	V_{DD} = 5 V	t_{PLCD}	–	20	100	μs

Notes to the characteristics

1. Outputs open; CBUS inactive.
2. Resets all logic, when $V_{DD} < V_{POR}$.
3. Periodically sampled (not 100% tested).
4. Outputs measured one at a time.
5. All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

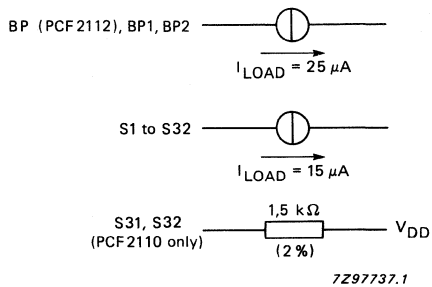
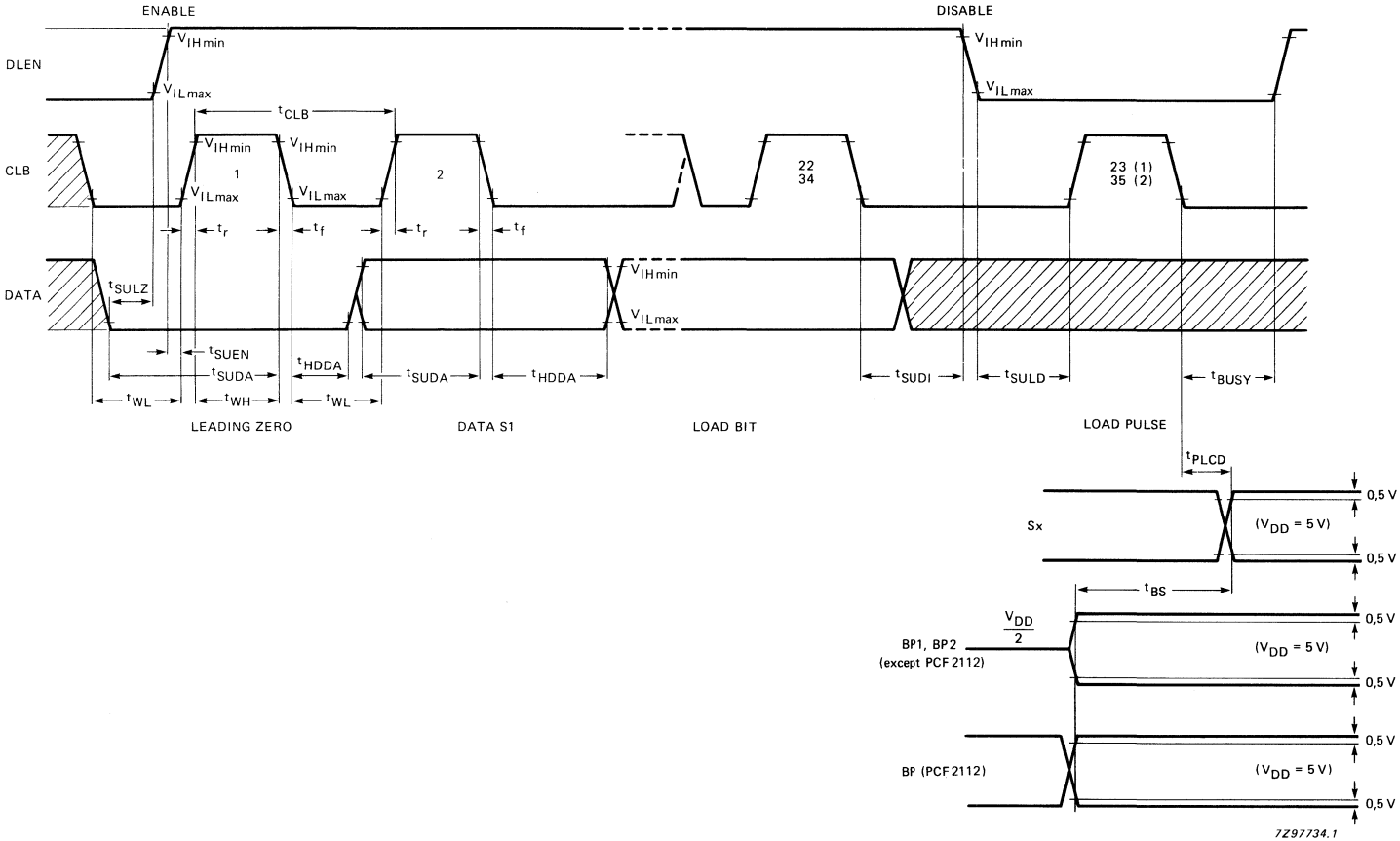


Fig. 16 Test loads.



(1) Load pulse 23 (for PCF2100).
(2) Load pulse 35 (for PCF2110, PCD2111 and PCF2112; see Fig. 10).

Fig. 17 CBUS timing.

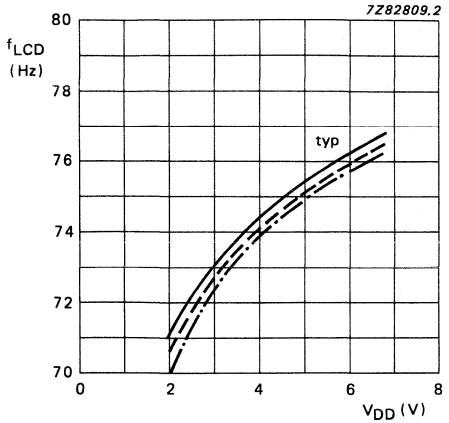


Fig. 18 Displays frequency as a function of supply voltage; C_O = 680 pF (except PCF2112).
——— T_{amb} = –40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

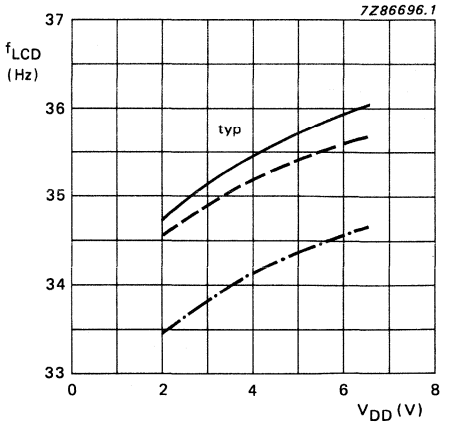


Fig. 19 Display frequency as a function of supply voltage; C_O = 1,5 nF (except PCF2112).
——— T_{amb} = –40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

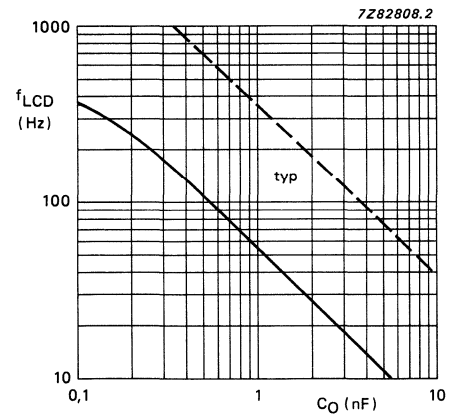


Fig. 20 Display frequency as a function of R_O and C_O; T_{amb} = + 25 °C; V_{DD} = 5 V.
——— R_O = 1 MΩ;
– – – – R_O = 100 kΩ.

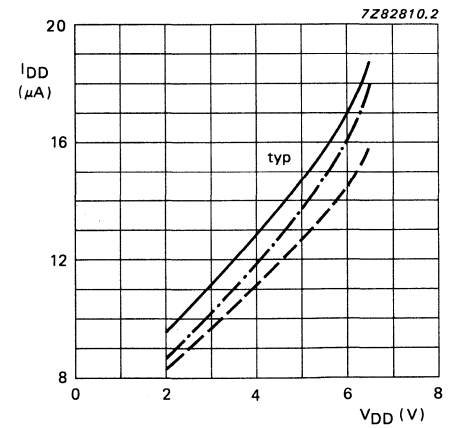


Fig. 21 Supply current as a function of supply voltage.
——— T_{amb} = –40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

DEVELOPMENT DATA

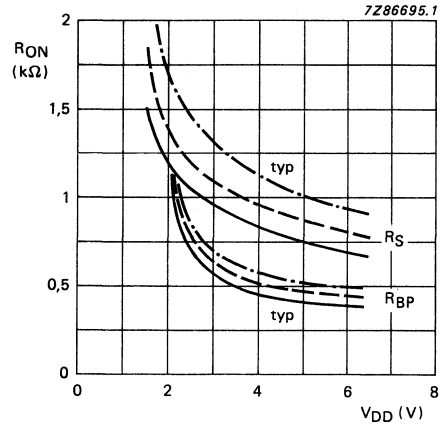


Fig. 22 Output resistance of backplane and segments.
——— T_{amb} = –40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

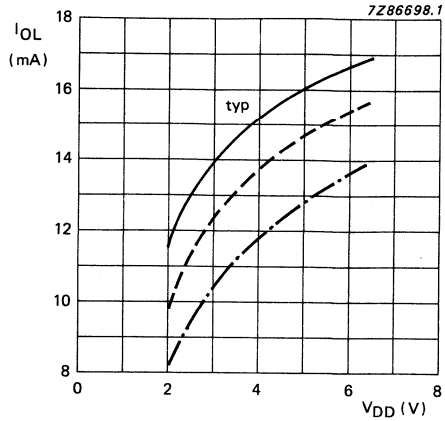


Fig. 23 Output current as a function of supply voltage (only PCF2112).
——— T_{amb} = –40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2,5 V to 6 V power supply range
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40-lead plastic mini-pack (VSO-40; SOT-158A)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8566P: 40-lead DIL; plastic (SOT129).
PCF8566T: 40-lead mini-pack (VSO40; SOT158A).

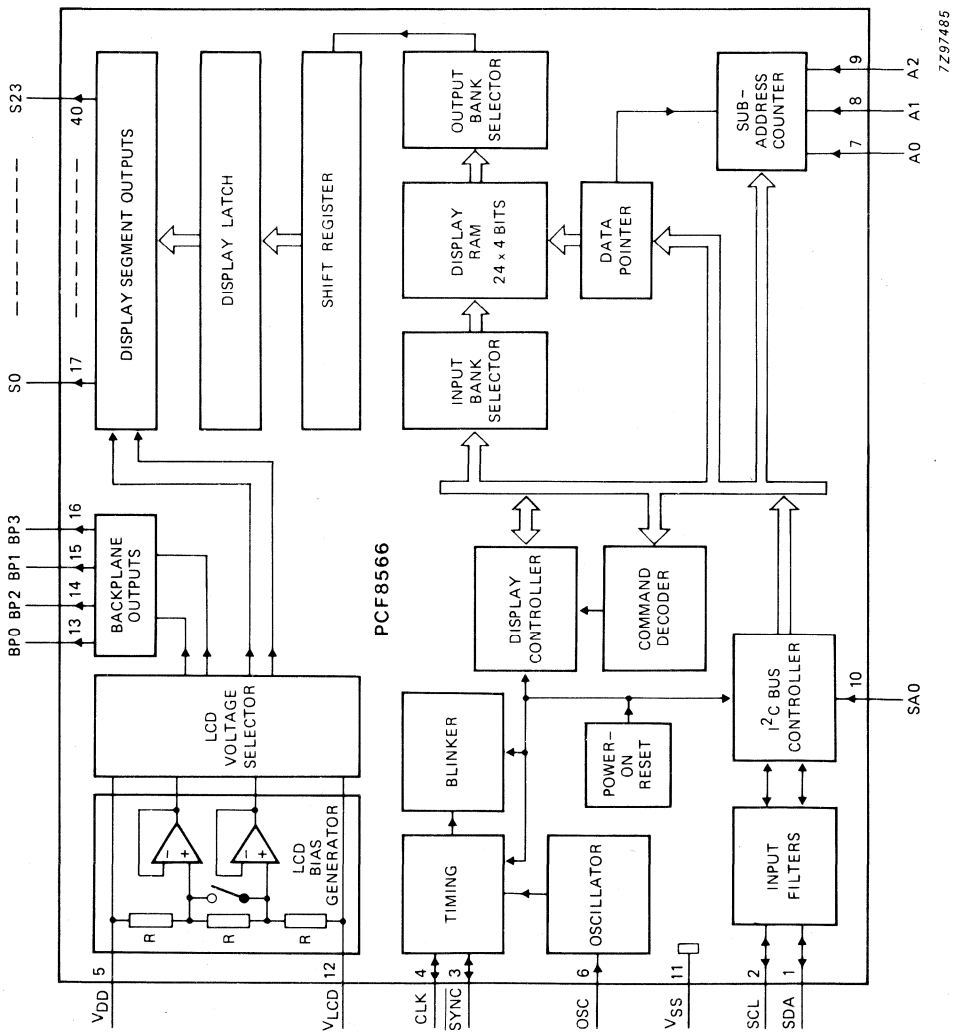


Fig. 1 Block diagram.

DEVELOPMENT DATA

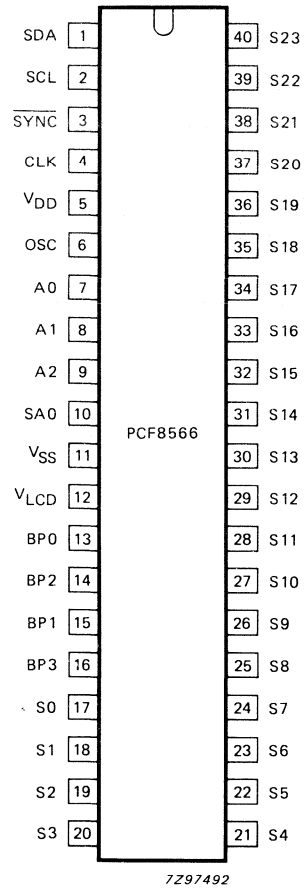


Fig. 2 Pinning diagram.

PINNING

1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{SYNC}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I^2C bus subaddress inputs
8	A1	
9	A2	
10	SA0	I^2C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	
15	BP1	
16	BP3	
17 to 40	S0 to S23	LCD segment outputs

FUNCTIONAL DESCRIPTION

The PCF8566 is a versatile peripheral device designed to interface any microprocessor to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 24 segments. The display configurations possible with the PCF8566 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active back-plane outputs	no. of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	96	12 digits + 12 indicator symbols	6 characters + 12 indicator symbols	96 dots (4 x 24)
3	72	9 digits + 9 indicator symbols	4 characters + 16 indicator symbols	72 dots (3 x 24)
2	48	6 digits + 6 indicator symbols	3 characters + 6 indicator symbols	48 dots (2 x 24)
1	24	3 digits + 3 indicator symbols	1 characters + 10 indicator symbols	24 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig. 3. The host microprocessor/microcontroller maintains the two-line I^2C bus communication channel with the PCF8566. The internal oscillator is selected by tying OSC (pin 6) to V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

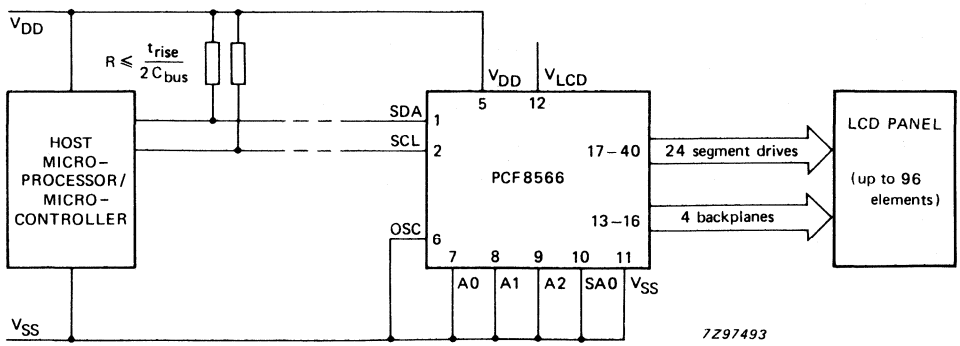


Fig. 3 Typical system configuration.

Power-on reset

At power-on the PCF8566 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0{,}354$	$\sqrt{10}/4 = 0{,}791$	$\sqrt{5} = 2{,}236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{5}/3 = 0{,}745$	$\sqrt{5} = 2{,}236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{33}/9 = 0{,}638$	$\sqrt{33}/3 = 1{,}915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{3}/3 = 0{,}577$	$\sqrt{3} = 1{,}732$

DEVELOPMENT DATA

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\ V_{th}$.

Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1{,}732$ for 1 : 3 multiplex or $\sqrt{21}/3 = 1{,}528$ for 1 : 4 multiplex). The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\ V_{off(rms)} = 2{,}449\ V_{off(rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\ V_{off(rms)} = 2{,}309\ V_{off(rms)}$

These compare with $V_{op} = 3\ V_{off(rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig. 4.

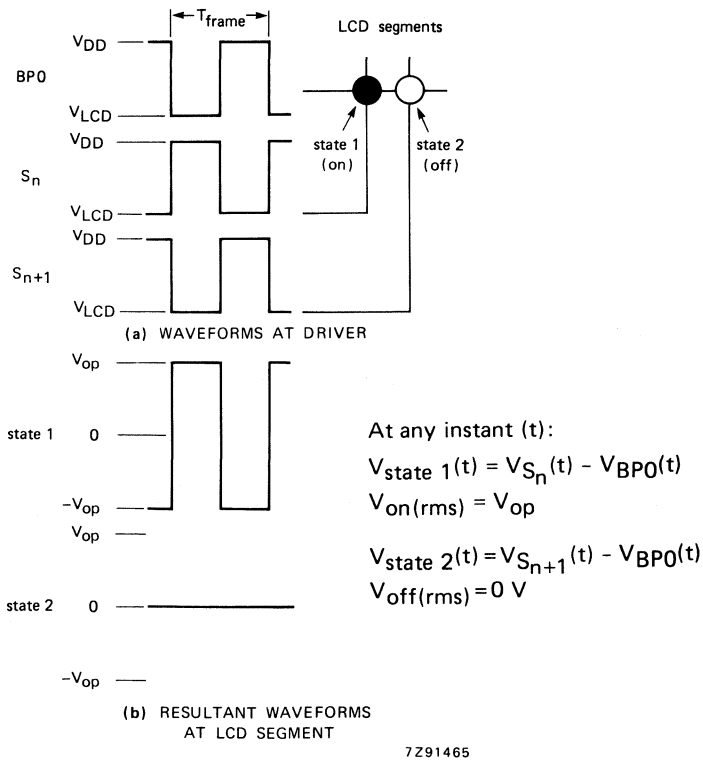


Fig. 4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8566 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

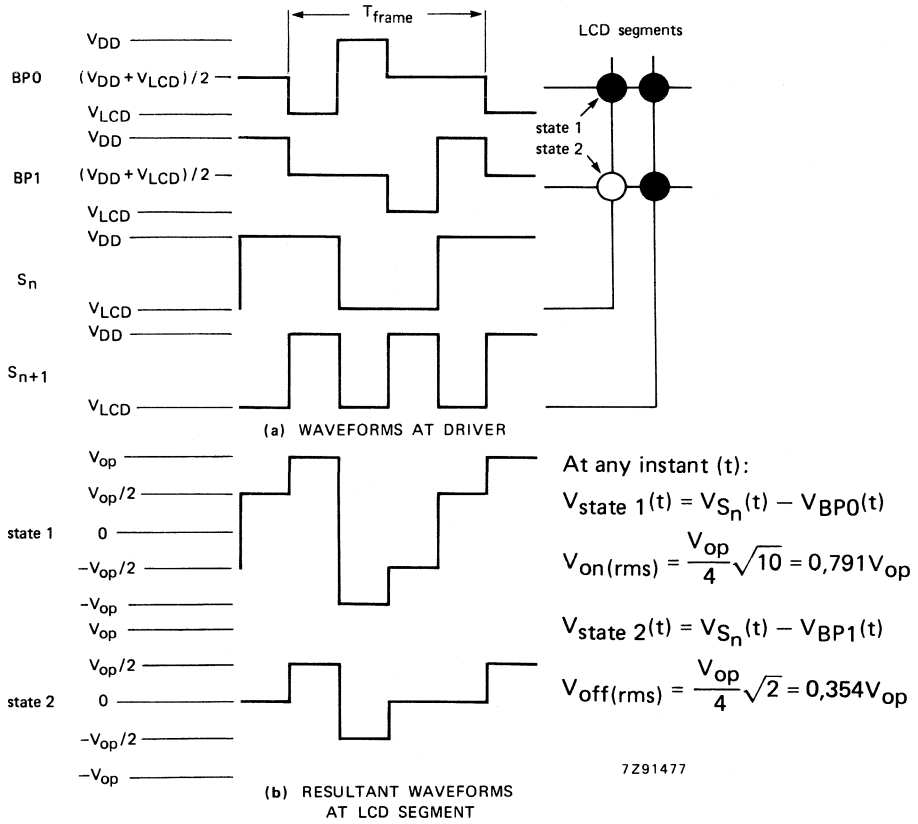


Fig. 5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

DEVELOPMENT DATA

LCD drive mode waveforms (continued)

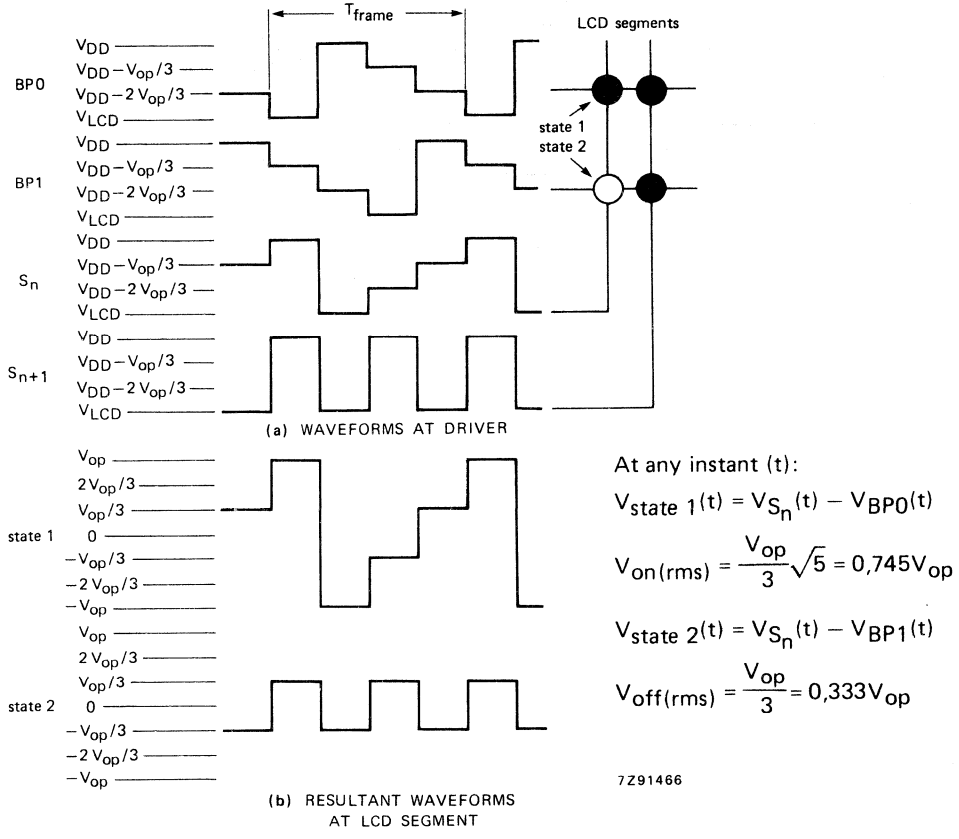


Fig. 6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive wavefront for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

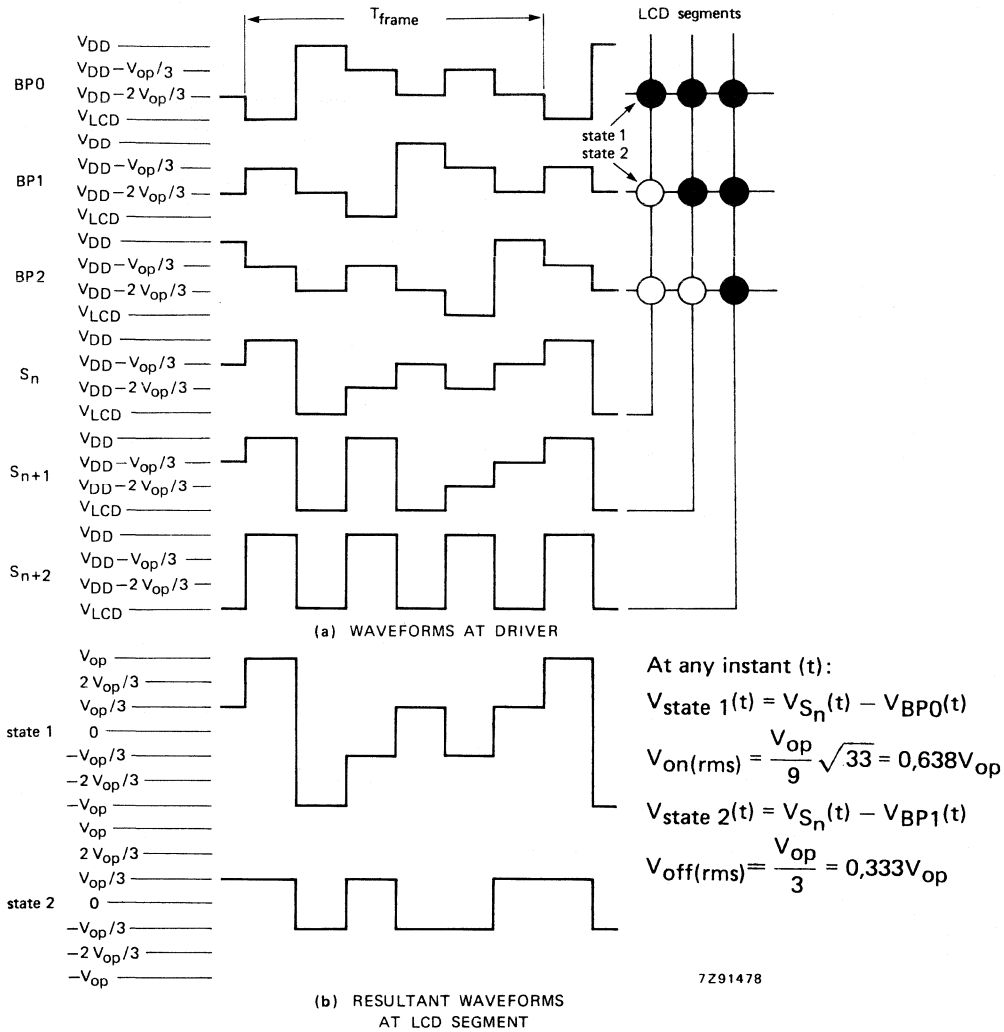


Fig. 7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

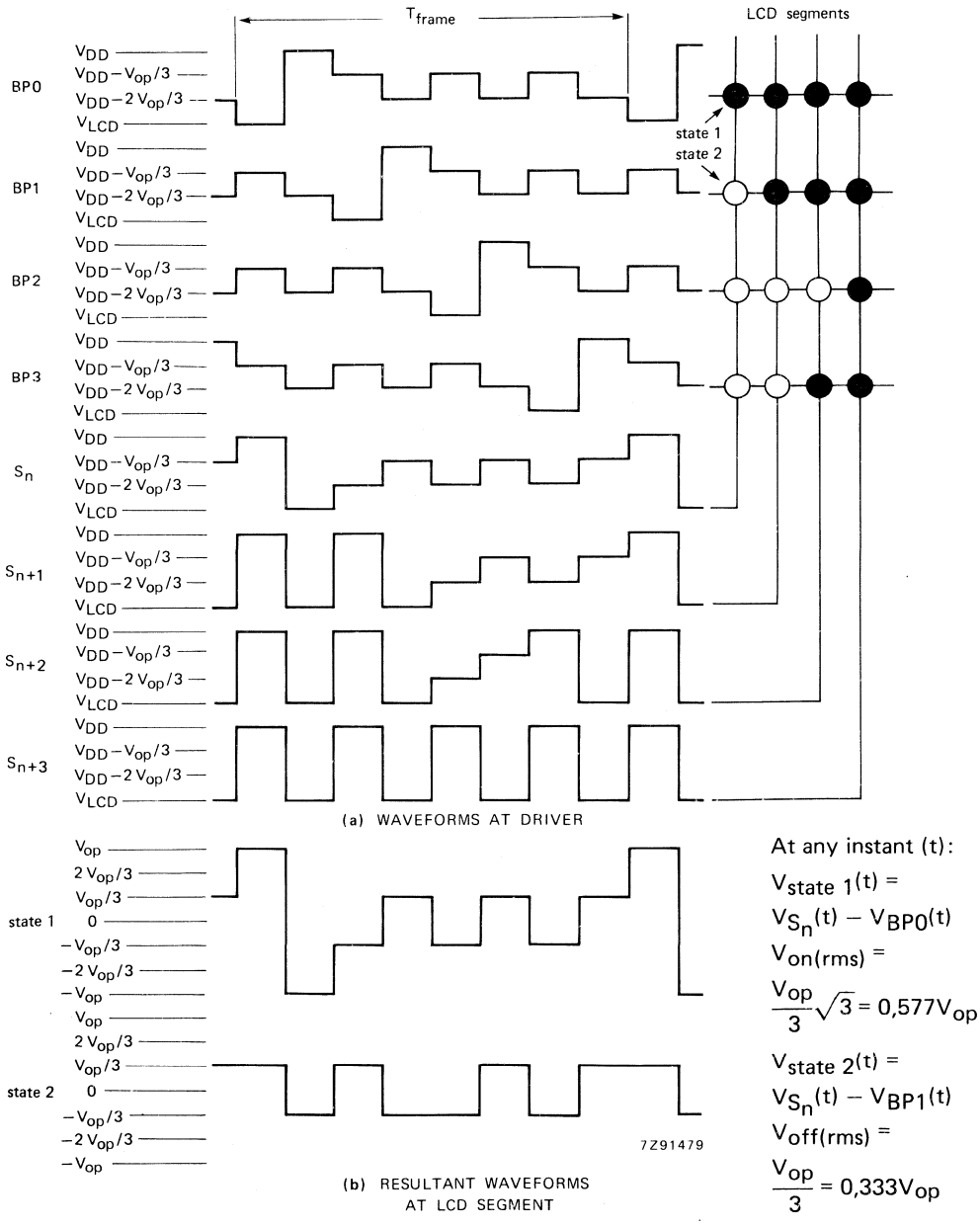


Fig. 8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

The internal logic and the LCD drive signals of the PCF8566 or PCF8576 are timed either by the built-in oscillator or from an external clock.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I^2C bus. To allow I^2C bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

Internal clock

When the internal oscillator is used, OSC (pin 6) should be tied to V_{SS}. In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8566s and PCF8576s in the system.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

Timing

The timing of the PCF8566 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8566s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by MODE SET commands when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8566 mode	f_{frame}	nominal f_{frame} (Hz)
normal mode	$f_{CLK}/2880$	64
power-saving mode	$f_{CLK}/480$	64

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line low until the first display data byte is stored. This slows down the transmission rate of the I^2C bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

Segment outputs

The LCD drive section includes 24 segment outputs S0 to S23 (pins 17 to 40) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 24 segment outputs are required the unused segment outputs should be left open-circuit.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 24 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 24 segments operated with respect to backplane BP0 (Fig. 9). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

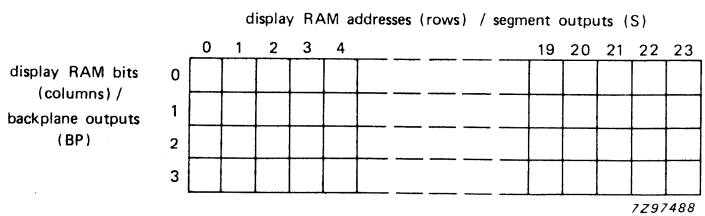


Fig. 9 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8566 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig. 10; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig. 10, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig. 10. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). A0, A1 and A2 should be tied to V_{SS} or V_{DD}. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8566 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

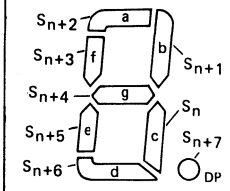
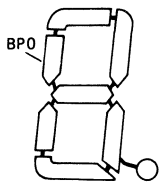
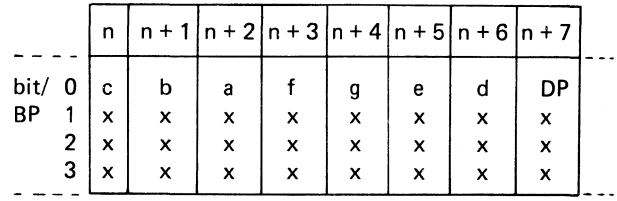
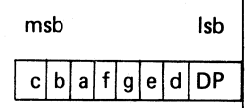
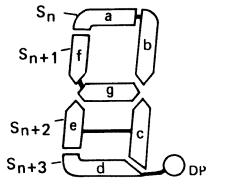
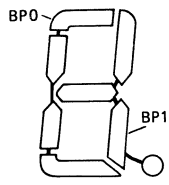
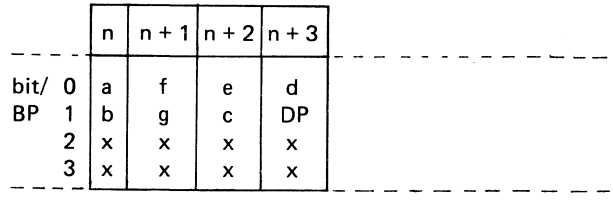
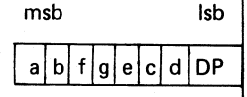
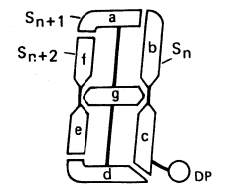
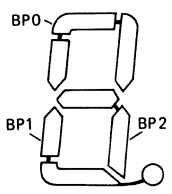
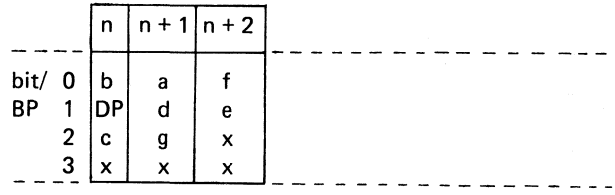
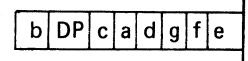
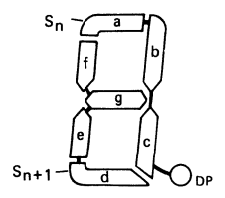
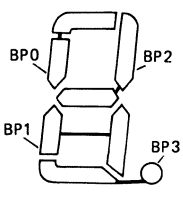
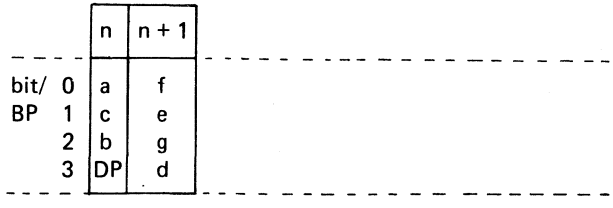
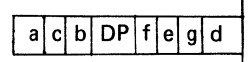
drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte
static				
1 : 2 multiplex				
1 : 3 multiplex				
1 : 4 multiplex				

Fig. 10 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

7Z91469

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8566 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8566 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

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Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0,5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0,5

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

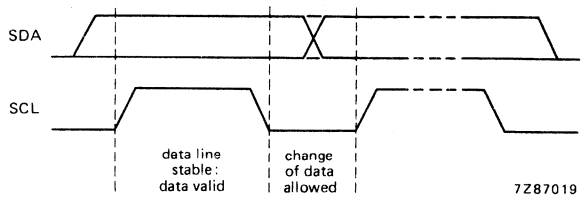


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

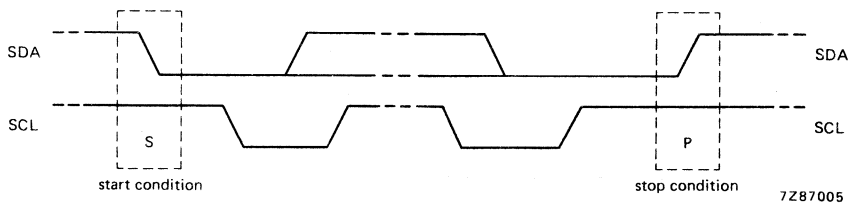


Fig. 12 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

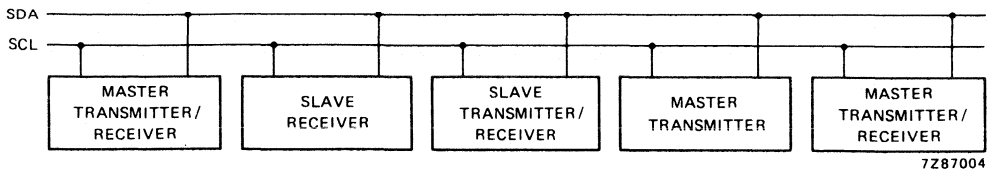


Fig. 13 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

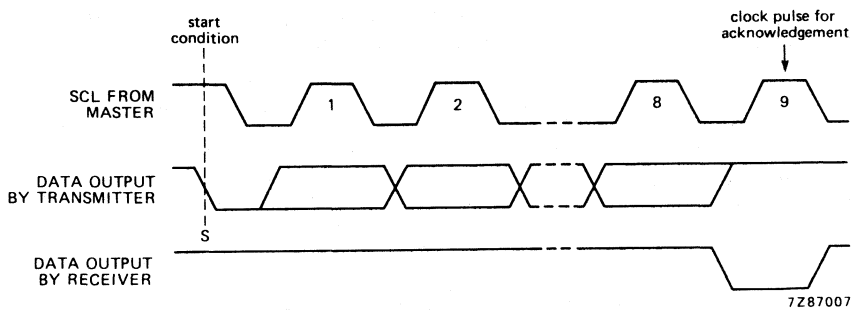


Fig. 14 Acknowledgement on the I^2C bus.

PCF8566 I²C bus controller

The PCF8566 acts as an I²C slave receiver. It does not initiate I²C bus transfers or transmit data to an I²C master receiver. The only data output from the PCF8566 are the acknowledge signals of the selected devices. Device selection depends on the I²C bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally left open-circuit or tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are left open-circuit or tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8566 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8566 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C bus protocol

Two I²C bus slave addresses (0111110 and 0111111) are reserved for PCF8566. The least-significant bit of the slave address that a PCF8566 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8566 can be distinguished on the same I²C bus which allows:

(a) up to 16 PCF8566s on the same I²C bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I²C bus.

The I²C bus protocol is shown in Fig. 15. The sequence is initiated with a start condition (S) from the I²C bus master which is followed by one of the two PCF8566 slave addresses available. All PCF8566s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8566s with the alternative SA0 level ignore the whole I²C bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8566s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8566s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8566 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8566. After the last display byte, the I²C bus master issues a stop condition (P).

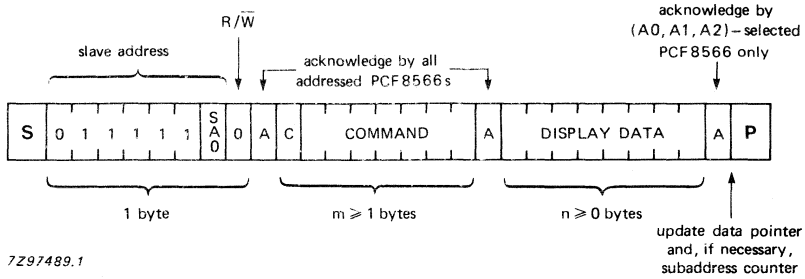


Fig. 15 I^2C bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I^2C bus. All available commands carry a continuation bit C in their most-significant bit position (Fig. 16). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

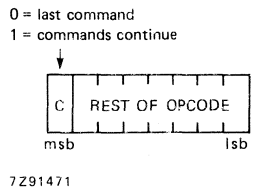


Fig. 16 General format of command byte.

The five commands available to the PCF8566 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8566 commands

command/opcode	options	description
MODE SET C 1 0 LP E B M1 M0	LCD drive mode: bits M1 M0 static (1 BP): 0 1 1 : 2 MUX (2 BP): 1 0 1 : 3 MUX (3 BP): 1 1 1 : 4 MUX (4 BP): 0 0 LCD bias: bit B 1/3 bias: 0 1/2 bias: 1 display status: bit E disabled (blank): 0 enabled: 1 mode: bit LP normal mode: 0 power-saving mode: 1	Defines LCD drive mode Defines LCD bias configuration Defines display status The possibility to disable the display allows implementation of blinking under external control Defines power dissipation mode
LOAD DATA POINTER C 0 0 P4 P3 P2 P1 P0	bits P4 P3 P2 P1 P0 5-bit binary value of 0 to 23	Five bits of immediate data, bits P4 to P0, are transferred to the data pointer to define one of twenty-four display RAM addresses
DEVICE SELECT C 1 1 0 0 A2 A1 A0	bits A0 A1 A2 3-bit binary value of 0 to 7	Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses

DEVELOPMENT DATA

command/opcode	options	description
BANK SELECT C 1 1 1 1 0 I O	static: 1 : 2 MUX, bit I RAM bit 0: RAM bits 0, 1: 0 RAM bit 2: RAM bits 2, 3: 1 static: 1 : 2 MUX, bit O RAM bit 0: RAM bits 0, 1: 0 RAM bit 2: RAM bits 2, 3: 1	Defines input bank selection (storage of arriving display data) Defines output bank selection (retrieval of LCD display data) The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes
BLINK C 1 1 1 0 A BF1 BF0	blink frequency: bits BF1 BF0 off: 0 0 2 Hz: 0 1 1 Hz: 1 0 0,5 Hz: 1 1 blink mode: bit A normal blinking: 0 alternation blinking: 1	Defines the blinking frequency Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8566 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8566s can be distinguished on the same I²C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I²C slave address (SA0). It is also possible to cascade up to 16 PCF8566s. When cascaded, several PCF8566s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8566s of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (Fig. 17).

The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded PCF8566s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8566s with differing SA0 levels are cascaded). $\overline{SYNC}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8566 asserts the $\overline{SYNC}$ line at the onset of its last active backplane signal and monitors the $\overline{SYNC}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8566 to assert $\overline{SYNC}$. The timing relationships between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCF8576 are shown in Fig. 18. The waveforms are identical with the parent device PCF8576. Casadability between PCF8566s and PCF8576s is possible, giving cost effective LCD applications.

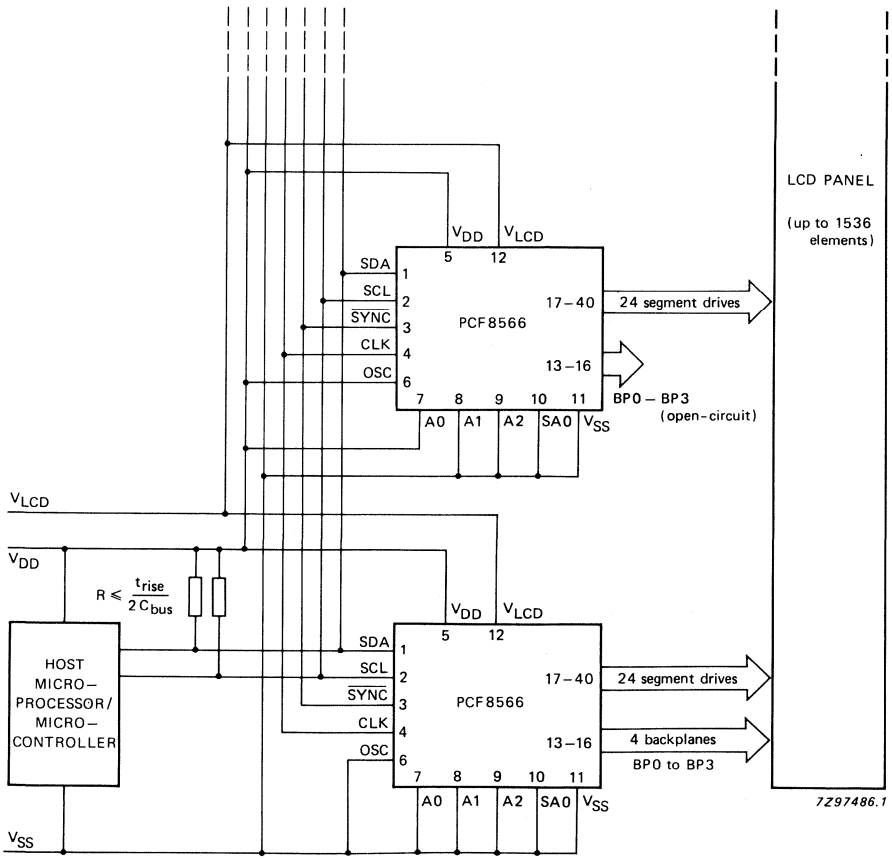


Fig. 17 Cascaded PCF8566 configuration.

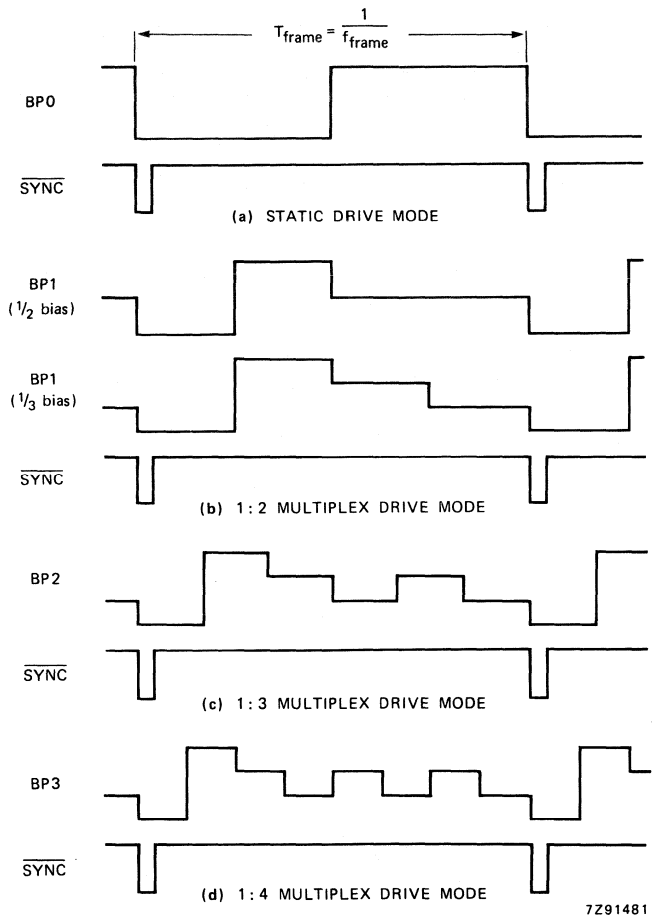


Fig. 18 Synchronization of the cascade for the various PCF8566 drive modes.

For single plane wiring of PCF8566s, see section "APPLICATION INFORMATION".

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range; see note	V_{DD}		−0,5 to + 7 V
LCD supply voltage range	V_{LCD}		V_{DD} −7 to V_{DD} V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_I		V_{SS} −0,5 to V_{DD} + 0,5 V
Output voltage range (S0 to S23; BP0 to BP3)	V_O		V_{LCD} −0,5 to V_{DD} + 0,5 V
DC input current	$\pm I_I$	max.	20 mA
DC output current	$\pm I_O$	max.	25 mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max.	50 mA
Power dissipation per package	P_{tot}	max.	400 mW
Power dissipation per output	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C

Note

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2,5 to 6 V; V_{LCD} = V_{DD} −2,5 to V_{DD} −6 V;

T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6	V
LCD supply voltage	V_{LCD}	V_{DD} −6	–	V_{DD} −2,5	V
Operating supply current (normal mode) at f_{CLK} = 200 kHz (note 1)	I_{DD}	–	30	90	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz; A0, A1 and A2 tied to V_{SS} (note 1)	I_{LP}	–	15	40	μA

parameter	symbol	min.	typ.	max.	unit
Logic					
Input voltage LOW	V_{IL}	V_{SS}	–	0,3 V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD} −0,05	–	–	V
Output current LOW (CLK, $\overline{SYNC}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	–	–	−1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current (SA0, CLK, OSC, A0, A1, A2, SCL, SDA) at $V_I = V_{SS}$ or V_{DD}	$\pm I_L$	–	–	1	μA
Pull-down current (A0; A1; A2; OSC) at V_I = 1 V and V_{DD} = 5 V	I_{pd}	15	50	150	μA
Pull-up resistor ($\overline{SYNC}$)	R_{SYNC}	15	25	60	kΩ
Power-on reset level (note 2)	V_{REF}	–	1,3	2,0	V
Tolerable spike width on bus	t_{sw}	–	–	100	ns
Input capacitance (note 3)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S23) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{DD}$ −5 V (note 4)	R_{BP}	–	1	5	kΩ
Output impedance (S0 to S23) at $V_{LCD} = V_{DD}$ −5 V (note 4)	R_S	–	3	7,0	kΩ

DEVELOPMENT DATA

AC CHARACTERISTICS (note 5)

V_{SS} = 0 V; V_{DD} = 2,5 to 6 V; V_{LCD} = V_{DD} −2,5 to V_{DD} −6 V;
T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) at V_{DD} = 5 V (note 6)	f_{CLK}	125	200	315	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{SYNC}$ propagation delay	t_{PSYNC}	–	–	400	ns
$\overline{SYNC}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at V_{LCD} = V_{DD} −5 V	t_{PLCD}	–	–	30	μs
I²C bus					
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4	–	–	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_r	–	–	1	μs
Fall time	t_f	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs

Notes to characteristics

1. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I²C bus inactive.
2. Resets all logic when $V_{DD} < V_{REF}$.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.
5. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
6. At $f_{CLK} < 125$ kHz, I²C bus maximum transmission speed is derated.

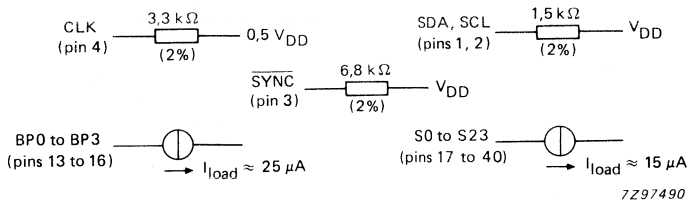


Fig. 19 Test loads.

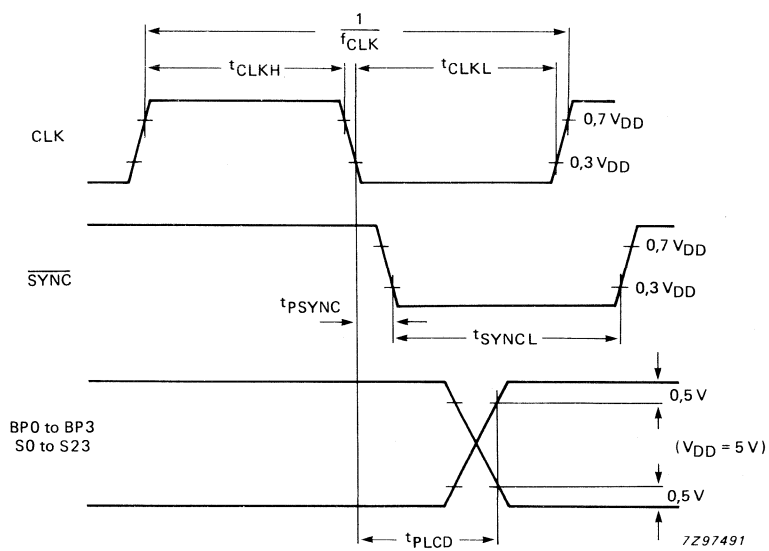


Fig. 20 Driver timing waveforms.

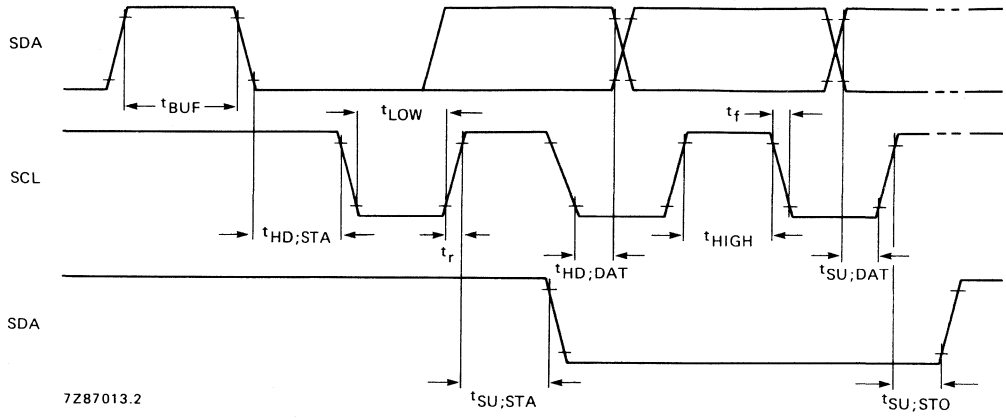
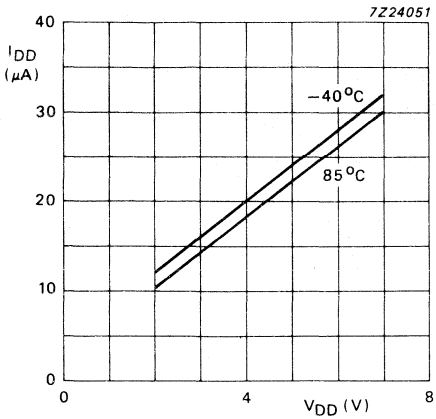
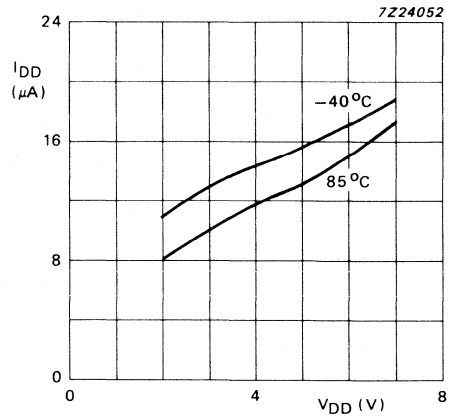


Fig. 21 I²C bus timing waveforms.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.



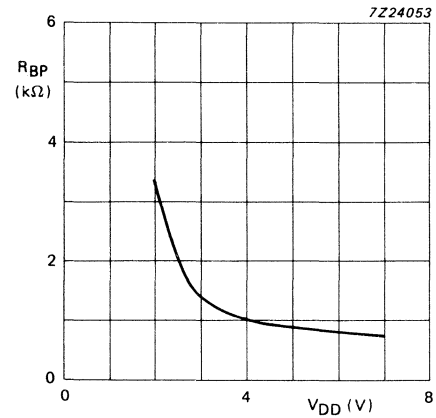
(a) Normal mode; V_{LCD} = 0 V; external clock = 200 kHz.



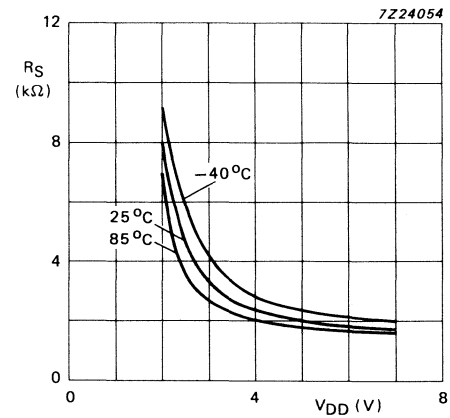
(b) Low power mode; V_{LCD} = 0 V; external clock = 35 kHz.

Fig. 22 Typical supply current characteristics.

DEVELOPMENT DATA



(a) Backplane output impedance BP0 to BP3 (R_{BP}); V_{DD} = 5 V; T_{amb} = −40 to + 85 °C.



(b) Segment output impedance S0 to S23 (R_S); V_{DD} = 5 V.

Fig. 23 Typical characteristics of LCD outputs.

APPLICATION INFORMATION

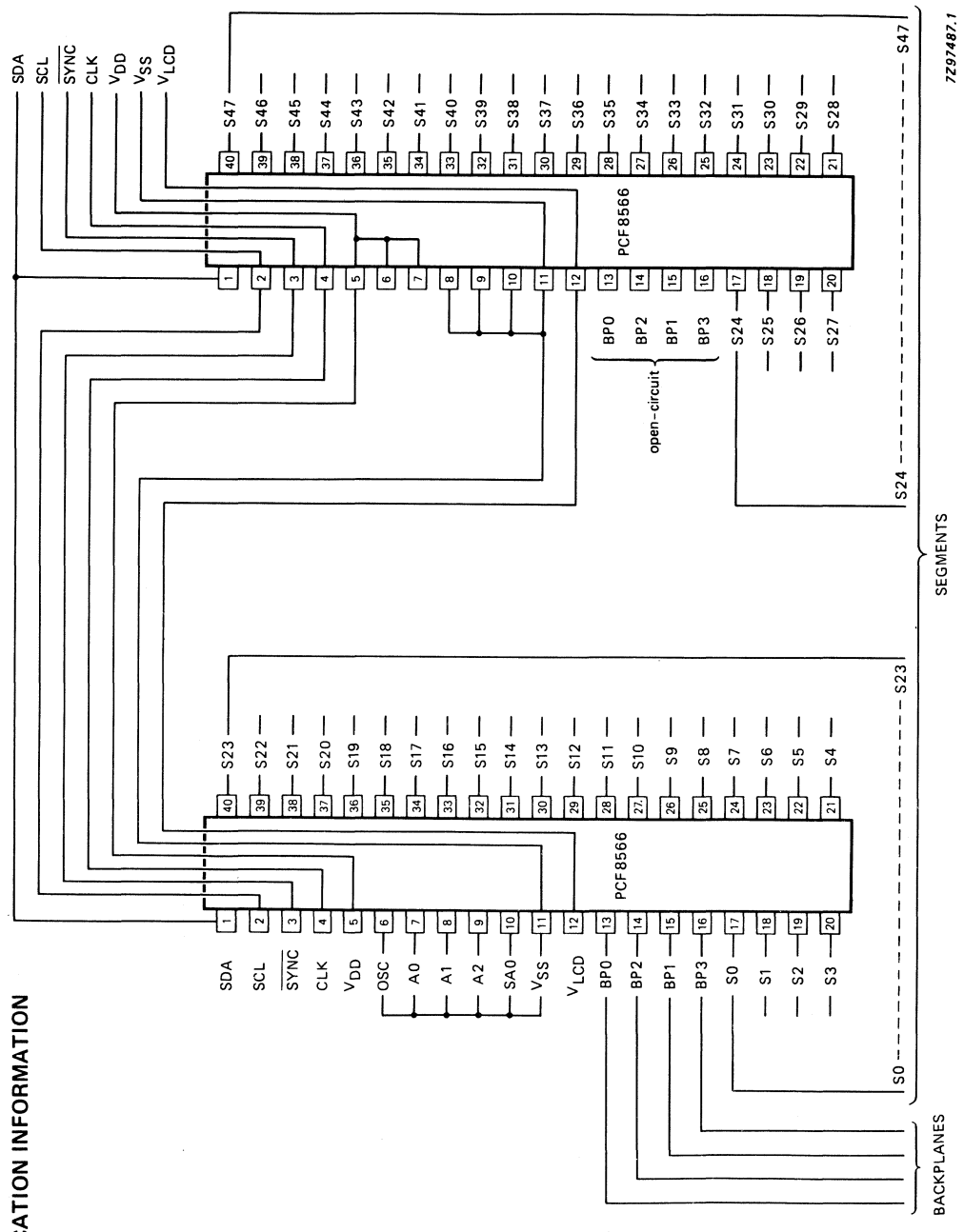
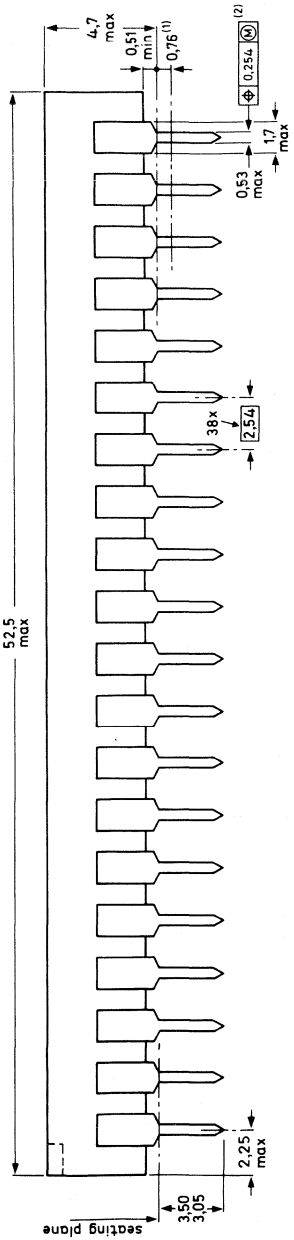
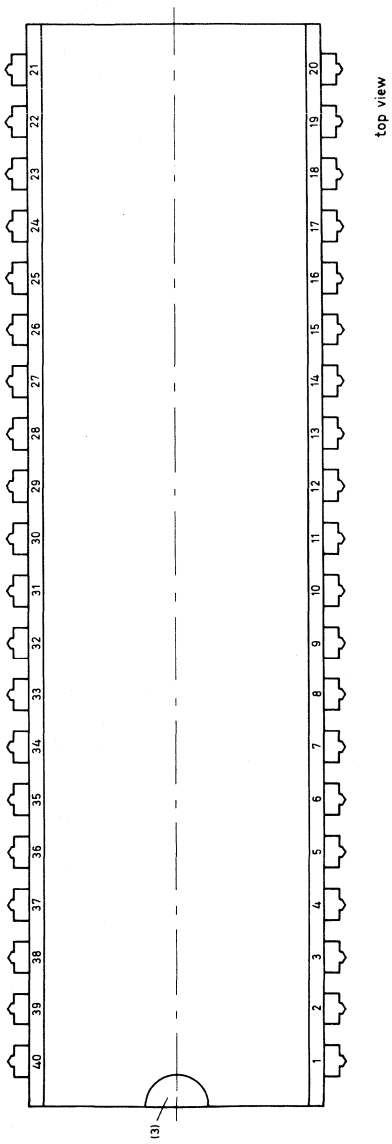


Fig. 24 Single plane wiring of packaged PCF8566s.

40-LEAD DUAL IN-LINE; PLASTIC (SOT-129)

DEVELOPMENT DATA





⊕ Positional accuracy.

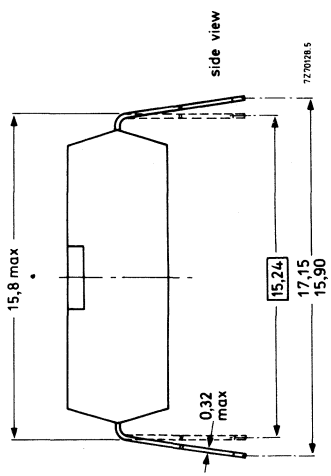
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm



SOLDERING

See next page.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

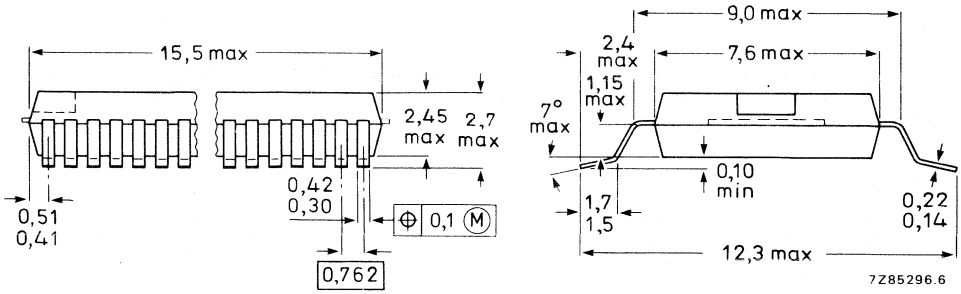
2. By dip or wave

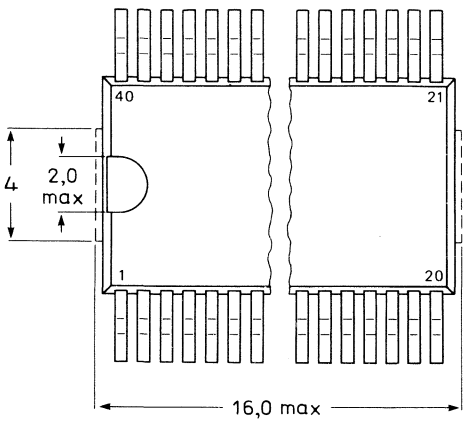
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

40-LEAD MINI-PACK; PLASTIC (VSO-40; SOT-158A)





top view

DEVELOPMENT DATA

Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

See next page.

SOLDERING

1. **By hand-held soldering iron or pulse-heated solder tool**

   Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

   For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. **By wave**

   Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

   A modified wave soldering technique is recommended, using two solder waves (dual-wave); a first turbulent wave with high upward pressure is followed by a smooth, laminar wave. A mildly activated flux will eliminate the need for removal of corrosive residues in most applications.

3. **By solder paste reflow**

   Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing or pressure-syringe dispensing before device placement.

   Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 8 and 60 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

   Pre-heating is necessary to dry paste and evaporate binding agent, and to reduce thermal shock on entry to reflow zone.

4. **Repairing soldered joints**

   The same precautions and limits apply as in (1) above.

SUPERSEDES DATA OF MARCH 1987

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with the 24-segment LCD driver PCF8566
- Optimized pinning for single plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic mini-pack (VSO56) or 64-lead tape-automated-bonding (TAB) module (SOT267A) ←
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8576T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8576U: uncased chip in tray.
PCF8576U/10: chip-on-film frame carrier (FFC).
PCF8576V: 64-lead tape-automated-bonding module (SOT267A). ←

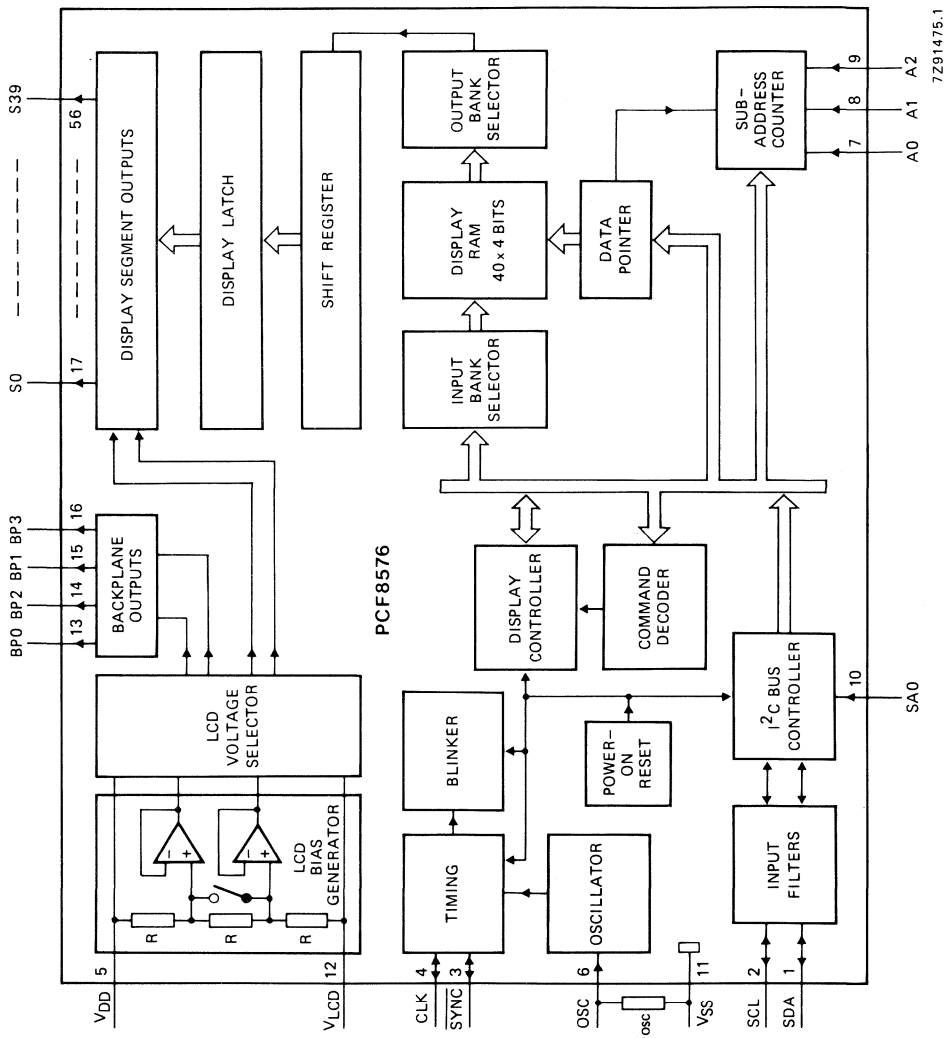


Fig. 1 Block diagram; VSO56; SOT190.

PINNING

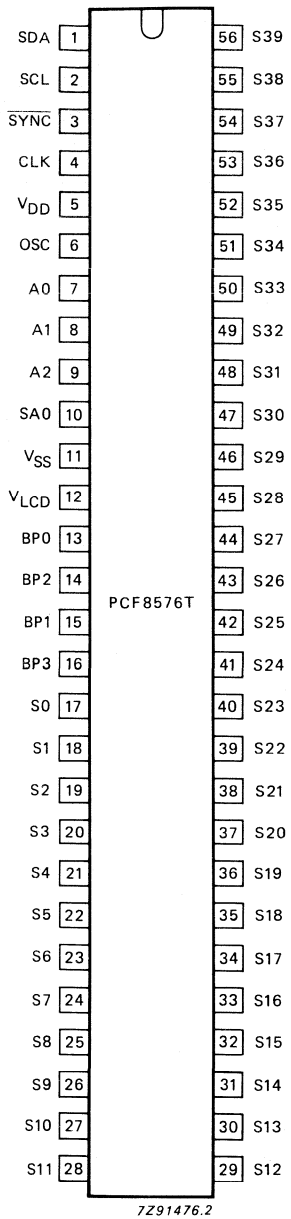
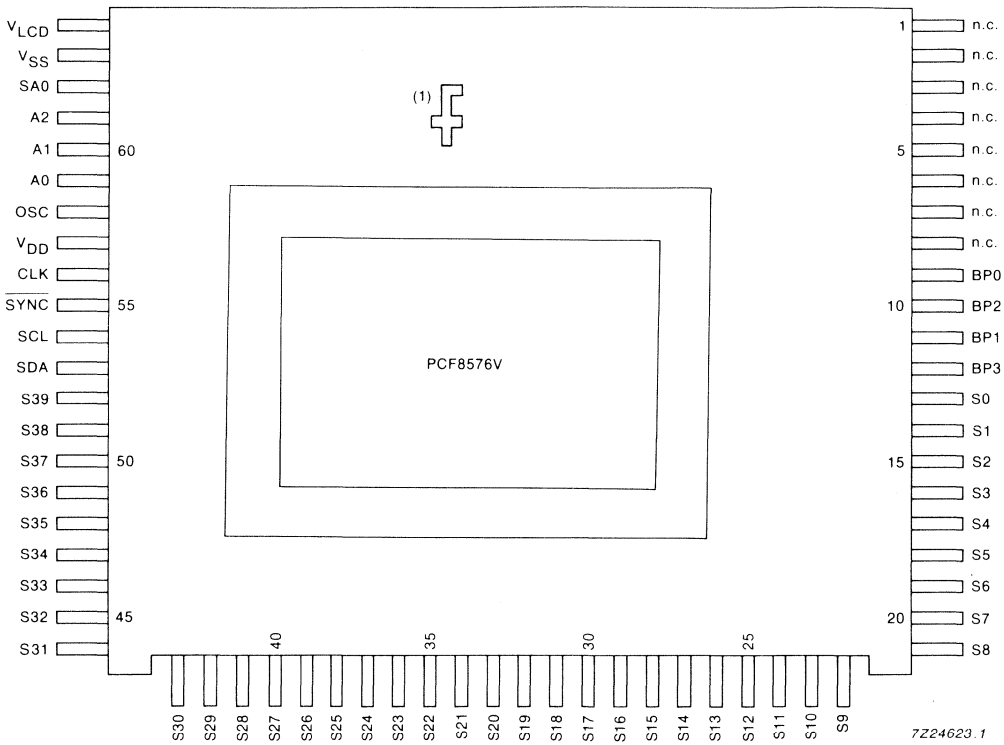


Fig.2(a) Pinning diagram: VSO56; SOT190.

PINNING (continued)



(1) Orientation mark.

Fig.2(b) Pinning diagram; SOT267A.

mnemonic	pin no.		description
	SOT190	SOT267A	
SDA	1	53	I^2C-bus serial data line
SCL	2	54	I^2C-bus serial clock line
$\overline{SYNC}$	3	55	cascade synchronization input
CLK	4	56	external clock input
V_{DD}	5	57	positive supply voltage
OSC	6	58	oscillator input
A0 to A2	7 - 9	59 - 61	I^2C-bus subaddress inputs
SA0	10	62	I^2C-bus slave address input (bit 0)
V_{SS}	11	63	ground (logic)
V_{LCD}	12	64	LCD supply voltage
n.c.		1 - 8	not connected
BP0 to BP3	13 - 16	9 - 12	LCD backplane outputs
S0 to S39	17 - 56	13 - 52	LCD segment outputs

FUNCTIONAL DESCRIPTION

The PCF8576 is a versatile peripheral device designed to interface any microprocessor/microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments. The display configurations possible with the PCF8576 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active back-plane outputs	no. of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	160	20 digits + 20 indicator symbols	10 characters + 20 indicator symbols	160 dots (4 x 40)
3	120	15 digits + 15 indicator symbols	8 characters + 8 indicator symbols	120 dots (3 x 40)
2	80	10 digits + 10 indicator symbols	5 characters + 10 indicator symbols	80 dots (2 x 40)
1	40	5 digits + 5 indicator symbols	2 characters + 12 indicator symbols	40 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig.3. The host microprocessor/microcontroller maintains the 2-line I^2C-bus communication channel with the PCF8576. A resistor connected between OSC (pin 6) and V_{SS} (pin 11) controls the device clock frequency. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

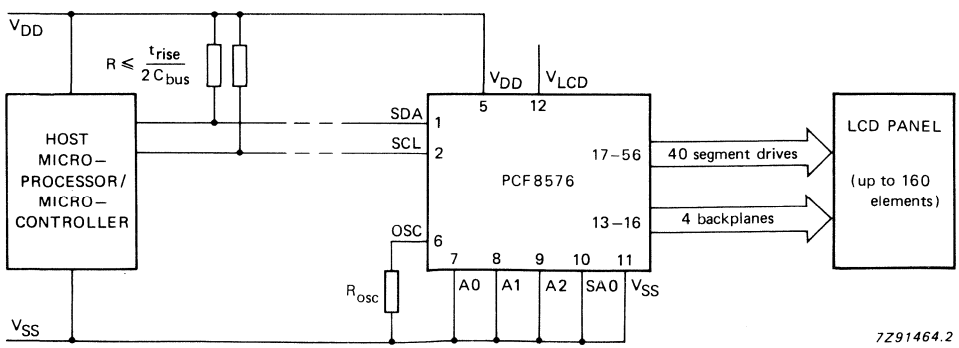


Fig.3 Typical system configuration.

Power-on reset

At power-on the PCF8576 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C-bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C-bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off\ (rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on\ (rms)}}{V_{off\ (rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0.354$	$\sqrt{10}/4 = 0.791$	$\sqrt{5} = 2.236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0.333$	$\sqrt{5}/3 = 0.745$	$\sqrt{5} = 2.236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0.333$	$\sqrt{33}/9 = 0.638$	$\sqrt{33}/3 = 1.915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0.333$	$\sqrt{3}/3 = 0.577$	$\sqrt{3} = 1.732$

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off\ (rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\ V_{th}$.
Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1.732$ for 1: 3 multiplex or $\sqrt{21}/3 = 1.528$ for 1 : 4 multiplex).
The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

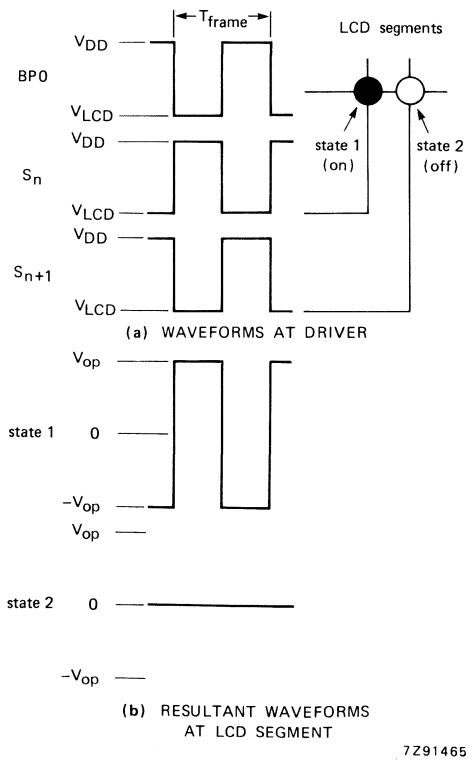
1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\ V_{off\ (rms)} = 2.449\ V_{off\ (rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\ V_{off\ (rms)} = 2.309\ V_{off\ (rms)}$

These compare with $V_{op} = 3\ V_{off\ (rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig.4.



At any instant (t):

$V_{state\ 1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on\ (rms)} = V_{op}$

$V_{state\ 2}(t) = V_{S_{n+1}}(t) - V_{BP0}(t)$

$V_{off\ (rms)} = 0\ V$

Fig.4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8576 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

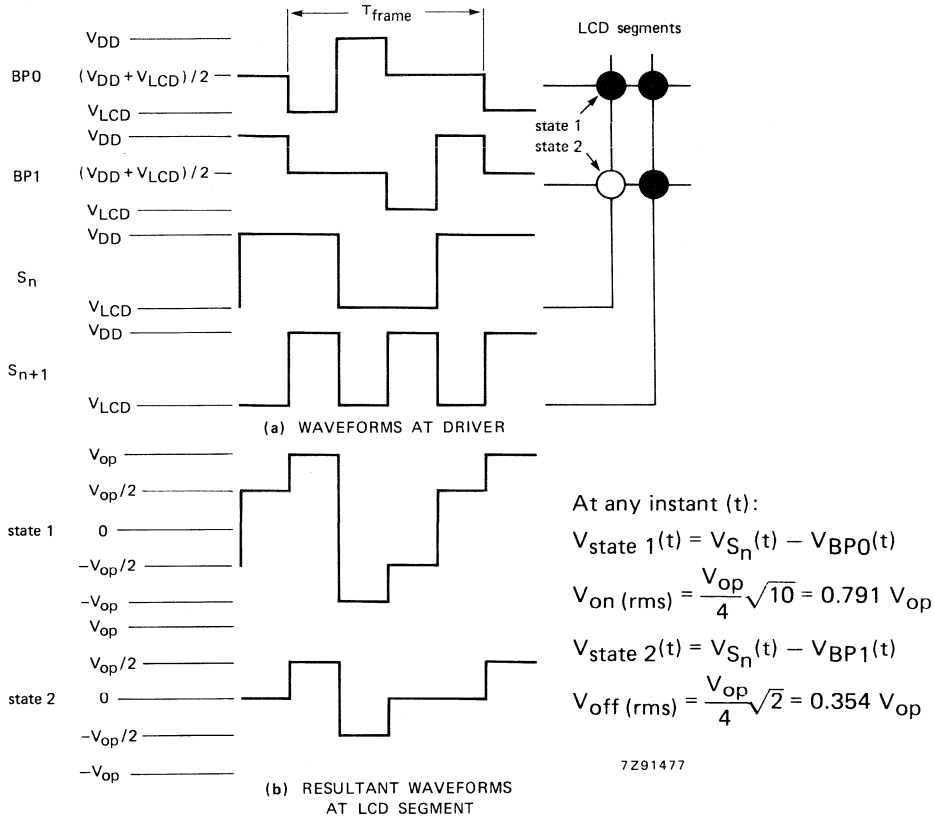


Fig.5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

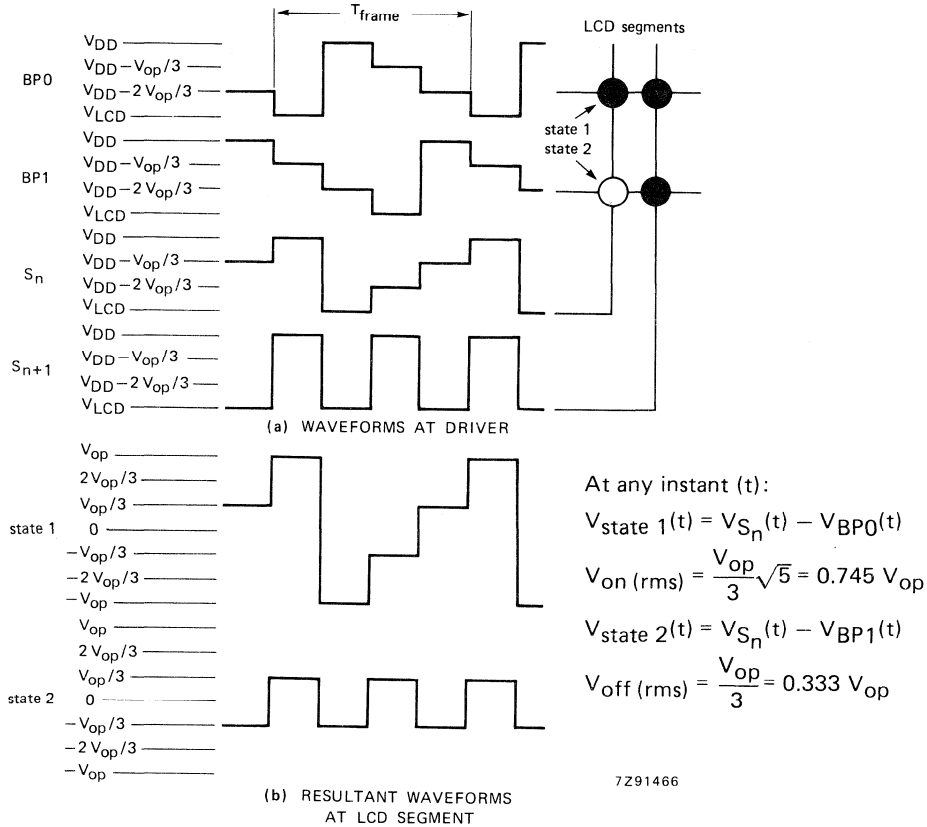


Fig.6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive waveform for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

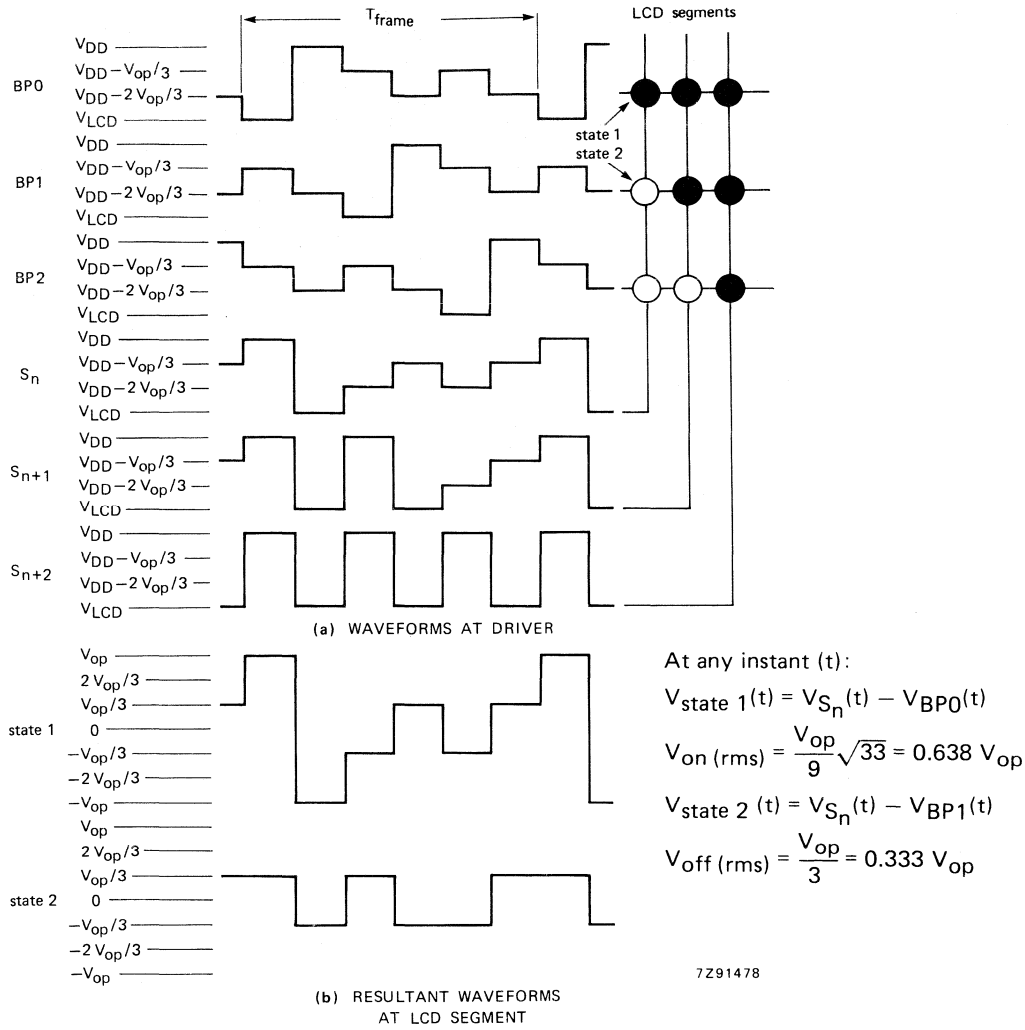
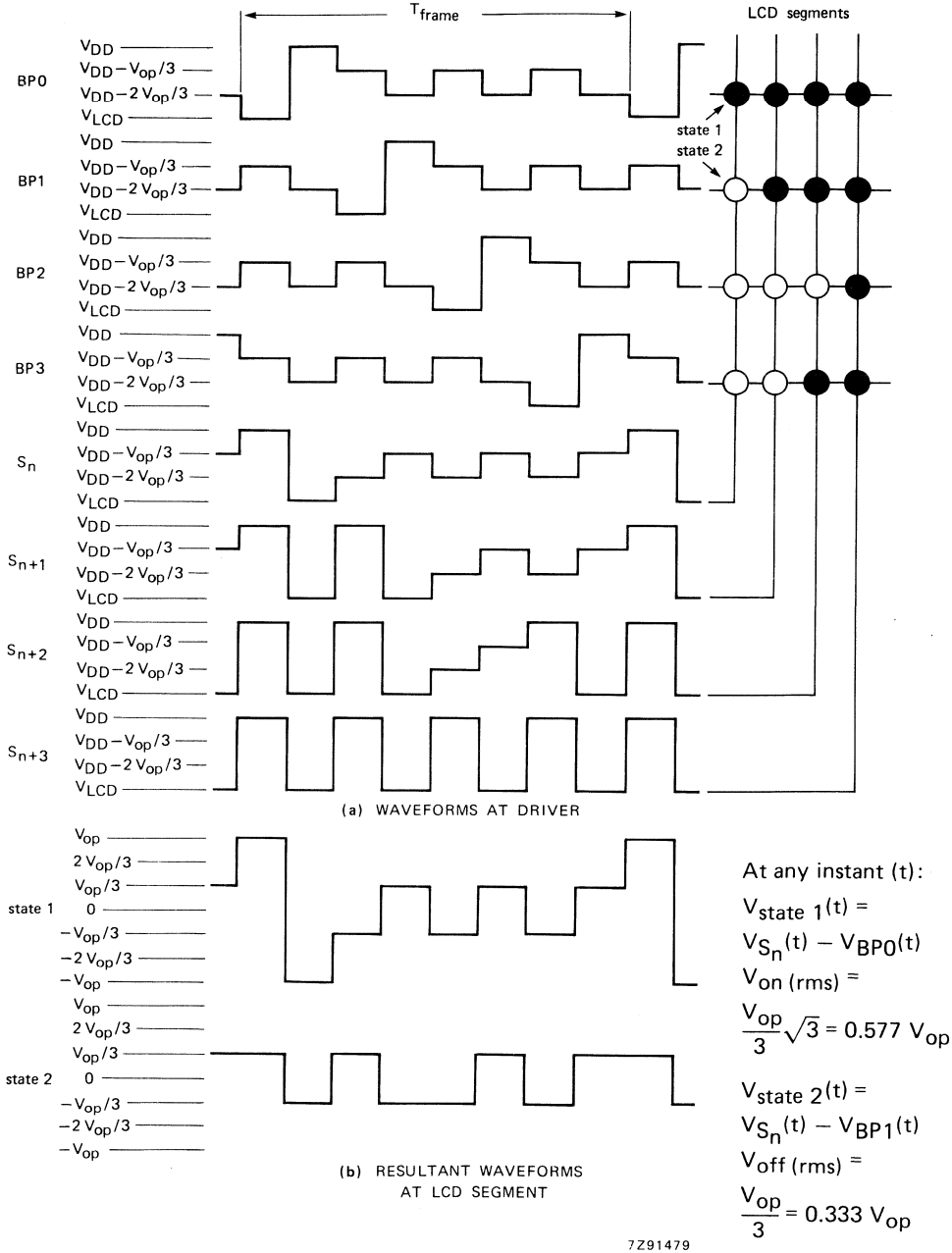


Fig.7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)



At any instant (t):

$V_{state\ 1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on\ (rms)} = \frac{V_{op}}{3}\sqrt{3} = 0.577\ V_{op}$

$V_{state\ 2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off\ (rms)} = \frac{V_{op}}{3} = 0.333\ V_{op}$

Fig.8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

Internal clock

The internal logic and the LCD drive signals of the PCF8576 are timed either by the built-in oscillator or from an external clock. When the internal oscillator is used, frequency control is performed by a single resistor connected between OSC (pin 6) and V_{SS} (pin 11) as shown in Fig.9. In this application, the output from CLK (pin 4) provides the clock signal for cascaded PCF8576s in the system.

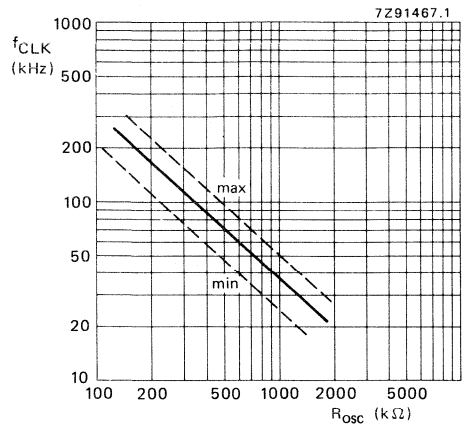


Fig.9 Oscillator frequency as a function of R_{osc}: $f_{CLK} \approx (3.4 \times 10^7/R_{osc})$ kHz·Ω.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I^2C-bus. To allow I^2C-bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

Timing

The timing of the PCF8576 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8576s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by the choice of value for R_{osc} when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8576 mode	recommended R_{osc} (kΩ)	f_{frame}	nominal f_{frame} (Hz)
normal mode	180	$f_{CLK}/2880$	64
power-saving mode	1200	$f_{CLK}/480$	64

Timing (continued)

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the normal mode, R_{osc} = 180 kΩ will result in the nominal frame frequency. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six and for the same frame frequency R_{osc} will be 1.2 MΩ. The reduced clock frequency and the increased value of R_{osc} together contribute to a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C-bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I^2C-bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data is displayed.

Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 (pins 17 to 56) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 40 segment outputs are required the unused segment outputs should be left open.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 40 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 40 segments operated with respect to backplane BP0 (Fig.10). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

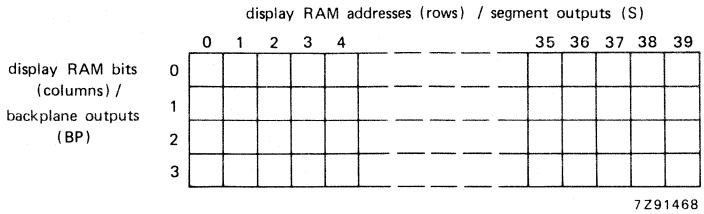


Fig.10 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8576 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig.11; the RAM filling organization depicted applies equally to other LCD types.

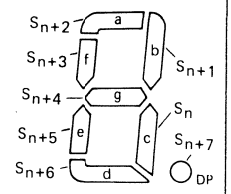
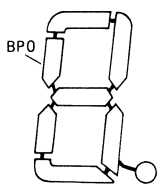
With reference to Fig.11, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig.11. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

<table>
<tr><th>drive mode</th><th>LCD segments</th><th>LCD backplanes</th><th>display RAM filling order</th><th>transmitted display byte</th></tr>
<tr><td>static</td><td> 
</td><td> 
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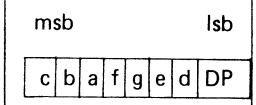
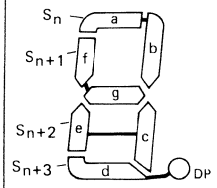
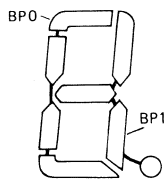
</td><td> 
</td></tr>
<tr><td>1 : 2
multiplex</td><td> 
</td><td> 
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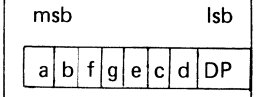
</td><td> 
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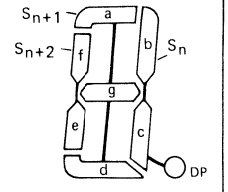
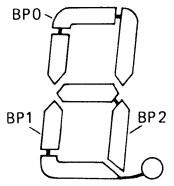
multiplex</td><td> 
</td><td> 
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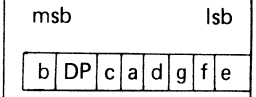
</td><td> 
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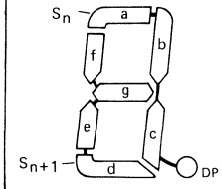
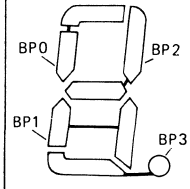
multiplex</td><td> 
</td><td> 
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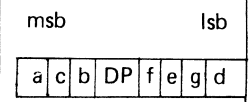
</td><td> 
</td></tr>
</table>

Fig. 11 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

7Z91469

Subaddress counter (continued)

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8576 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1 : 3 multiplex mode).

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8576 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8576 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Blinker (continued)

Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0.5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0.5

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

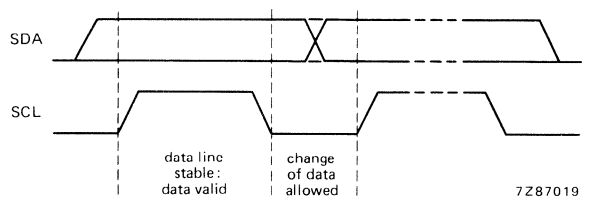


Fig.12 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

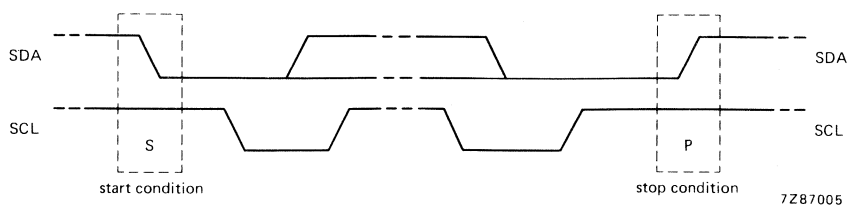


Fig.13 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

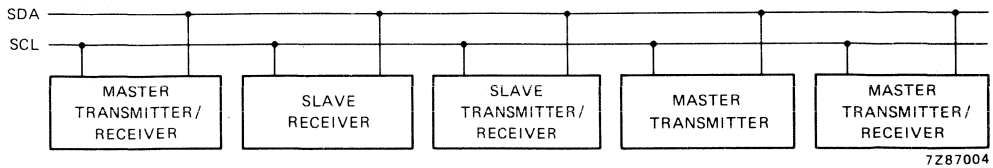


Fig.14 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

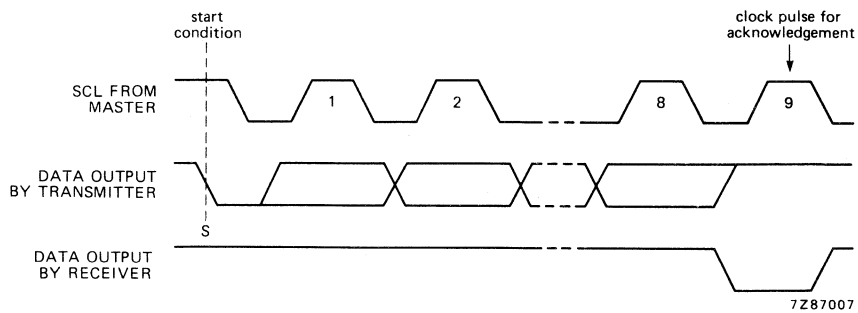


Fig.15 Acknowledgement on the I^2C-bus.

Note

The general characteristics and detailed specification of the I^2C-bus are described in Handbook IC12: I^2C-bus compatible ICs.

PCF8576 I²C-bus controller

The PCF8576 acts as an I²C slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C master receiver. The only data output from the PCF8576 are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8576 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8576 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C-bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C-bus protocol

Two I²C-bus slave addresses (0111000 and 0111001) are reserved for PCF8576. The least-significant bit of the slave address that a PCF8576 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8576 can be distinguished on the same I²C-bus which allows:

(a) up to 16 PCF8576s on the same I²C-bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I²C-bus.

The I²C-bus protocol is shown in Fig.16. The sequence is initiated with a start condition (S) from the I²C-bus master which is followed by one of the two PCF8576 slave addresses available. All PCF8576s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8576s with the alternative SA0 level ignore the whole I²C-bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8576s. The last command byte is tagged with a cleared mist significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8576s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8576 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8576. After the last display byte, the I²C-bus master issues a stop condition (P).

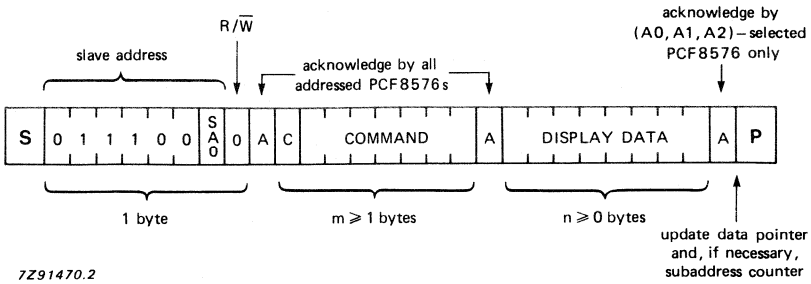


Fig.16 I²C-bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. All available commands carry a continuation bit C in their most-significant bit position (Fig.17). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

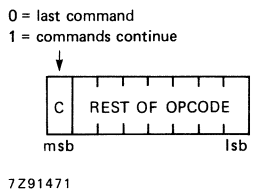


Fig.17 General format of command byte.

The five commands available to the PCF8576 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8576 commands

<table>
<tr><th>command/opcode</th><th>options</th><th>description</th></tr>
<tr><td>MODE SET

C | 1 | 0 | LP | E | B | M1 | M0</td><td>LCD drive mode | bits M1 M0
static (1 BP) | 0 1
1 : 2 MUX (2 BP) | 1 0
1 : 3 MUX (3 BP) | 1 1
1 : 4 MUX (4 BP) | 0 0

LCD bias | bit B
1/3 bias | 0
1/2 bias | 1

display status | bit E
disabled (blank) | 0
enabled | 1

mode | bit LP
normal mode | 0
power-saving mode | 1</td><td>Defines LCD drive mode

Defines LCD bias configuration

Defines display status
The possibility to disable the display allows implementation of blinking under external control

Defines power dissipation mode</td></tr>
<tr><td>LOAD DATA POINTER

C | 0 | P5 P4 P3 P2 P1 P0</td><td>bits P5 P4 P3 P2 P1 P0
6-bit binary value of 0 to 39</td><td>Six bits of immediate data, bits P5 to P0, are transferred to the data pointer to define one of forty display RAM addresses</td></tr>
<tr><td>DEVICE SELECT

C | 1 1 0 0 | A2 A1 A0</td><td>bits A0 A1 A2
3-bit binary value of 0 to 7</td><td>Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses</td></tr>
</table>

<table>
<tr><th>command/opcode</th><th>options</th><th>description</th></tr>
<tr><td>BANK SELECT

C | 1 | 1 | 1 | 1 | 0 | I | O</td><td>
<table>
<tr><td>static</td><td>1 : 2 MUX</td><td>bit I</td></tr>
<tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr>
</table>
<table>
<tr><td>static</td><td>1 : 2 MUX</td><td>bit O</td></tr>
<tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr>
</table>
</td><td>Defines input bank selection (storage of arriving display data)

Defines output bank selection (retrieval of LCD display data)

The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
<tr><td>BLINK

C | 1 | 1 | 1 | 0 | A | BF1 | BF0</td><td>
<table>
<tr><td>blink frequency</td><td>bits BF1</td><td>BF0</td></tr>
<tr><td>off</td><td>0</td><td>0</td></tr>
<tr><td>2 Hz</td><td>0</td><td>1</td></tr>
<tr><td>1 Hz</td><td>1</td><td>0</td></tr>
<tr><td>0.5 Hz</td><td>1</td><td>1</td></tr>
</table>
<table>
<tr><td>blink mode</td><td>bit A</td></tr>
<tr><td>normal blinking
alternation blinking</td><td>0
1</td></tr>
</table>
</td><td>Defines the blinking frequency

Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
</table>

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8576 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8576s can be distinguished on the same I^2C-bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I^2C slave address (SA0). It is also possible to cascade up to 16 PCF8576s. When cascaded, several PCF8576s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8576s of the cascade contribute additional segment outputs but their backplane outputs are left open (Fig.18).

The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded PCF8576s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8576s with differing SA0 levels are cascaded). $\overline{SYNC}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8576 asserts the $\overline{SYNC}$ line at the onset of its last active backplane signal and monitors the $\overline{SYNC}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8576 to assert $\overline{SYNC}$. The timing relationships between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCF8576 are shown in Fig.19.

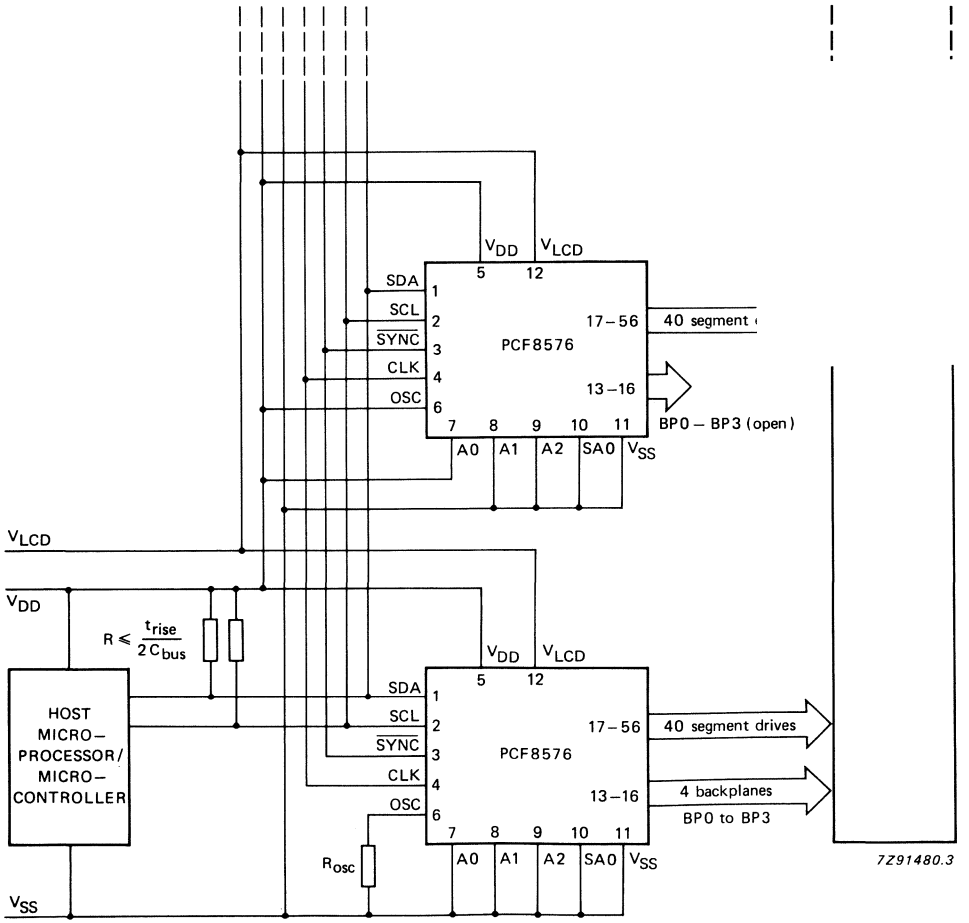
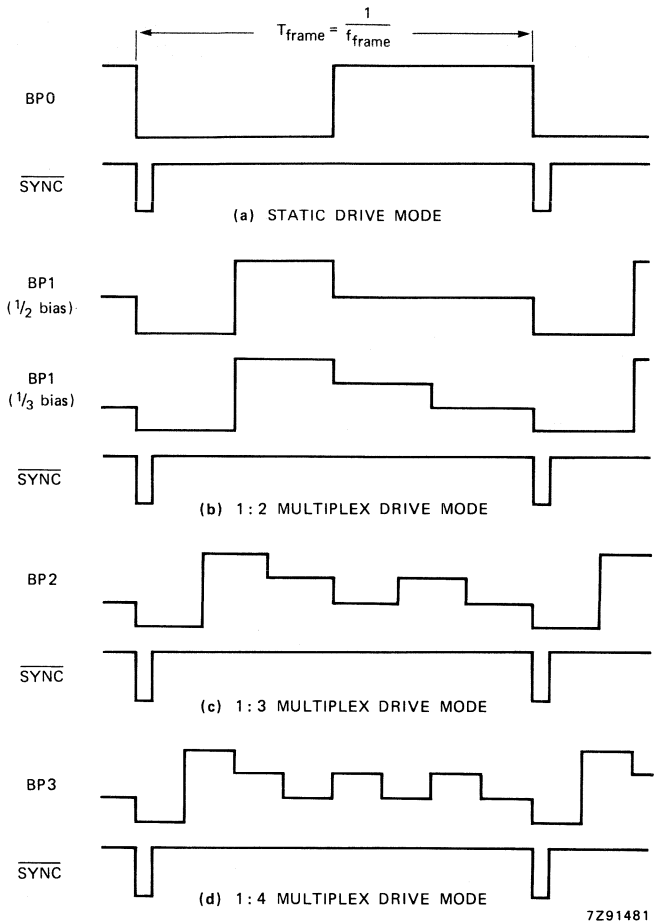


Fig.18 Cascaded PCF8576 configuration.



Note

Excessive capacitive coupling between SCL or CLK and SYNC may cause erroneous synchronization. If this proves to be a problem, the capacitance of the $\overline{SYNC}$ line should be increased (e.g. by an external capacitor between $\overline{SYNC}$ and V_{DD}). Degradation of the positive edge of the $\overline{SYNC}$ pulse may be countered by an external pull-up resistor.

Fig.19 Synchronization of the cascade for the various PCF8576 drive modes.

For single plane wiring of packaged PCF8576s and chip-on-glass cascading, see 'APPLICATION INFORMATION'.

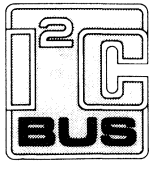
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	+ 11.0	V
LCD supply voltage range	V_{LCD}	V_{DD}−11	V_{DD}	V
Input voltage range SDA; SCL; CLK; $\overline{SYNC}$; SA0; OSC; A0 to A2	V_I	V_{SS}−0.5	V_{DD} + 0.5	V
Output voltage range S0 to S39; BP0 to BP3	V_O	V_{LCD}−0.5	V_{DD} + 0.5	V
DC input current	$\pm I_I$	–	20	mA
DC output current	$\pm I_O$	–	25	mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	–	50	mA
Power dissipation per package	P_{tot}	–	400	mW
Power dissipation per output	P_O	–	100	mW
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

DC CHARACTERISTICS

V_{DD} = 2 V to 9 V; V_{SS} = 0 V; V_{LCD} = V_{DD}−2 V to V_{DD}−9 V; T_{amb} = −40 °C to + 85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2	–	9	V
LCD supply voltage	note 1	V_{LCD}	V_{DD}−9	–	V_{DD}−2	V
Supply current	note 2;					
normal mode	f_{CLK} = 200 kHz	I_{DD}	–	–	180	μA
power-saving mode	V_{DD} = 3.5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz	I_{LP}	–	–	60	μA
Logic						
Input voltage LOW		V_{IL}	V_{SS}	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Output voltage LOW	I_O = 0 mA	V_{OL}	–	–	0.05	V
Output voltage HIGH	I_O = 0 mA	V_{OH}	V_{DD}−0.05	–	–	V
Output current LOW						
CLK; $\overline{SYNC}$	V_{OL} = 1 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH						
CLK	V_{OH} = 4 V; V_{DD} = 5 V	$-I_{OH}$	1	–	–	mA
Output current LOW						
SDA; SCL	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current						
SA0; A0 to A2; CLK; SDA; SCL	V_I = V_{SS} or V_{DD}	$\pm I_{L1}$	–	–	1	μA
OSC	V_I = V_{DD}	$\pm I_{L2}$	–	–	1	μA
Pull-up resistor ($\overline{SYNC}$)		R_{SYNC}	20	50	150	kΩ
Power-on reset level	note 3	V_{POR}	–	1.0	1.6	V
Tolerable spike width on bus		t_{SW}	–	–	100	ns
Input capacitance	note 4	C_I	–	–	7	pF
LCD outputs						
DC voltage component						
BP0 to BP3	C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
S0 to S39	C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance	note 5					
BP0 to BP3	V_{LCD} = V_{DD}−5 V	R_{BP}	–	–	5	kΩ
S0 to S39	V_{LCD} = V_{DD}−5 V	R_S	–	–	7.5	kΩ

AC CHARACTERISTICS (note 6)

V_{DD} = 2 V to 9 V; V_{SS} = 0 V; V_{LCD} = V_{DD}−2 V to V_{DD}−9 V; T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator frequency						
normal mode	V_{DD} = 5 V; note 7 R_{OSC} = 180 kΩ	f_{CLK}	125	185	288	kHz
power-saving mode	V_{DD} = 3.5 V; R_{OSC} = 1.2 MΩ	f_{CLKLP}	21	31	48	kHz
CLK HIGH time		t_{CLKH}	1	–	–	μs
CLK LOW time		t_{CLKL}	1	–	–	μs
$\overline{SYNC}$ propagation delay		t_{PSYNC}	–	–	400	ns
$\overline{SYNC}$ LOW time		t_{SYNCL}	1	–	–	μs
Driver delays						
with test loads	V_{LCD} = V_{DD}−5 V	t_{PLCD}	–	–	30	μs
I^2C-bus						
Bus free time		t_{BUF}	4.7	–	–	μs
Start condition hold time		$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time		t_{LOW}	4.7	–	–	μs
SCL HIGH time		t_{HIGH}	4.0	–	–	μs
Start condition set-up time						
(repeated start code only)		$t_{SU;STA}$	4.7	–	–	μs
Data hold time		$t_{HD;DAT}$	0	–	–	μs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	300	ns
Stop condition set-up time		$t_{SU;STO}$	4.0	–	–	μs

Notes to the characteristics

1. $V_{LCD} \leqslant V_{DD}$−3 V for 1/3 bias.
2. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I^2C-bus inactive.
3. Resets all logic when $V_{DD} < V_{POR}$.
4. Periodically sampled, not 100% tested.
5. Outputs measured one at a time.
6. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
7. At $f_{CLK} < 125$ kHz, I^2C-bus maximum transmission speed is derated.

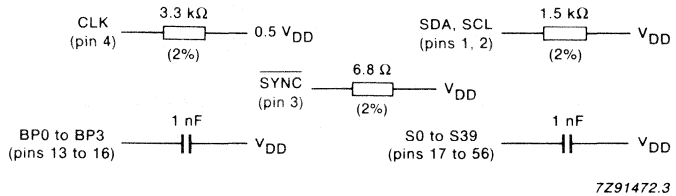


Fig.20 Test loads.

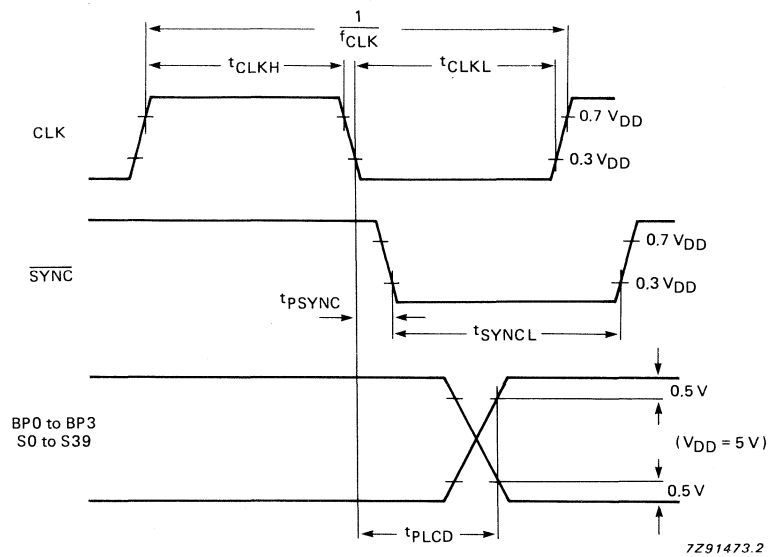


Fig.21 Driver timing waveforms.

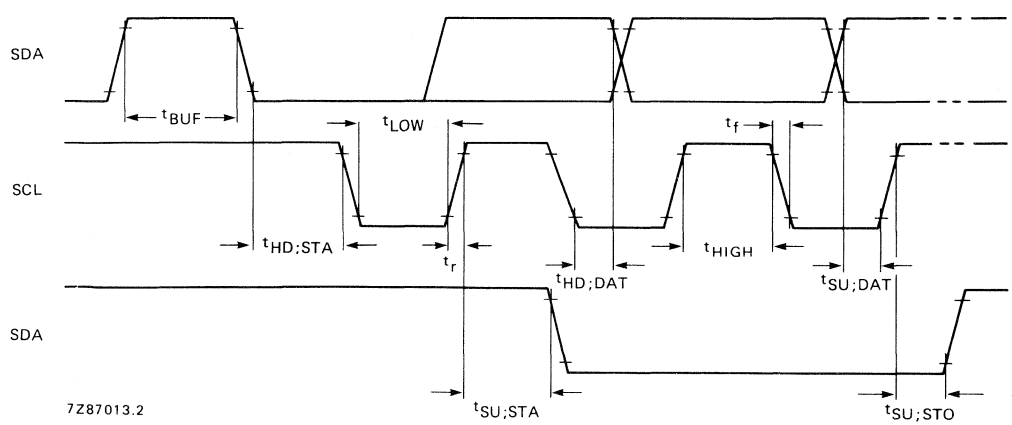
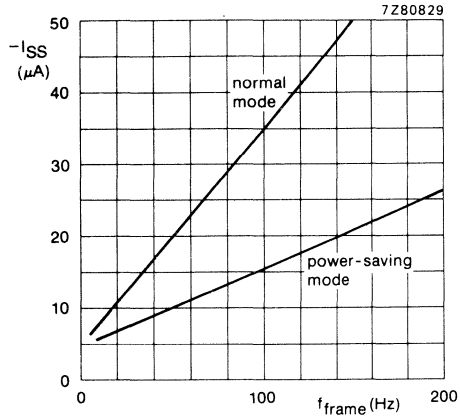
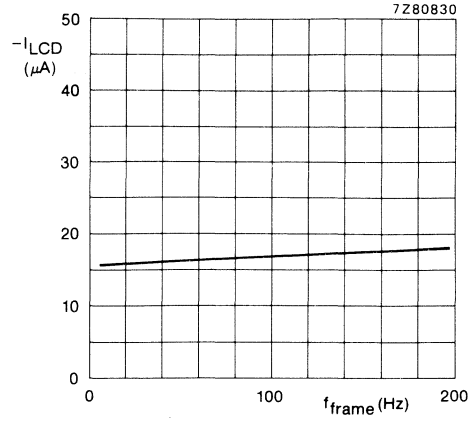


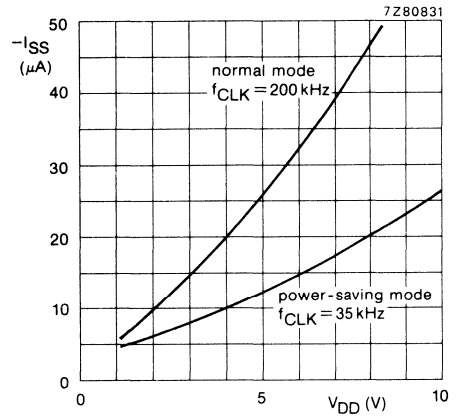
Fig.22 I^2C-bus timing waveforms.



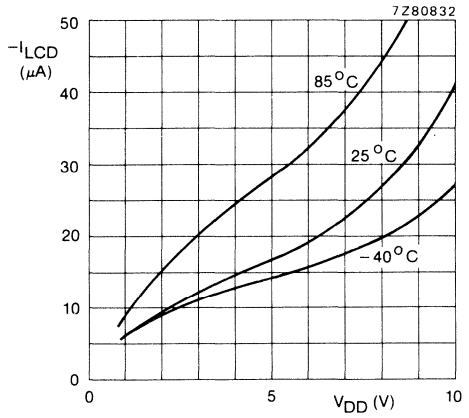
(a) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

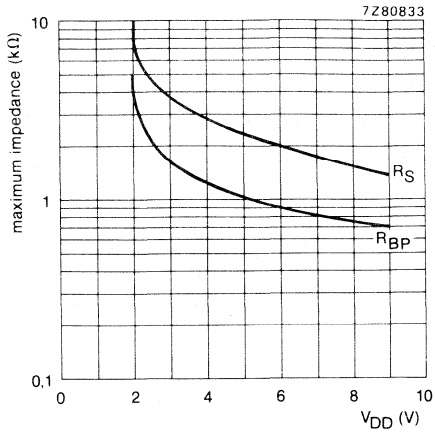


(c) V_{LCD} = 0 V; external clock;
T_{amb} = -40 to 85 °C.

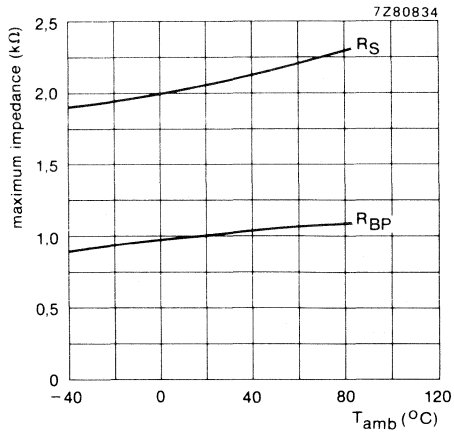


(d) V_{LCD} = 0 V; external clock;
f_{CLK} = nominal frequency.

Fig.23 Typical supply current characteristics.



(a) V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V.

Fig.24 Typical characteristics of LCD outputs.

APPLICATION INFORMATION

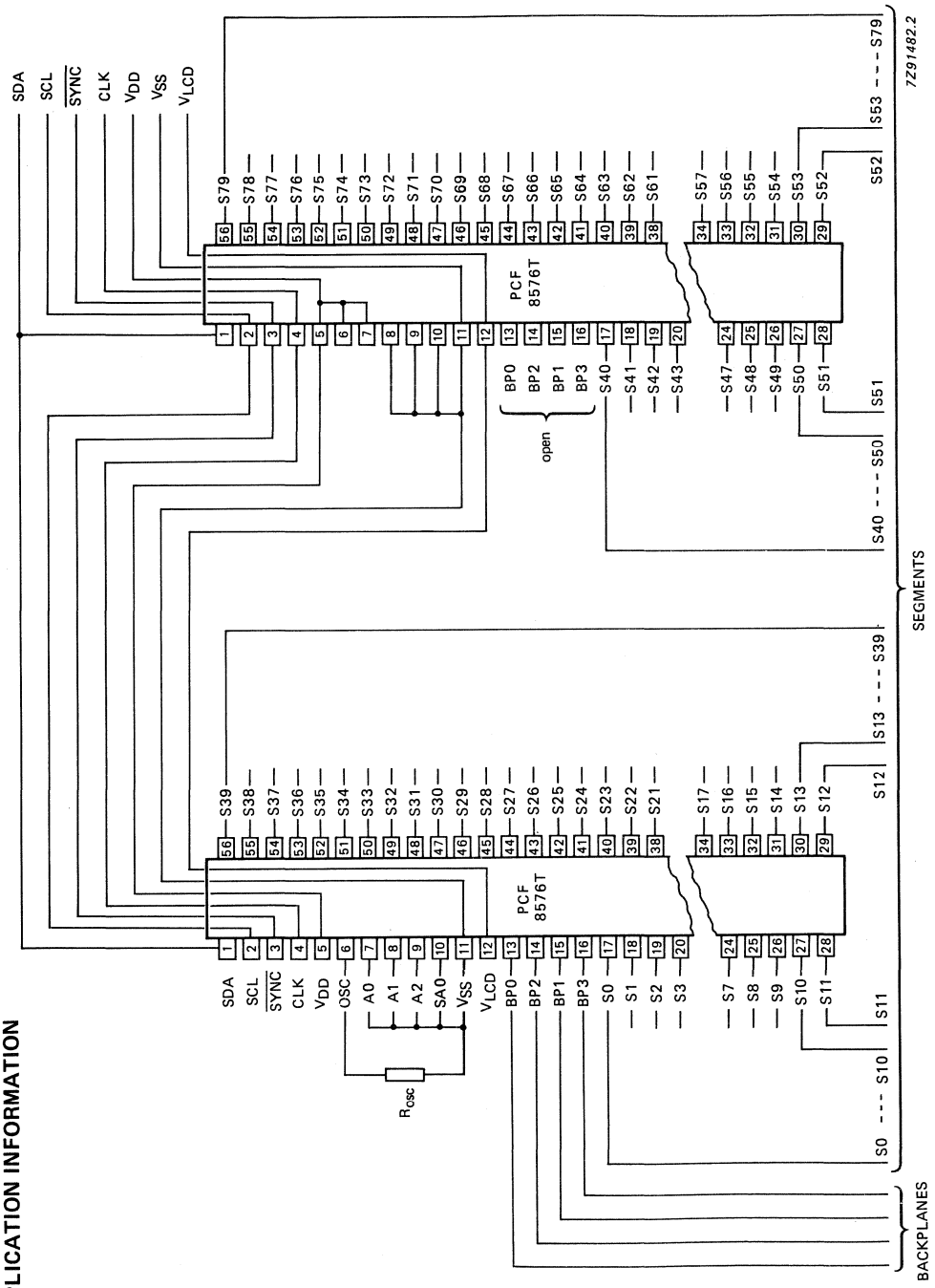


Fig.25 Single plane wiring of packaged PCF8576Ts.

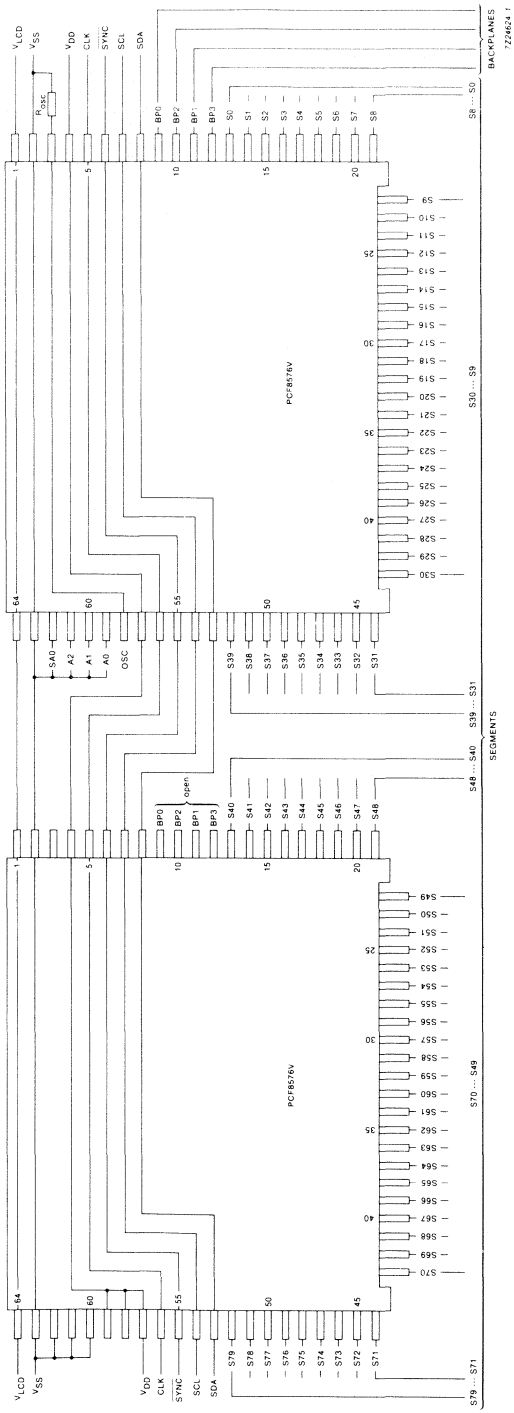


Fig.26 Single plane wiring of packaged PCF8576Vs.

APPLICATION INFORMATION (continued)

Chip-on-glass cascadability in single plane

In chip-on-glass technology, where driver devices are bonded directly onto the glass of the LCD, it is important that the devices may be cascaded without the crossing of conductors, but the paths of conductors can be continued on the glass under the chip. All of this is facilitated by the PCF8576 bonding pad layout (Fig.27). Pads needing bus interconnection between all PCF8576s of the cascade are V_{DD}, V_{SS}, V_{LCD}, CLK, SCL, SDA and $\overline{SYNC}$. These lines may be led to the corresponding pads of the next PCF8576 through the wide opening between V_{LCD} pad and the backplane output pads. The only bussed line that does not require a second opening to lead through to the next PCF8576 is V_{LCD}, being the cascade centre. The placing of V_{LCD} adjacent to V_{SS} allows the two supplies to be tied together.

Fig.28 shows the connection diagram for a cascaded PCF8576 application with single plane wiring. Note the use of the open space between the V_{LCD} pad and the backplane output pads to route V_{DD}, V_{SS}, CLK, SCL, SDA and $\overline{SYNC}$. The external connections may be made to either end of the cascade, wherever most convenient for the connector.

When an external clocking source is to be used, OSC of all devices should be tied to V_{DD}. The pads OSC, A0, A1, A2 and SA0 have been placed between V_{SS} and V_{DD} to facilitate wiring of oscillator, hardware subaddress and slave address.

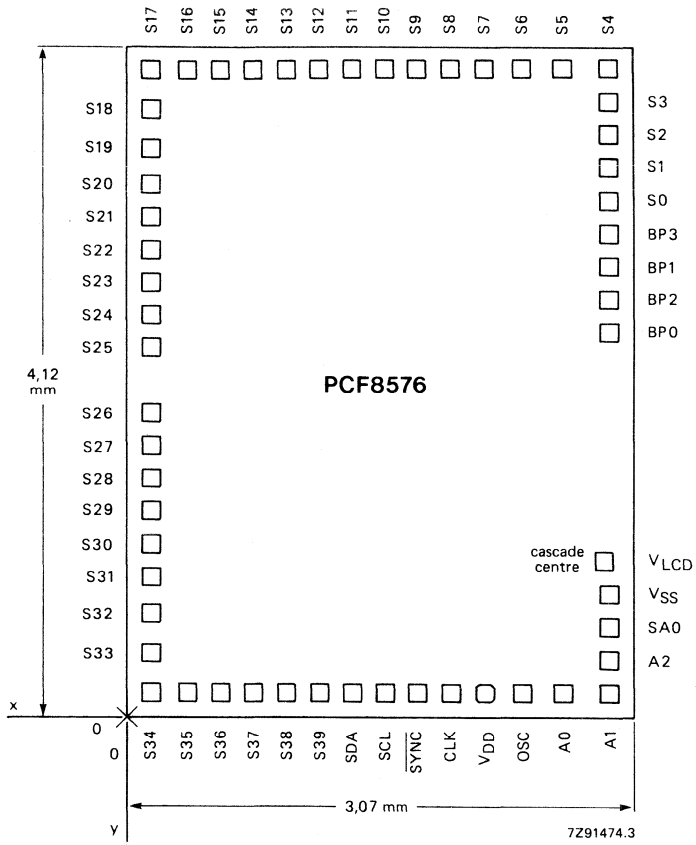


Fig.27 PCF8576 bonding pad locations.

APPLICATION INFORMATION (continued)

Bonding pad locations

All x/y coordinates are referenced to left-hand bottom corner (0/0, Fig.27).

Dimensions in μm

pad	x	y	
S34	160	160	bottom
S35	380		
S36	580		
S37	780		
S38	980		
S39	1180		
SDA	1380		
SCL	1580		
$\overline{\text{SYNC}}$	1780		
CLK	1980		
V_{DD}	2180		
OSC	2400		
A0	2640		
A1	2910	160	bottom
S17	160	3960	top
S16	380		
S15	580		
S14	780		
S13	980		
S12	1180		
S11	1380		
S10	1580		
S9	1780		
S8	1980		
S7	2180		
S6	2400		
S5	2640		
S4	2910	3960	top

pad	x	y	
S33	160	400	left
S32		640	
S31		860	
S30		1060	
S29		1260	
S28		1460	
S27		1660	
S26		1860	
S25		2260	
S24		2460	
S23		2660	
S22		2860	
S21		3060	
S20		3260	
S19		3480	
S18	160	3720	left
A2	2910	360	right
SA0		560	
V_{SS}	2910	760	
V_{LCD}	2880	960	
BP0	2910	2360	
BP2		2560	
BP1		2760	
BP3		2960	
S0		3160	
S1		3360	
S2		3560	
S3	2910	3760	right

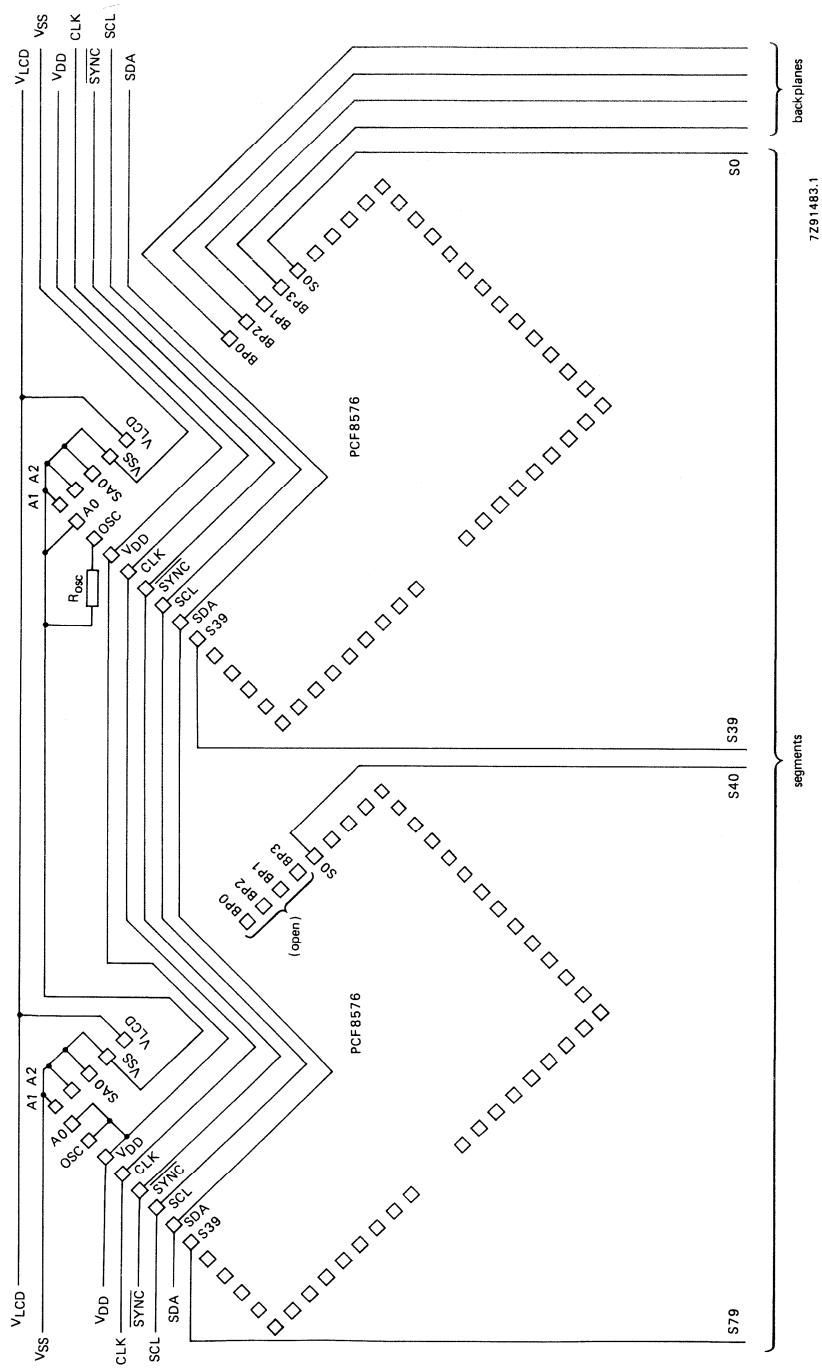
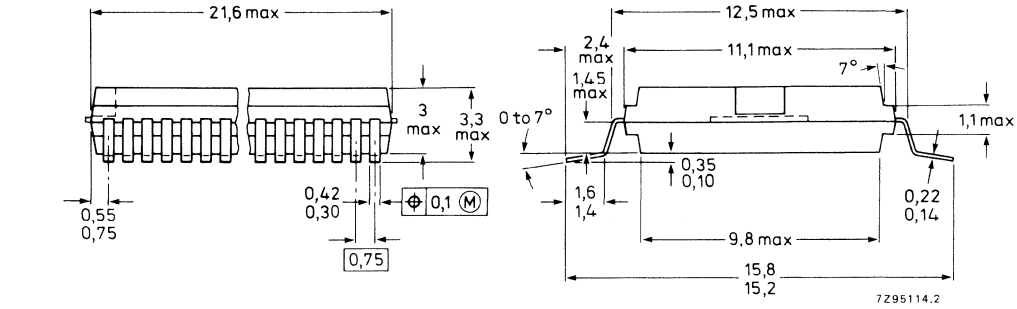
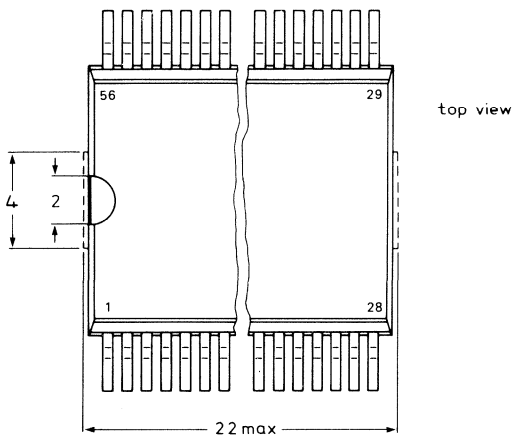


Fig.28 Chip-on-glass application; cascaded PCF8576s with single-plane wiring (viewed from back of chip).

56-LEAD MINI-PACK; PLASTIC (VSO56; SOT190)





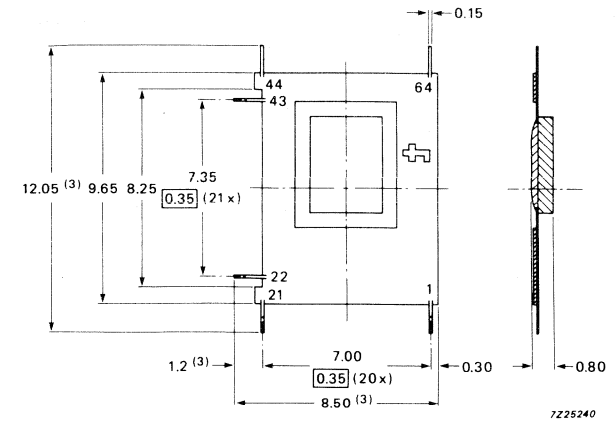
top view

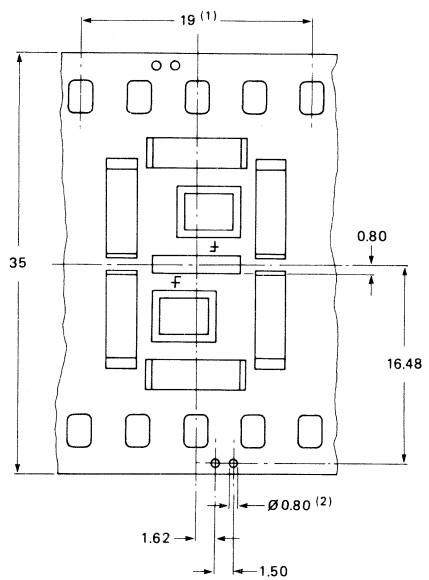
⊕ Positional accuracy.

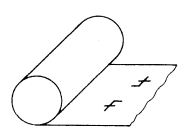
Ⓜ Maximum Material Condition.

Dimensions in mm

64-LEAD TAPE-AUTOMATED-BONDING (TAB) MODULE (SOT267A,C,D)







orientation on reel

7Z25241

Dimensions in mm

(1) 1 pattern = 4 perforation pitch intervals (contains two modules)
(2) Circuit-test holes
(3) Fixed by the user

SOLDERING PLASTIC MINI-PACKS

1. By hand-held soldering iron or pulse-heated solder tool

Fix the component by first soldering two, diagonally opposite end leads. Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

3. By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry paste and evaporate binding agent.

Pre-heating duration: 45 minutes at 45 °C.

4. Repairing soldered joints

The same precaution and limits apply as in (1) above.

SOLDERING TAB MODULES

1. Fluxing

(a) a flux that does not have to be removed,
or
(b) a water-soluble flux.

2. Soldering

The reflow soldering method using a pulse-heated soldering tool is usually suitable. Limit the soldering operation to 3 seconds at 250 °C at the leads.

3. Cleaning

Avoid cleaning if possible.

If cleaning is necessary, use cold or hot water. A detergent may be added to the water. Finally rinse with de-ionized water.

Do not use ultrasonic cleaning methods as these may damage the inner or outer leads.

Do not use solvents.

SUPERSEDES DATA OF MARCH 1989

LCD DIRECT / DUPLEX DRIVER WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8577 is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing and display memory switching (direct drive mode).
The PCF8577 and PCF8577C differ from the PCF8577A and PCF8577CA only in their slave addresses.
The PCF8577C/77CA is a low-voltage version of the PCF8577/77A.

Features

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Opering supply voltage:
  PCF8577/77A: 2.5 to 9 V
  PCF8577C/77CA: 2.5 to 6 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- Display memory switching in direct drive mode
- May be used as I²C-bus output expander
- System expansion up to 256 segments (512 segments with PCF8577A/CA)
- Power-on reset blanks display

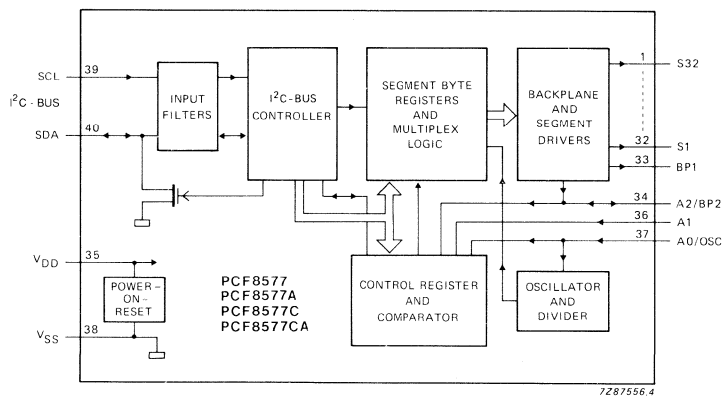


Fig.1 Block diagram.

PAKCAGE OUTLINES

PCF8577P, PCF8577AP	:	40-lead DIL; plastic (SOT129).
PCF8577CP, PCF8577CAP	:	
PCF8577T, PCF8577AT	:	40-lead mini-pack; plastic (VSO40; SOT158A).
PCF8577CT, PCF8577CAT	:	
PCF8577T, PCF8577AT	:	in blister tape.
PCF8577CT, PCF8577CAT	:	
PCF8577U/5	:	wafer unsawn.
PCF8577CU/5	:	
PCF8577U/10	:	chip on film-frame-carrier (FFC).
PCF8577CU/10	:	

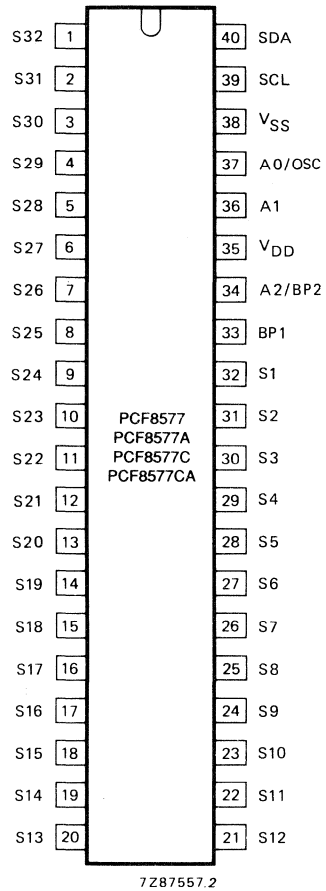


Fig.2 Pinning diagram.

PINNING

Supply

35	V_{DD}	positive supply
38	V_{SS}	negative supply

I^2C-bus

40	SDA	I^2C-bus data line
39	SCL	I^2C-bus clock line

Inputs

36	A1	hardware address line
37	A0/OSC	hardware address line/oscillator pin

Outputs

1 – 32	S32 – S1	segment outputs

Input – Output

34	A2/BP2	harware address line/cascade sync input/backplane output
33	BP1	cascade sync input/backplane output

FUNCTIONAL DESCRIPTION

Hardware subaddress A0, A1, A2

The hardware subaddress lines A0, A1, A2 are used to program the device subaddress for each PCF8577 on the bus. Lines A0 and A2 are shared with OSC and BP2 respectively to reduce pin-out requirements.

A0/OSC Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as HIGH (logic 1) when connected to V_{DD}.

A1 Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to V_{SS} or V_{DD} respectively.

A2/BP2 In the direct drive mode the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as LOW (logic 0) when connected to V_{SS} or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as HIGH (logic 1) when connected to V_{DD}.

In the duplex drive mode the second backplane signal BP2 is required and the A2 signal is undefined. In this mode device selection is made exclusively from lines A0 and A1.

Oscillator A0/OSC

The PCF8577 has a single-pin built-in oscillator which provides the modulation for the LCD segment driver outputs. One external resistor and one external capacitor are connected to the A0/OSC pin to form the oscillator. In an expanded system containing more than one PCF8577 the backplane signals are usually common to all devices and only one oscillator is needed. The devices which are not used for the oscillator are put into the cascade mode by connecting the A0/OSC pin to either V_{DD} or V_{SS} depending on the required state for A0. In the cascade mode each PCF8577 is synchronized from the backplane signal(s).

User-accessible registers

There are nine user-accesible 1-byte registers. The first is a control register which is used to control the loading of data into the segment byte registers and to select display options. The other eight are segment byte registers, split into two banks of storage, which store the segment data. The set of even numbered segment byte registers is called BANK A. Odd numbered segment byte registers are called BANK B.

There are two slave addresses, one for PCF8577/PCF8577C, and one for PCF8577A/PCF8577CA (see Fig.6). All addressed devices load the second byte into the control register and each device maintains an identical copy of the control byte in the control register at all times (see I²C-bus protocol Fig.7), i.e. all addressed devices respond to control commands sent on the bus.

The control register is shown in more detail in Fig.3. The least-significant bits select which device and which segment byte register is loaded next. This part of the register is therefore called the Segment Byte Vector (SBV).

The upper three bits of the SBV (V5 to V3) are compared with the hardware subaddress input signals A2, A1 and A0. If they are the same then the device is enabled for loading, if not the device ignores incoming data but remains active.

The three least-significant bits of the SBV (V2 to V0) address one of the segment byte registers within the enabled chip for loading segment data.

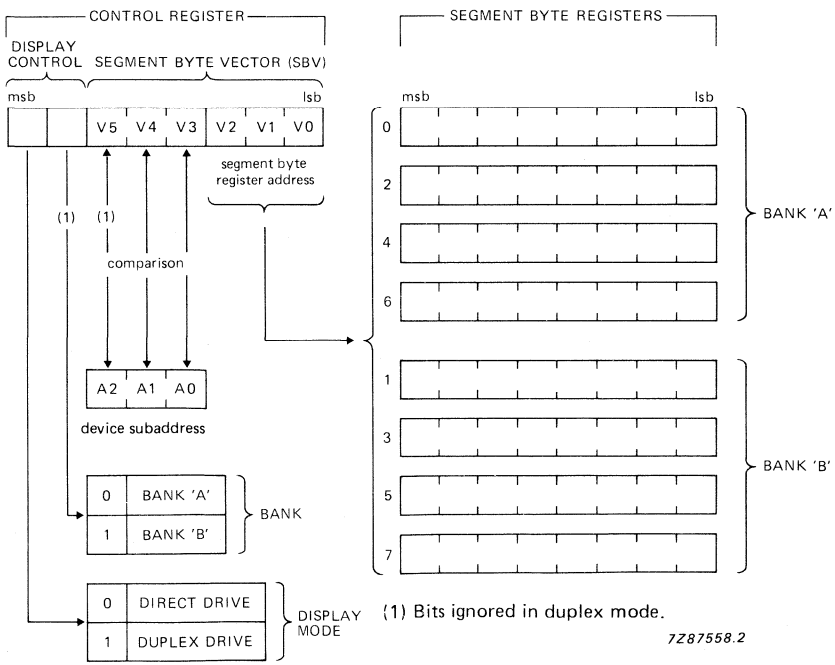


Fig.3 PCF8577 register organization.

FUNCTIONAL DESCRIPTION (continued)

The control register also has two display control bits. These bits are named MODE and BANK. The MODE bit selects whether the display outputs are configured for direct or duplex drive displays. The BANK bit allows the user to display BANK A or BANK B.

Auto-incremented loading

After each segment byte is loaded the SBV is incremented automatically. Thus auto-incremented loading occurs if more than one segment byte is received in a data transfer.

Since the SBV addresses both device and segment registers in all addressed chips, auto-incremented loading may proceed across device boundaries provided that the hardware subaddresses are arranged contiguously.

Direct drive mode

The PCF8577 is set to the direct drive mode by loading the MODE control bit with logic 0. In this mode only four bytes are needed to store the data for the 32 segment drivers. Setting the BANK bit to logic 0 selects even bytes (BANK A); setting the BANK bit to logic 1 selects odd bytes (BANK B).

In the direct drive mode the SBV is auto-incremented by two after the loading of each segment byte register. This means that auto-incremented loading of BANK A or BANK B is possible. Either bank may be completely or partially loaded irrespective of which bank is being displayed. Direct drive output waveforms are shown in Fig.4.

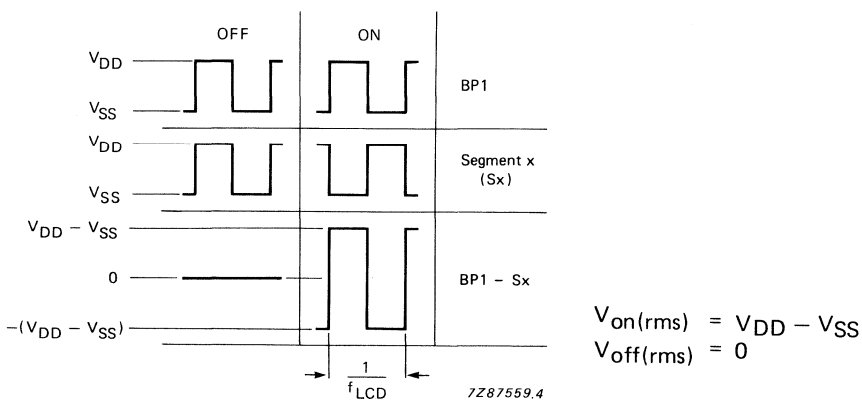


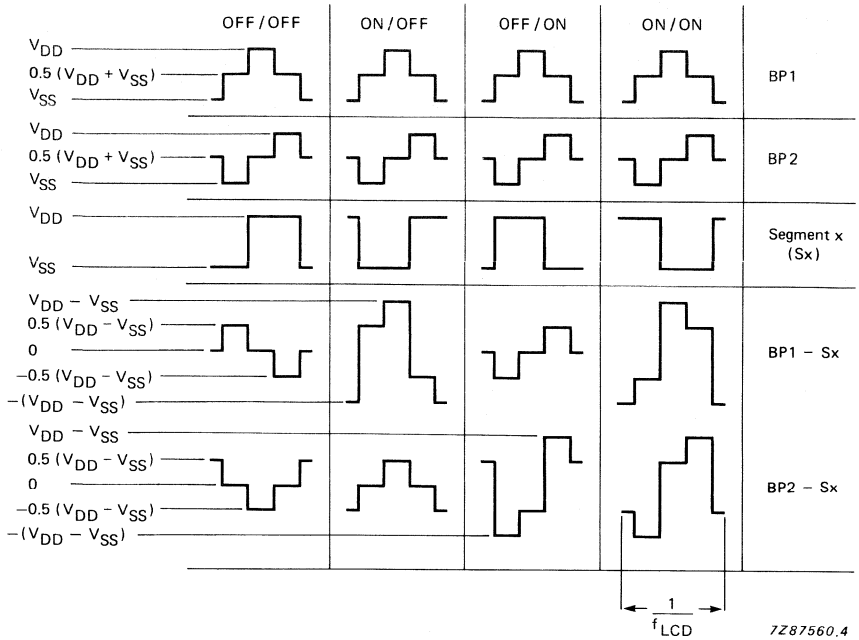
Fig.4 Direct drive mode display output waveforms.

Duplex mode

The PCF8577 is set to the duplex mode by loading the MODE bit with logic 1. In this mode a second backplane signal (BP2) is needed and pin A2/BP2 is used for this; therefore A2 and its equivalent SBV bit V5 are undefined. The SBV auto-increments by one between loaded bytes.

All of the segment bytes are needed to store data for the 32 segment drivers and the BANK bit is ignored.

Duplex mode output waveforms are shown in Fig.5.



$$V_{on(rms)} = 0.791\,(V_{DD} - V_{SS})$$
$$V_{off(rms)} = 0.354\,(V_{DD} - V_{SS})$$
$$\frac{V_{on(rms)}}{V_{off(rms)}} = 2.236$$

Fig.5 Duplex mode display output waveforms.

DEVELOPMENT DATA

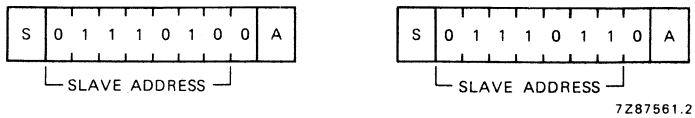
Power-on reset

At power-on reset the PCF8577 resets to a defined starting condition as follows:

1. Both backplane outputs are set to V_{SS} in master mode; to 3-state in cascade mode.
2. All segment outputs are set to V_{SS}.
3. The segment byte registers and control register are cleared.
4. The I²C-bus interface is initialized.

Slave address

The PCF8577 slave addresses are shown in Fig.6.



(a) PCF8577/PCF8577C (b) PCF8577A/PCF8577CA

Fig.6 PCF8577 slave addresses.

Before any data is transmitted on the I^2C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

I^2C-bus protocol

The PCF8577 I^2C-bus protocol is shown in Fig.7.

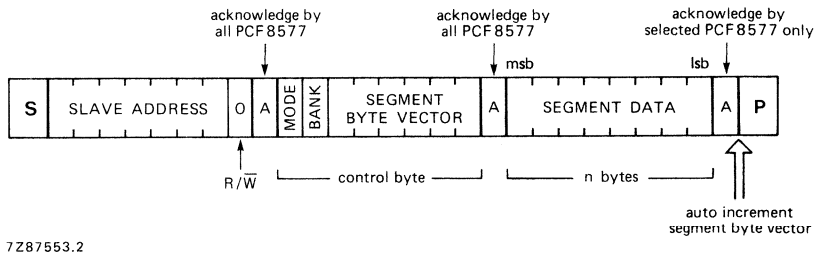


Fig.7 I^2C-bus protocol.

The PCF8577 is a slave receiver and has a fixed slave address (Fig.6). All PCF8577s with the same slave address acknowledge the slave address in parallel. The second byte is always the control byte and is loaded into the control register of each PCF8577 on the bus. All addressed devices acknowledge the control byte. Subsequent data bytes are loaded into the segment registers of the selected device. Any number of data bytes may be loaded in one transfer and in an expanded system rollover of the SBV from 111 111 to 000 000 is allowed. If a stop (P) condition is given after the control byte acknowledge the segment data remains unchanged. This allows the BANK bit to be toggled without changing the segment register contents. During loading of segment data only the selected PCF8577 gives an acknowledge. Loading is terminated by generating a stop (P) condition.

Display memory mapping

The mapping between the eight segment registers and the segment outputs S1 to S32 is shown in Tables 1 and 2.

Since only one register bit per segment is needed in the direct drive mode, the BANK bit allows swapping of display information. If BANK is set to logic 0 even bytes (BANK A) are displayed; if BANK is set to logic 1 odd bytes (BANK B) are displayed. BP1 is always used for the backplane output in the direct drive mode.

Table 1 Segment byte-segment driver mapping in the direct drive mode

MODE	BANK	V2	V1	V0	segment register / bit	MSB 7	6	5	4	3	2	1	LSB 0	backplane
0	0	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	1	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	0	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	1	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	0	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	1	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	0	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
0	1	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP1

Mapping example: bit 0 of register 7 controls the LCD segment S25 if BANK bit is a logic 1.

In duplex mode even bytes (BANK A) correspond to backplane 1 (BP1) and odd bytes (BANK B) correspond to backplane 2 (BP2).

Table 2 Segment byte-segment driver mapping in the duplex mode

MODE	BANK	V2	V1	V0	segment register / bit	MSB 7	6	5	4	3	2	1	LSB 0	backplane
1	x	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
1	x	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP2
1	x	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
1	x	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP2
1	x	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
1	x	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP2
1	x	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
1	x	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP2

x = don't care.

Mapping example: bit 7 of register 5 controls the LCD segment S24/BP2.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

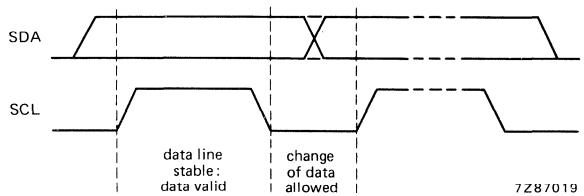


Fig.8 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

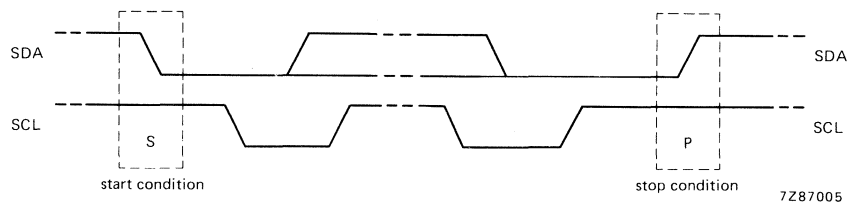


Fig.9 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

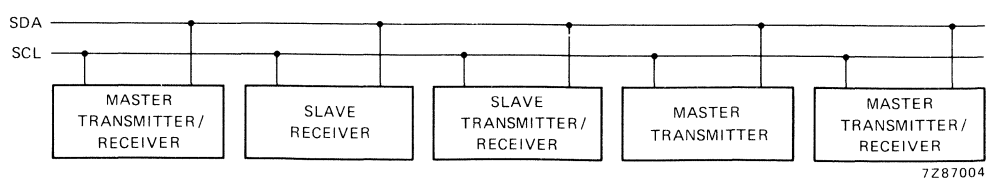


Fig.10 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

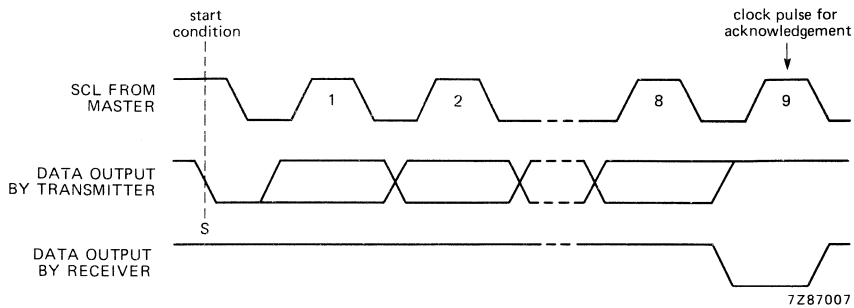


Fig.11 Acknowledgement on the I²C-bus.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage				
PCF8577/PCF8577A	V_{DD}	−0.5	+ 11.0	V
PCF8577C/PCF8577CA	V_{DD}	−0.5	+ 8.0	V
Voltage on pin	V_I	−0.5	V_{DD} + 0.5	V
V_{DD} or V_{SS} current	I_{DD}; I_{SS}	−50	+ 50	mA
DC input current	I_I	−20	+ 20	mA
DC output current	I_O	−25	+ 25	mA
Power dissipation per package	P_{tot}	−	500*	mW
Power dissipation per output	P_o	−	100	mW
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* Derate 7.7 mW/K when $T_{amb} > 60$ °C.

DC CHARACTERISTICS

V_{DD} = 2.5 to 9.0 V (PCF8577/77A) or 2.5 to 6.0 V (PCF8577C/77CA); V_{SS} = 0 V;
T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.*	max.	unit
Supply						
Supply voltage						
PCF8577/77A		V_{DD}	2.5	–	9.0	V
PCF8577C/77CA		V_{DD}	2.5	–	6.0	V
Supply current	non specified inputs at V_{DD} or V_{SS}					
at f_{SCL} = 100 kHz	no load; R_{OSC} = 1 MΩ; C_{OSC} = 680 pF					
PCF8577/77A		I_{DD1}	–	80	250	μA
PCF8577C/77CA		I_{DD1}	–	50	125	μA
at f_{SCL} = 0	no load; R_{OSC} = 1 MΩ; C_{OSC} = 680 pF					
PCF8577/77A		I_{DD2}	–	25	150	μA
PCF8577C/77CA		I_{DD2}	–	25	75	μA
at f_{SCL} = 0	no load; R_{OSC} = 1 MΩ; C_{OSC} = 680 pF; V_{DD} = 5 V; T_{amb} = 25 °C	I_{DD3}	–	25	40	μA
at f_{SCL} = 0	no load; direct mode; A0/OSC = V_{DD}; V_{DD} = 5 V; T_{amb} = 25 °C	I_{DD4}	–	10	20	μA
Power-on reset level	note 1	V_{POR}	–	1.1	2.0	V
Input A0						
Input voltage LOW		V_{IL1}	0	–	0.05	V
Input voltage HIGH		V_{IH1}	V_{DD}−0.05	–	V_{DD}	V
Input A1						
Input voltage LOW		V_{IL2}	0	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH2}	0.7 V_{DD}	–	V_{DD}	V
Input A2						
Input voltage LOW		V_{IL3}	0	–	0.10	V
Input voltage HIGH		V_{IH3}	V_{DD}−0.10	–	V_{DD}	V

* Typical conditions: V_{DD} = 5 V; T_{amb} = 25 °C.

parameter	conditions	symbol	min.	typ.*	max.	unit
Inputs SCL; SDA						
Input voltage LOW		V_{IL4}	0	–	0.8	V
Input voltage HIGH						
PCF8577/77A		V_{IH4}	2.0	–	9.0	V
PCF8577C/77CA		V_{IH4}	2.0	–	6.0	V
Input capacitance	note 2	C_I	–	–	7	pF
Output SDA						
Output current LOW	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL}	3.0	–	–	mA
A1; SCL; SDA						
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\pm I_{L1}$	–	–	1	μA
A2/BP2; BP1						
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\pm I_{L2}$	–	–	5	μA
A2/BP2						
Pull-down current	$V_I = V_{DD}$	$-I_{L2}$	–	1.5	5	μA
A0/OSC						
Leakage current	$V_I = V_{DD}$	$-I_{L3}$	–	–	1	μA
Oscillator						
Start-up current	$V_I = V_{SS}$	I_{OSC}	–	1.2	5	μA
LCD outputs						
DC component of LCD driver		$\pm V_{BP}$	–	20	–	mV
Segment output current	V_{DD} = 5 V; note 6					
PCF8577/77A	V_{OL} = 0.4 V	I_{OL1}	0.3	–	–	mA
PCF8577C/77CA	V_{OL} = 0.8 V	I_{OL1}	0.3	–	–	mA
PCF8577/77A	$V_{OH} = V_{DD}-0.4$ V	$-I_{OH1}$	0.3	–	–	mA
PCF8577C/77CA	$V_{OH} = V_{DD}-0.8$ V	$-I_{OH1}$	0.3	–	–	mA
Backplane output resistance (BP1; BP2)	$V_O = V_{SS}$, V_{DD}, $(V_{SS}+V_{DD})/2$; note 3	R_{BP}	–	0.4	5	kΩ

* Typical conditions: V_{DD} = 5 V; T_{amb} = 25 °C.

DEVELOPMENT DATA

AC CHARACTERISTICS (note 4)

V_{DD} = 2.5 to 9.0 V (PCF8577/77A) or 2.5 to 6.0 V (PCF8577C/77CA);
T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.*	max.	unit
Display frequency	C_{OSC} = 680 pF; R_{OSC} = 1 MΩ	f_{LCD}	65	90	120	Hz
Driver delays with test loads	V_{DD} = 5 V	t_{BS}	–	20	100	μs
I²C-bus						
SCL clock frequency		f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	note 5	t_{SW}	–	–	100	ns
Bus free time		t_{BUF}	4.7	–	–	μs
Start condition set-up time		$t_{SU;STA}$	4.0	–	–	μs
Start condition hold time		$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time		t_{LOW}	4.7	–	–	μs
SCL HIGH time		t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time		t_r	–	–	1.0	μs
SCL and SDA fall time		t_f	–	–	0.3	μs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Data hold time		$t_{HD;DAT}$	0	–	–	ns
Stop condition set-up time		$t_{SU;STO}$	4.0	–	–	μs

Notes to the characteristics

1. Resets all logic when $V_{DD} < V_{POR}$.
2. Periodically sampled, not 100% tested.
3. Outputs measured one at a time; V_{DD} = 5 V; I_{load} = 100 μA.
4. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
5. PCF8577C/CA 25 °C only.
6. Outputs measured one at a time.

* Typical conditions: V_{DD} = 5 V; T_{amb} = 25 °C.

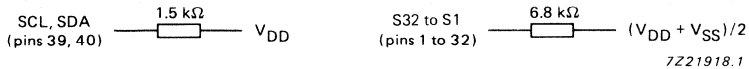


Fig.12 Test loads.

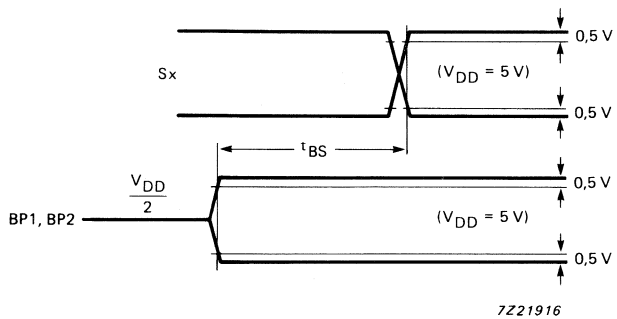


Fig.13 Driver timing waveforms.

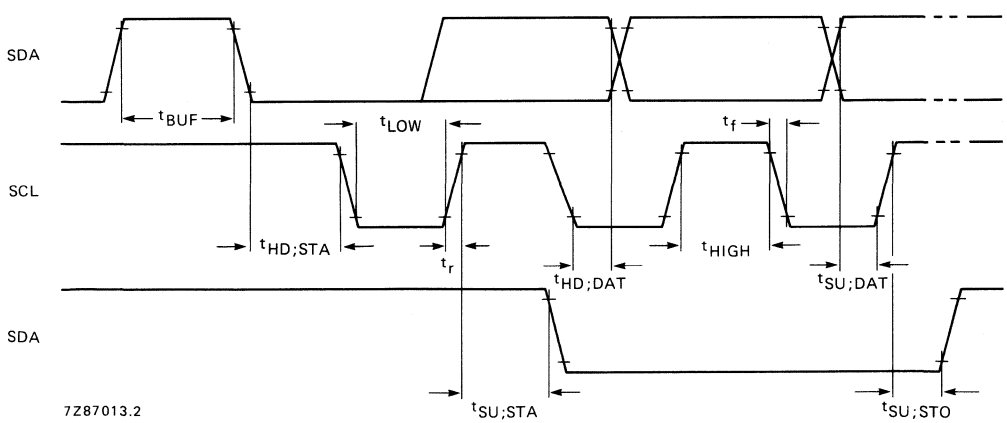


Fig.14 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

APPLICATION INFORMATION

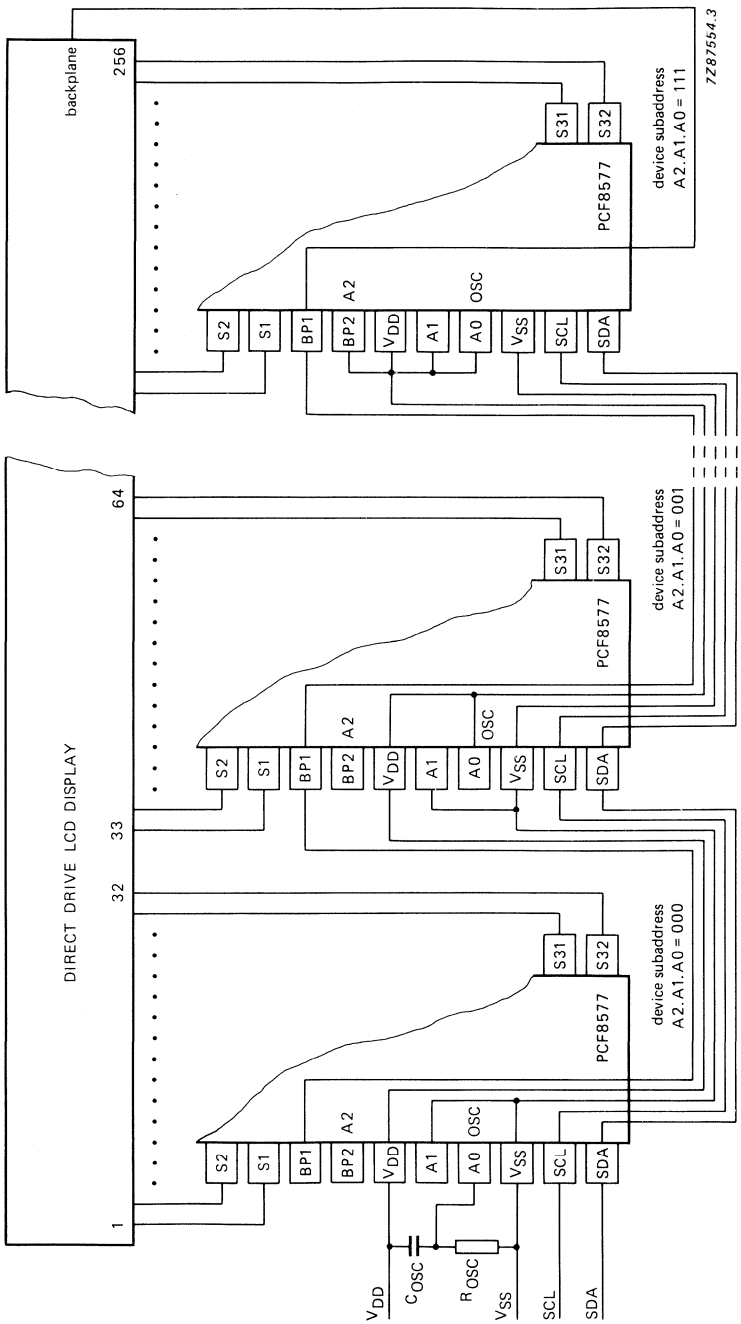


Fig.15 Direct drive display; expansion to 256 segments using eight PCF8577.

DEVELOPMENT DATA

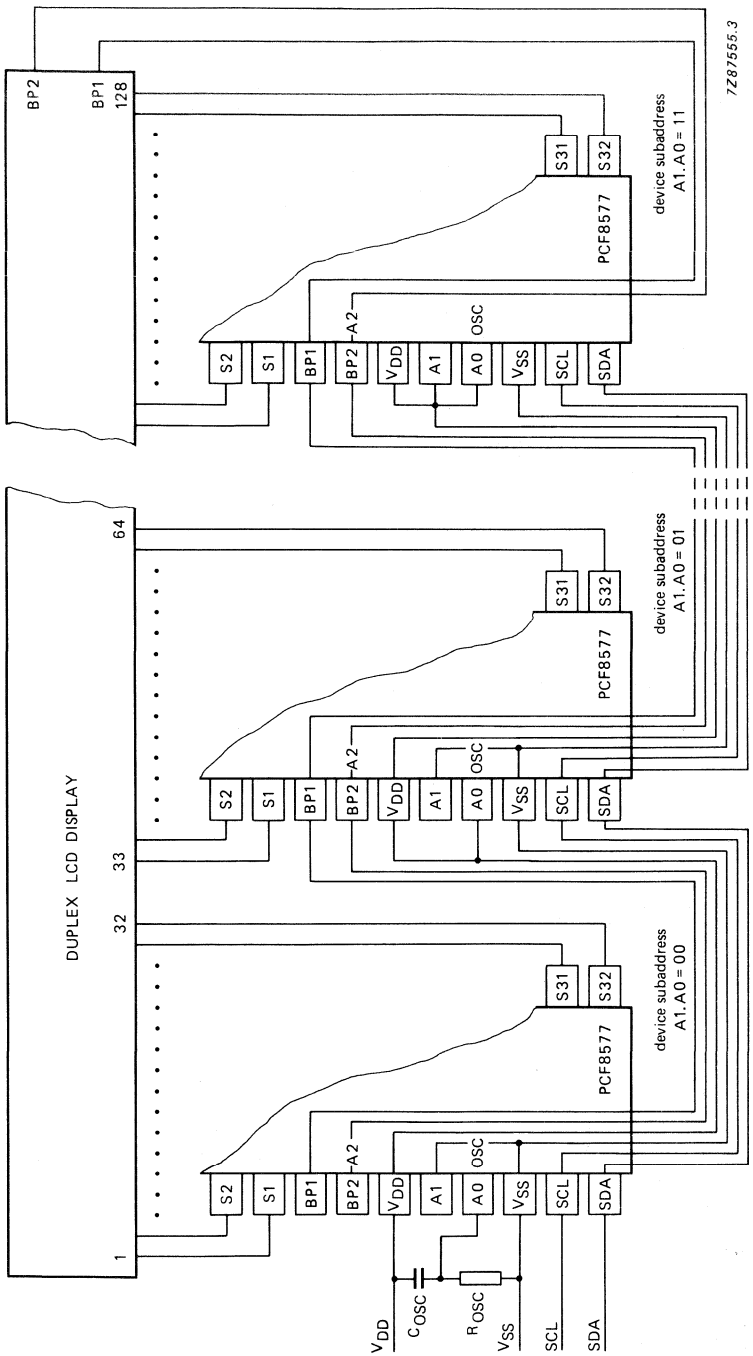
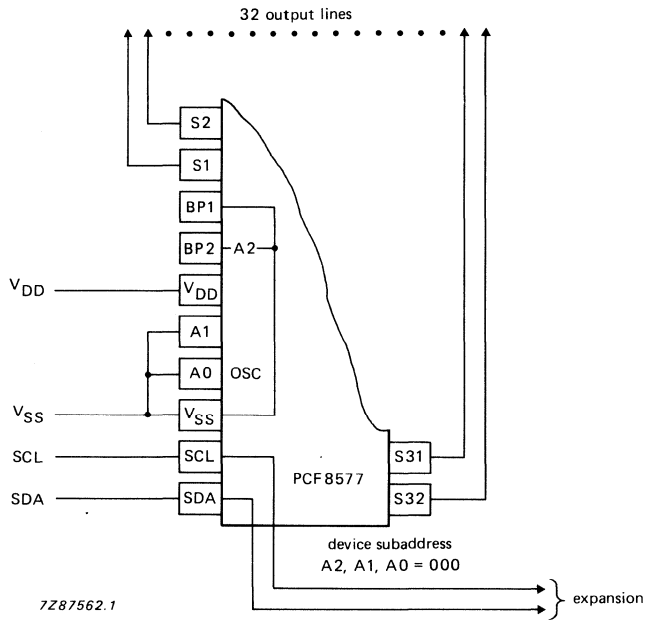


Fig.16 Duplex display; expansion to 2 x 128 segments using four PCF8577.

APPLICATION INFORMATION (continued)



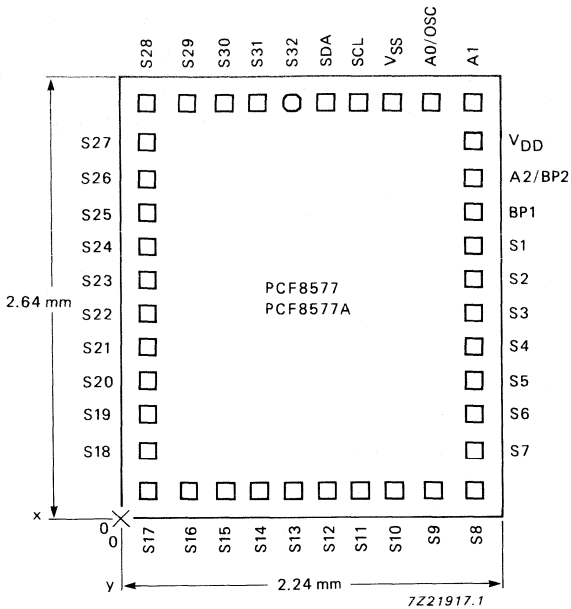
Notes

1. MODE bit must always be set to logic 0 (direct drive).
2. BANK switching is permitted.
3. BP1 must always be connected to V_{SS} and A0/OSC must be connected to either V_{DD} or V_{SS} (no LCD modulation).

Fig.17 Use of PCF8577 as 32-bit output expander in I²C-bus application.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS PCF8577/77A



Chip area: 5.91 mm²

Bonding pad dimensions: 120 μm x 120 μm

Fig.18 Bonding pad locations; PCF8577/PCF8577A.

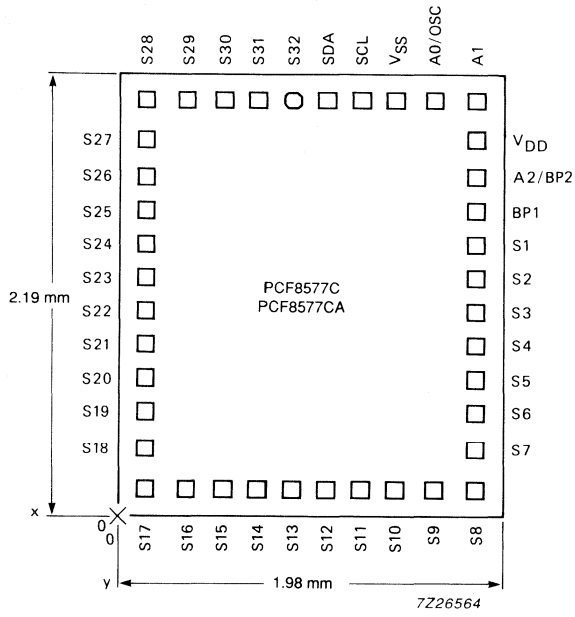
Table 3 Bonding pad locations; PCF8577/77A (dimensions in μm)

All x/y coordinates are referenced to bottom left corner, see Fig.18.

pad	X	Y	pad	X	Y
S32	1020	2480	S12	1220	160
S31	820	2480	S11	1420	160
S30	620	2480	S10	1620	160
S29	400	2480	S9	1840	160
S28	160	2480	S8	2080	160
S27	160	2240	S7	2080	400
S26	160	2020	S6	2080	620
S25	160	1820	S5	2080	820
S24	160	1620	S4	2080	1020
S23	160	1420	S3	2080	1220
S22	160	1220	S2	2080	1420
S21	160	1020	S1	2080	1620
S20	160	820	BP1	2080	1820
S19	160	620	A2/BP2	2080	2020
S18	160	400	V_{DD}	2080	2240
S17	160	160	A1	2080	2480
S16	400	160	A0/OSC	1840	2480
S15	620	160	V_{SS}	1620	2480
S14	820	160	SCL	1420	2480
S13	1020	160	SDA	1220	2480

DEVELOPMENT DATA

CHIP DIMENSIONS AND BONDING PAD LOCATIONS PCF8577C/77CA



Chip area: 4.34 mm^2

Bonding pad dimensions: 110 μm x 110 μm

Fig.19 Bonding pad locations; PCF8577C/77CA.

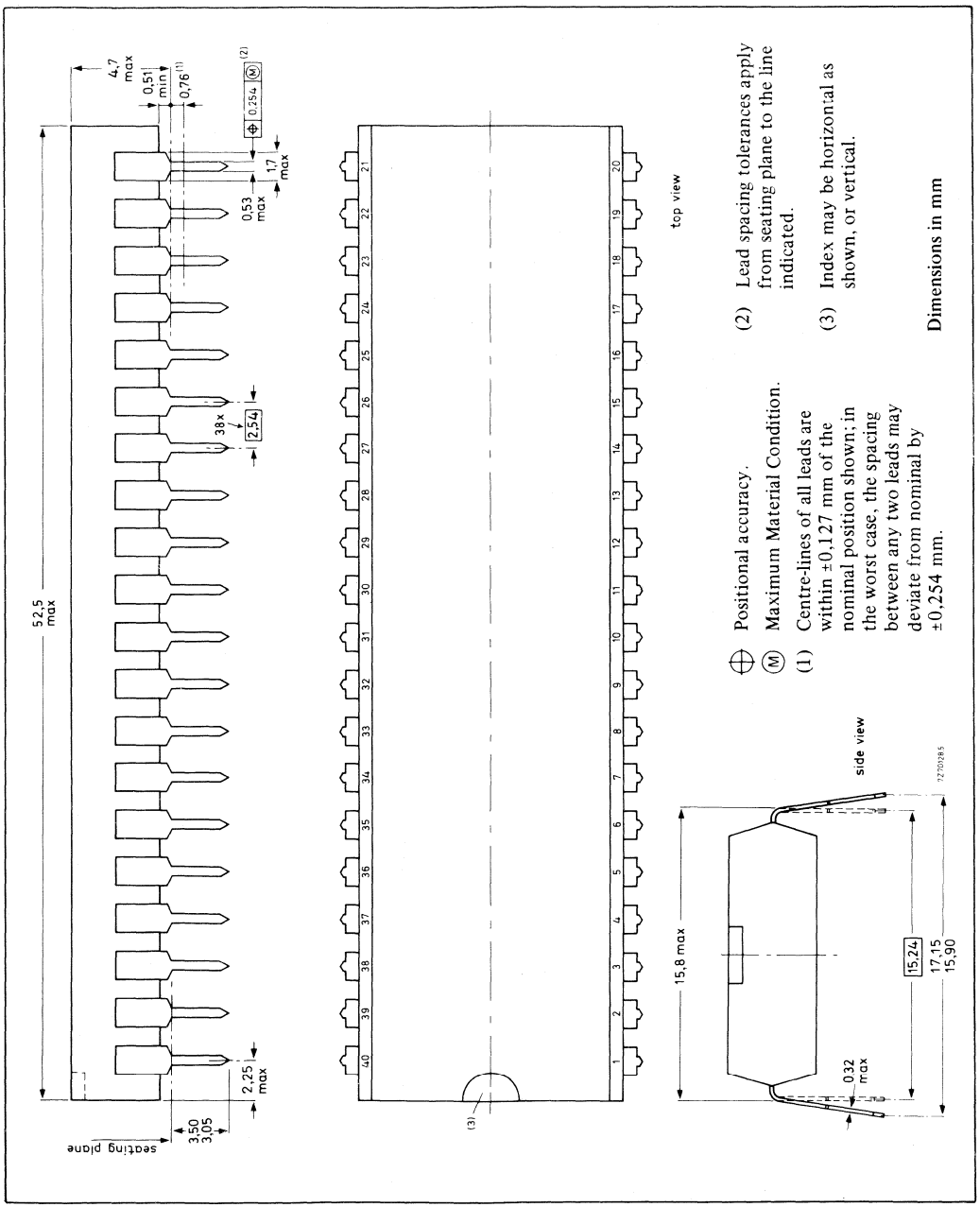
Table 4 Bonding pad locations; PCF8577C/77CA (dimensions in μm)

All x/y coordinates are referenced to bottom left corner, see Fig.19.

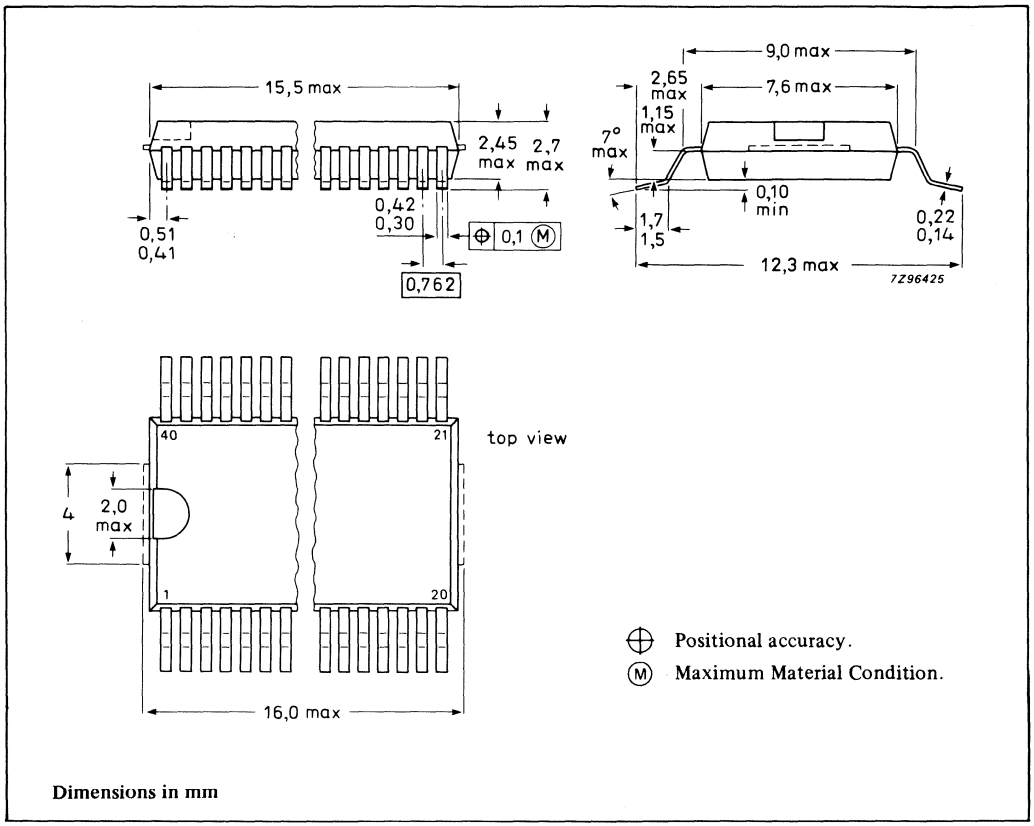
pad	X	Y	pad	X	Y
S32	904	2036	S12	1075	154
S31	733	2036	S11	1246	154
S30	562	2036	S10	1417	154
S29	391	2036	S9	1588	154
S28	154	2036	S8	1826	154
S27	154	1864	S7	1826	325
S26	154	1693	S6	1826	496
S25	154	1522	S5	1826	667
S24	154	1351	S4	1826	838
S23	154	1180	S3	1826	1009
S22	154	1009	S2	1826	1180
S21	154	838	S1	1826	1351
S20	154	667	BP1	1826	1522
S19	154	496	A2/BP2	1826	1693
S18	154	325	V_{DD}	1826	1846
S17	154	154	A1	1826	2036
S16	391	154	A0/OSC	1588	2036
S15	562	154	V_{SS}	1417	2036
S14	733	154	SCL	1246	2036
S13	904	154	SDA	1075	2036

DEVELOPMENT DATA

40-LEAD DUAL IN-LINE; PLASTIC (SOT129)



40-LEAD MINI-PACK; PLASTIC (VSO40; SOT158A)



Dimensions in mm

SOLDERING PLASTIC MINI-PACKS

1. By hand-held soldering iron or pulse-heated solder tool

Fix the component by first soldering two, diagonally opposite end leads. Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

3. By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry paste and evaporate binding agent.

Pre-heating duration: 45 minutes at 45 °C.

4. Repairing soldered joints

The same precaution and limits apply as in (1) above.

SOLDERING PLASTIC DUAL IN-LINE PACKAGES

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

LCD FLAT-PANEL ROW/COLUMN DRIVER

GENERAL DESCRIPTION

The PCF2201 is a row or column LCD driver, designed to drive LCD flat-panels at multiplex rates of up to 1 : 256. The PCF2201 converts serial or parallel 4-bit display data into parallel LCD drive waveforms, capable of driving up to 81 rows or 80 columns of an LCD matrix. The PCF2201 is cascadable, enabling it to drive any LCD flat-panel matrix. The PCF2201 is controlled by an alphanumeric/graphic controller.

Features

- Row or column drive capability
- 80 data latches
- 81 stage bidirectional shift register
- 81 LCD drive outputs
- Proprietary margin control drive output
- Low drive impedance
- LCD drive voltage of up to 25 V
- 5 V logic compatibility
- High speed operation (4 MHz)
- Multiplex rates of up to 1 : 256
- Externally adjusted bias voltages
- Maximum LCD voltage and V_{DD} may be separated
- 64/65 pin programmable output operation mode
- Low power consumption
- Overall flat-panel power consumption minimized
- Pin programmable right/left orientation for convenience of flat-panel construction
- Optimized pinning for single plane wiring
- Space-saving 120-lead Tape-Automated Bonding package
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINE

PCF2201V: 120-lead Tape-Automated Bonding (TAB) module (SOT235)

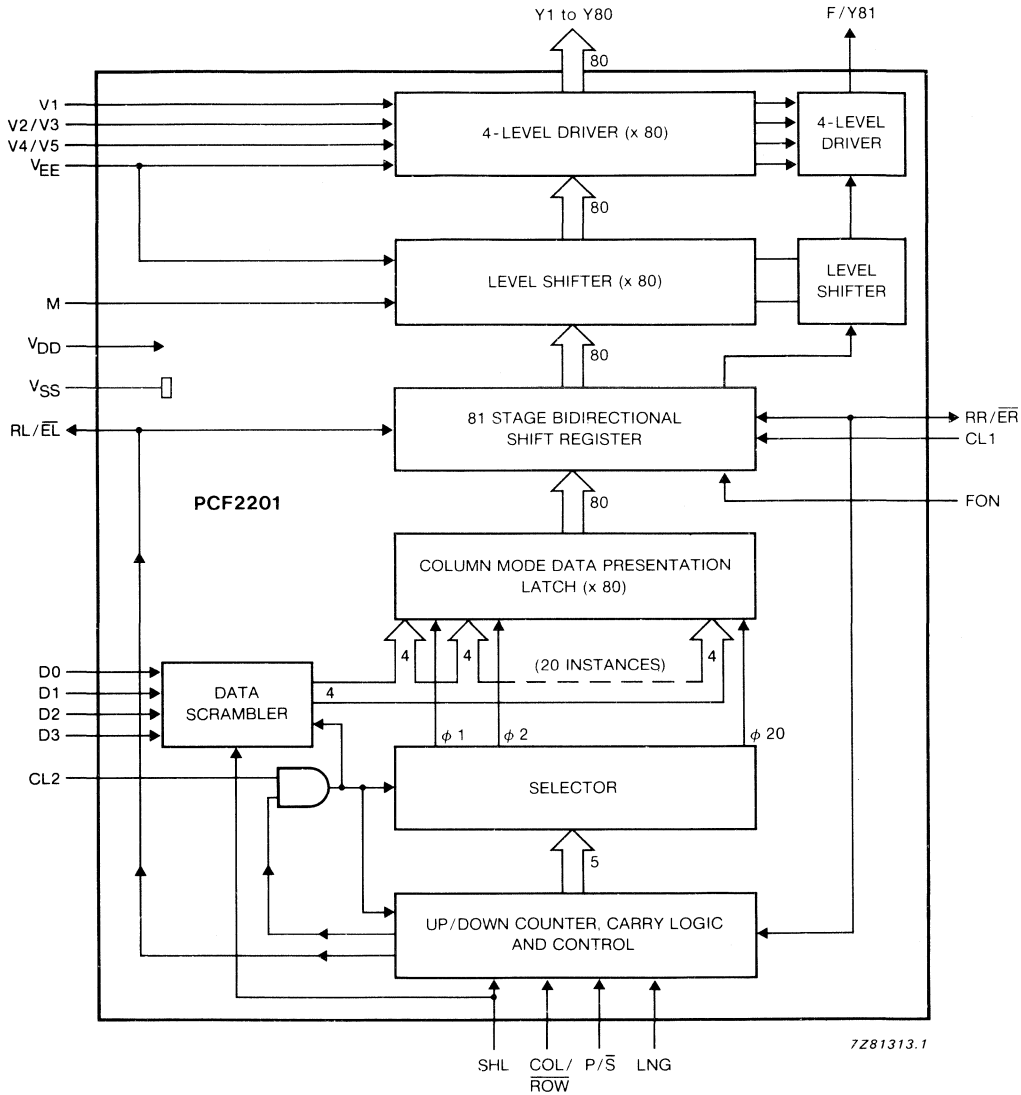
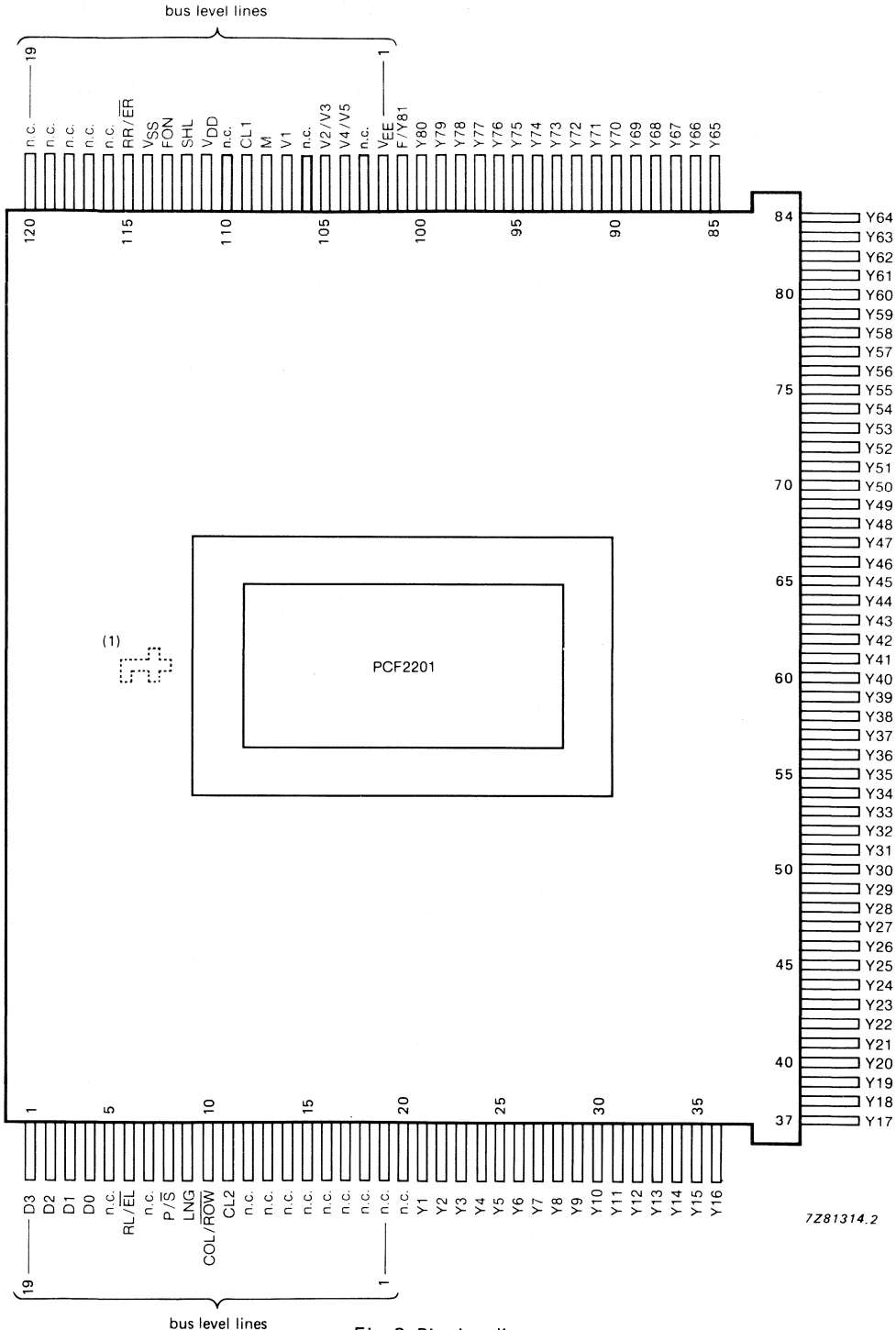


Fig. 1 Block diagram.

DEVELOPMENT DATA



bus level lines

(1) mark orientation

Fig. 2 Pinning diagram.

PINNING FUNCTIONS

mnemonic	I/O	function
V_{DD}	P	Positive supply voltage (5 V)
V_{SS}	P	Logic ground (0 V)
V_1	P	Most positive LCD supply voltage ($\leqslant V_{DD}$), selection level
V_2/V_3	P	Upper non-selection level for row (V2) or column (V3) driver
V_4/V_5	P	Lower non-selection level for row (V5) or column (V4) driver
V_{EE}	P	Most negative LCD supply voltage (−20 V), selection level
Y1 to Y80	O	Liquid crystal driver outputs
CL1	I	Clock for 81 stage bidirectional shift register Loads parallel data from the data presentation latch and frame control in column driver mode Shifts data in row driver mode Negative edge triggered
CL2	I	Data transfer clock in column driver modes Data must be valid on the negative edge of CL2 Unused in row driver mode (may be left open)
COL/$\overline{ROW}$	I	Column/row driver mode select
P/$\overline{S}$	I	Parallel/serial mode select for column drivers Tie to V_{SS} in row driver mode
SHL	I	Shift direction select
D0 to D3	I	Data inputs in column driver modes Unused in row driver mode (may be left open) Filling order:

COL/$\overline{ROW}$	P/$\overline{S}$	SHL	D0	D1	D2	D3
H	L	L	Y1, Y2, Y3,.	unused	unused	unused
H	L	H	Y80, Y79,...	(may be left open)	(may be left open)	(may be left open)
H	H	L	Y1, Y5, Y9,.	Y2, Y6, Y10,.	Y3, Y7, Y11,.	Y4, Y8, Y12,..
H	H	H	Y80, Y76,...	Y79, Y75,....	Y78, Y74,....	Y77, Y73,.....

Also in the **serial** column driver mode, a multiple of 4 data bits must always be transferred. Add dummy bits if necessary

DEVELOPMENT DATA

<table>
<tr><th>mnemonic</th><th>I/O</th><th>function</th></tr>
<tr><td>RL/$\overline{EL}$
RR/$\overline{ER}$</td><td>I/O</td><td>Left/right serial input/outputs in row driver mode, left/right enable input/outputs in column driver modes
<table>
<tr><th>COL/$\overline{ROW}$</th><th>P/$\overline{S}$</th><th>SHL</th><th>RL/$\overline{EL}$</th><th>RR/$\overline{ER}$</th><th>comments</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>I</td><td>O</td><td>shift direction:
RL/$\overline{EL}$ –> RR/$\overline{ER}$ (Y1 –> F/Y81)</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>O</td><td>I</td><td>shift direction:
RR/$\overline{ER}$ –> RL/$\overline{EL}$ (F/Y81 –> Y1)</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>I</td><td>O</td><td>RR/$\overline{ER}$ goes LOW 80 CL2 pulses after RL/$\overline{EL}$</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>O</td><td>I</td><td>RL/$\overline{EL}$ goes LOW 80 CL2 pulses after RR/$\overline{ER}$</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>I</td><td>O</td><td>RR/$\overline{ER}$ goes LOW 20 CL2 pulses after RL/$\overline{EL}$</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>O</td><td>I</td><td>RL/$\overline{EL}$ goes LOW 20 CL2 pulses after RR/$\overline{ER}$</td></tr>
</table>
In the serial column mode, the device accepts one bit of display data at each CL2 pulse after RL/$\overline{EL}$ (or RR/$\overline{ER}$ respectively) goes LOW
When 80 bits of display data have been accepted, the device accepts no further display data and takes its output RR/$\overline{ER}$ (or RL/$\overline{EL}$ respectively) LOW, thereby enabling the next PCF2201 to accept display data
The sequence is reset when CL1 is HIGH and CL2 is LOW

In the parallel column mode, the device accepts one nibble of display data at each CL2 pulse after RL/$\overline{EL}$ (or RR/$\overline{ER}$ respectively) goes LOW
When 20 nibbles of display data have been accepted, the device accepts no further display data and takes its output RR/$\overline{ER}$ (or RL/$\overline{EL}$ respectively) LOW, thereby enabling the next PCF2201 to accept display data.
The sequence is reset when CL1 is HIGH and CL2 is LOW</td></tr>
<tr><td>LNG</td><td>I</td><td>Length control
<table>
<tr><th>COL/$\overline{ROW}$</th><th>LNG</th><th>SHL</th><th>description</th><th>valid Yi</th><th>undefined Yi</th></tr>
<tr><td>L
L</td><td>L
L</td><td>L
H</td><td>65-bit row mode
operation</td><td>Y1...Y65
Y17...Y80, F/Y81</td><td>Y66...Y80, F/Y81
Y1...Y16</td></tr>
<tr><td>L
L</td><td>H
H</td><td>L
H</td><td>81-bit row mode
operation</td><td>Y1...Y80, F/Y81
Y1...Y80, F/Y81</td><td>–
–</td></tr>
<tr><td>H
H</td><td>L
L</td><td>L
H</td><td>64-bit column
mode operation</td><td>Y1...Y64
Y17...Y80</td><td>Y65...Y80
Y1...Y16</td></tr>
<tr><td>H
H</td><td>H
H</td><td>L
H</td><td>80-bit column
mode operation</td><td>Y1...Y80
Y1...Y80</td><td>–
–</td></tr>
</table>
In 80/81-bit operation, the device behaves as previously described
In 64/65-bit operation, the device behaves as if all resources have been reduced to 64/65 instances; i.e. 16 outputs (determined by SHL) can no longer be accessed and should be left open circuit.</td></tr>
</table>

PINNING FUNCTIONS (continued)

<table>
<tr><th>mnemonic</th><th>I/O</th><th>function</th></tr>
<tr><td>F/Y81*</td><td>O</td><td>Frame output in column driver mode
It continuously delivers the select or non-select column driver LCD voltages depending on the state of the frame control
The frame output is used to blank the flat-panel display margin outside the actual LCD matrix
Liquid crystal driver output, number 81 in row driver mode</td></tr>
<tr><td>FON</td><td>I</td><td>Frame control
Defines the contents of the shift register cell corresponding to F/Y81 in column driver mode
Tie to V_{DD} or V_{SS} in row driver mode</td></tr>
<tr><td>M</td><td>I</td><td>Signal to convert LCD drive waveform into a.c.:
<table>
<tr><th>COL/$\overline{\text{ROW}}$</th><th>SR data</th><th>M</th><th>output level (Y_i or F/Y81)</th><th>note</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>V_2/V_3</td><td rowspan="4">row driver</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>V_4/V_5</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>V_{EE}</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>V_1</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>V_2/V_3</td><td rowspan="4">column driver</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>V_4/V_5</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>V_1</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>V_{EE}</td></tr>
</table></td></tr>
<tr><td>n.c.</td><td>—</td><td>not connected</td></tr>
</table>

* Patent application pending.

FUNCTIONAL DESCRIPTION

4-level driver

One of the liquid crystal driver levels (V_1, V_2/V_3, V_4/V_5 and V_{EE}) is output onto lines Y1 to Y80 and F/Y81 depending on the state of the relevant level shifter.

Level shifter

The level shifter converts logic level driver information into LCD level selection signals. The LCD level selection signals are dependent on the contents of the 81 stage bidirectional shift register and the state of signals M and COL/$\overline{\text{ROW}}$.

81 stage bidirectional shift register

In row driver mode the bidirectional shift register is used for the row line scan. In column driver mode the bidirectional shift register is used to hold column data until the next line is assembled in the data presentation latch.

Column mode data presentation latch

The column mode data presentation latch provides temporary storage during transfer of column data required for the next row.

Data scrambler

In serial column data transfer, the data scrambler converts 1-bit data to parallel 4-bit nibbles. Data is rearranged by the data scrambler according to the orientation (left or right) of the chip, as defined by pin SHL.

Selector

The selector generates latch clocks $\phi 1$ to $\phi 20$ for the presentation latch. Selection is determined by the state of the up/down counter and the carry logic.

Up/down counter, carry logic and control

Incoming column data storage locations are determined by the up/down counter making use of enable lines (RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$) and the length control select (LNG). The carry logic inhibits the data transfer clock (CL2) in inactive column drivers, thereby reducing power dissipation. When data transfer to one column driver is completed, the subsequent column driver is enabled by the carry logic. The control part co-ordinates the up/down counter and carry logic, depending upon the condition of the device (SHL, COL/$\overline{\text{ROW}}$, P/$\overline{\text{S}}$, LNG, RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	V_{SS} −0,3 to V_{SS} + 7	V
LCD supply voltage range	V_{EE}	V_{DD} −30 to V_{DD}	V
V_1, V_2/V_3 voltage range (note 1)	V_U	$\frac{V_{DD} + V_{EE}}{2} - 1$ to V_{DD}	V
V_4/V_5 voltage range (note 1)	V_L	V_{EE} to $\frac{V_{DD} + V_{EE}}{2} - 1$	V
Input voltage range (CL1, CL2, COL/$\overline{\text{ROW}}$, P/$\overline{\text{S}}$, SHL, D0, D1, D2, D3, RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$, LNG, FON, M)	V_I	V_{SS} −0,3 to V_{DD} + 0,3	V
Output voltage range (RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$)	V_O	V_{SS} −0,3 to V_{DD} + 0,3	V
Driver output voltage range (F/Y81, Y1 to Y80)	V_Y	V_{EE} −0,3 to V_{DD} + 0,3	V
DC input current	$\pm I_I$	max. 20	mA
DC output current	$\pm I_O$	max. 25	mA
V_{DD}, V_{SS}, V_1, V_2/V_3, V_4/V_5 or V_{EE} current	$\pm I_{SUP}$	max. 20	mA
Power dissipation per package	P_{tot}	max. 400	mW
Power dissipation per output	P_O	max. 100	mW
Storage temperature range	T_{stg}	−65 to + 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 4,5 to 5,5 V;

V_{EE} = 0 to −20 V; $V_{DD} \geqslant V_1 \geqslant V_2/V_3 \geqslant \frac{V_{DD} + V_{EE}}{2} - 1\ V \geqslant V_4/V_5 \geqslant V_{EE}$; f_M = 100 Hz

T_{amb} = −40 to + 85 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Positive supply voltage		V_{DD}	4,5	–	5,5	V
Negative LCD supply voltage		V_{EE}	$V_{DD}-25$	–	$V_{DD}-5$	V
Static supply current	$f_{CL1} = f_{CL2}$ = 0 Hz; COL/$\overline{\text{ROW}}$ = H; M = L; note 2	I_{DD1}	–	15	40	μA
Operating supply current	COL/$\overline{\text{ROW}}$ = H; f_{CL1} = 25 kHz; f_{CL2} = 4 MHz; note 2	I_{DD2}	–	0,4	1	mA
Operating supply current	COL/$\overline{\text{ROW}}$ = H; RL/$\overline{\text{EL}}$ = H (SHL = L) or RR/$\overline{\text{ER}}$ = H (SHL = H); f_{CL1} = 25 kHz; note 2	I_{DD3}	–	50	150	μA
Operating supply current	COL/$\overline{\text{ROW}}$ = L; f_{CL1} = 100 kHz; note 2	I_{DD4}	–	75	200	μA
Logic						
Input voltage LOW		V_{IL}	0	–	0,3 V_{DD}	V
HIGH		V_{IH}	0,7 V_{DD}	–	V_{DD}	
Output voltage LOW to RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$	I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH to RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$	I_O = 0 mA	V_{OH}	$V_{DD}-0,05$	–	–	V
Output current LOW to RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$	V_{OL} = 1 V	I_{OL}	1	–	–	mA

DC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output current HIGH RL/$\overline{EL}$ and RR/$\overline{ER}$	$V_{OH} = V_{DD}-1$ V	I_{OH}	–	–	1	mA
Leakage current at CL1, CL2, COL/$\overline{ROW}$, P/$\overline{S}$, SHL, D0 to D3, RL/$\overline{EL}$, RR/$\overline{ER}$, LNG, FON and M		$\pm I_{L1}$	–	–	1	μA
Input capacitance	note 3	C_I	–	–	7	pF
LCD outputs						
Leakage current at V_1, V_2/V_3, V_4/V_5		$\pm I_{L2}$	–	–	2	μA
Resistance ON between V_1, V_2/V_3, V_4/V_5, V_{EE} and Y1 to Y80, F/Y81	$I_O = 100$ μA; $V_{EE} = V_{DD}-25$ V note 4	R_{ON}	–	–	2	kΩ

AC CHARACTERISTICS (note 5)

$V_{SS} = 0$ V; $V_{DD} = 4{,}5$ to $5{,}5$ V;
$V_{EE} = 0$ to -20 V; $V_{DD} \geqslant V_1 \geqslant V_2/V_3 \geqslant \frac{V_{DD}+V_{EE}}{2} - 1\text{ V} \geqslant V_4/V_5 \geqslant V_{EE}$;
$f_M = 100$ Hz; see Figs 4 and 5; $T_{amb} = -40$ to $+85$ °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Column driver data transfer rate		f_{CL2}	–	–	4	MHz
CL2 HIGH time		t_{CL2H}	100	–	–	ns
CL2 LOW time		t_{CL2L}	100	–	–	ns
CL2 rise time		t_{CL2r}	–	–	25	ns
CL2 fall time		t_{CL2f}	–	–	25	ns
Row driver clock rate		f_{CL1}	–	–	100	kHz
CL1 HIGH time		t_{CL1H}	275	–	–	ns
CL1 LOW time		t_{CL1L}	5	–	–	μs
CL1 rise time		t_{CL1r}	–	–	50	ns
CL1 fall time		t_{CL1f}	–	–	50	ns

DEVELOPMENT DATA

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Column data set-up time	COL/$\overline{\text{ROW}}$ = H	t_{SUC}	50	–	–	ns
Column data hold time	COL/$\overline{\text{ROW}}$ = H	t_{HDC}	30	–	–	ns
Row data set-up time	COL/$\overline{\text{ROW}}$ = L	t_{SUR}	200	–	–	ns
Row data hold time	COL/$\overline{\text{ROW}}$ = L	t_{HDR}	0	–	–	ns
Enable HIGH to CL2 set-up time	COL/$\overline{\text{ROW}}$ = H	t_{ECH}	90	–	–	ns
Enable LOW to CL2 set-up time	COL/$\overline{\text{ROW}}$ = H	t_{ECL}	85	–	–	ns
Propagation delay to enable HIGH	COL/$\overline{\text{ROW}}$ = H	t_{PEH}	–	–	185	ns
Propagation delay to enable LOW	COL/$\overline{\text{ROW}}$ = H	t_{PEL}	–	–	140	ns
CL2 to CL1 time	COL/$\overline{\text{ROW}}$ = H	t_{CL21}	50	–	–	ns
CL1 to CL2 time	COL/$\overline{\text{ROW}}$ = H	t_{CL12}	50	–	–	ns
Overlap time of CL2 = LOW and CL1 = HIGH	COL/$\overline{\text{ROW}}$ = H	t_{ov}	275	–	–	ns
Propagation delay HIGH to RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$	COL/$\overline{\text{ROW}}$ = L	t_{PLH}	20	–	200	ns
Propagation delay LOW to RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$	COL/$\overline{\text{ROW}}$ = L	t_{PHL}	20	–	200	ns
Propagation delay to Y1 . . . Y80, F/Y81	$V_{EE} = V_{DD}$ −20 V	t_{PY}	–	–	3	μs

Notes to characteristics

1. Maintain $V_{DD} \geqslant V_1 \geqslant V_2/V_3 \geqslant \frac{V_{DD} + V_{EE}}{2} - 1\ V \geqslant V_4/V_5 \geqslant V_{EE}$.
2. Outputs open, inputs at V_{SS} or V_{DD}.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.
5. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

Fig. 3 Test loads.

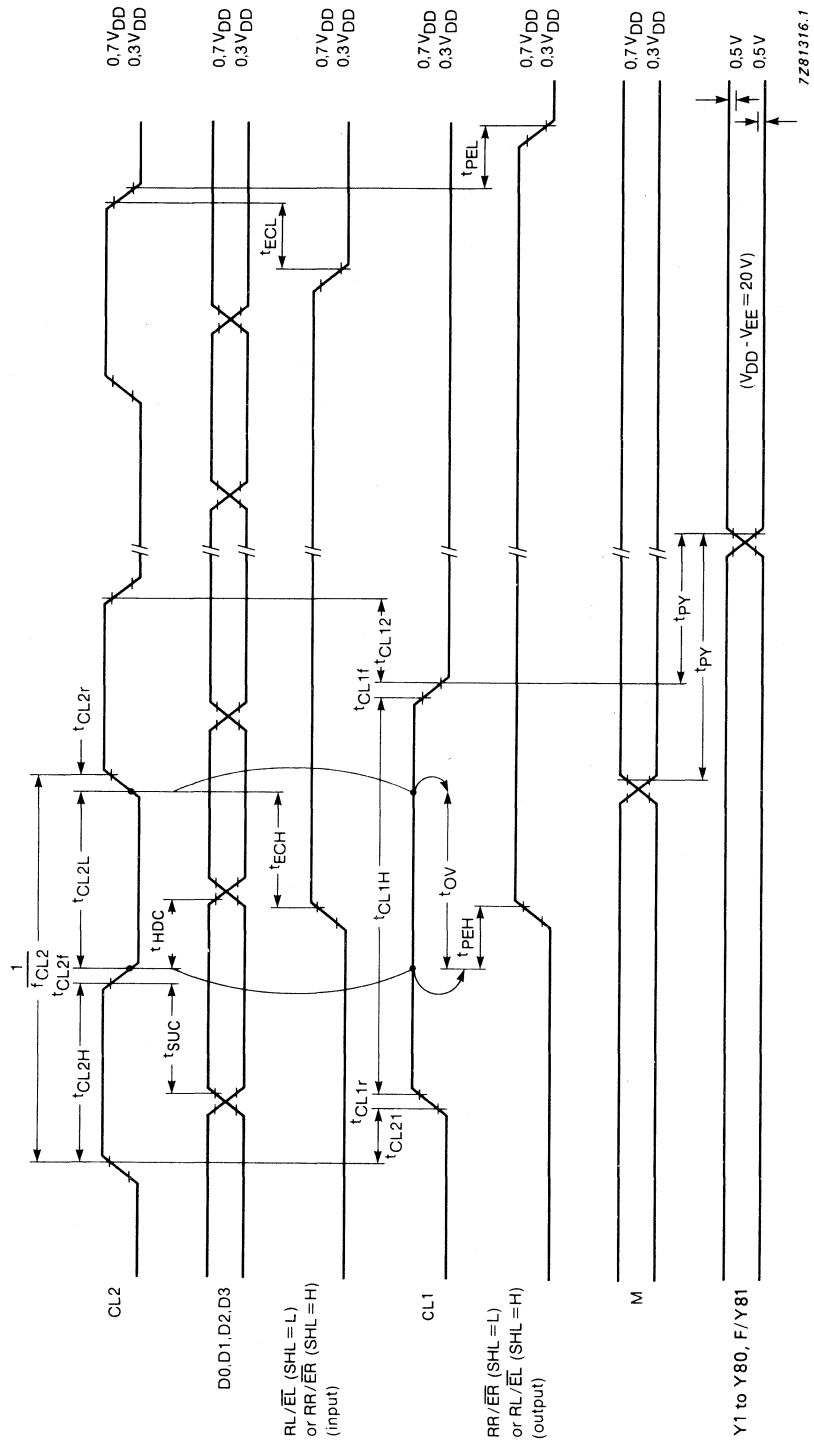


Fig. 4 Column driver timing waveforms.

DEVELOPMENT DATA

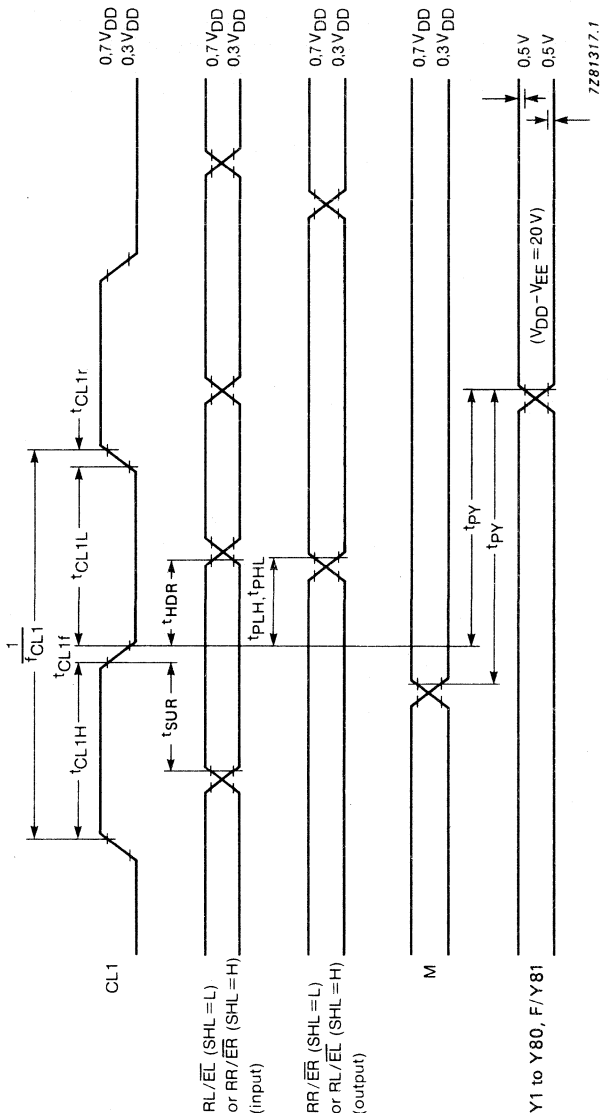


Fig. 5 Row driver timing waveforms.

APPLICATION INFORMATION

Generation of LCD bias levels

Optimum contrast for LCD flat-panels is achieved when the bias levels are selected using the formulae in Table 1. The multiplex rate is denoted by the variable n ($n \geqslant 9$). V_{th} is defined as the LCD threshold voltage, typically where the LCD exhibits approximately 10% contrast. The ratio of the 'ON' voltage to the 'OFF' voltage is discrimination (D) and is a measure of the flat-panel contrast at a given multiplex rate.

Table 1 LCD flat-panel bias levels for optimum contrast ($V_{op} = V1 - V_{EE}$)

$\frac{V_2}{V_{op}} = \frac{\sqrt{n}}{\sqrt{n}+1}$	$\frac{V_3}{V_{op}} = \frac{\sqrt{n}-1}{\sqrt{n}+1}$	$\frac{V_4}{V_{op}} = \frac{2}{\sqrt{n}+1}$	$\frac{V_5}{V_{op}} = \frac{1}{\sqrt{n}+1}$
$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}}$		$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n(\sqrt{n}+1)}}$	
$D = \frac{V_{on(rms)}}{V_{off(rms)}} = \frac{\sqrt{n-1}}{\sqrt{n}-1}$		$\frac{V_{op}}{V_{th}} = \frac{\sqrt{n}+1}{\sqrt{2(1-1/\sqrt{n}}}$	

The intermediate bias levels are generated by a resistive divider (see Fig. 6). Capacitors (C) are used to smooth out switching transients. Considerable power consumption may result by using this arrangement when driving a large LCD flat-panel, because of the low impedance of the resistive divider.

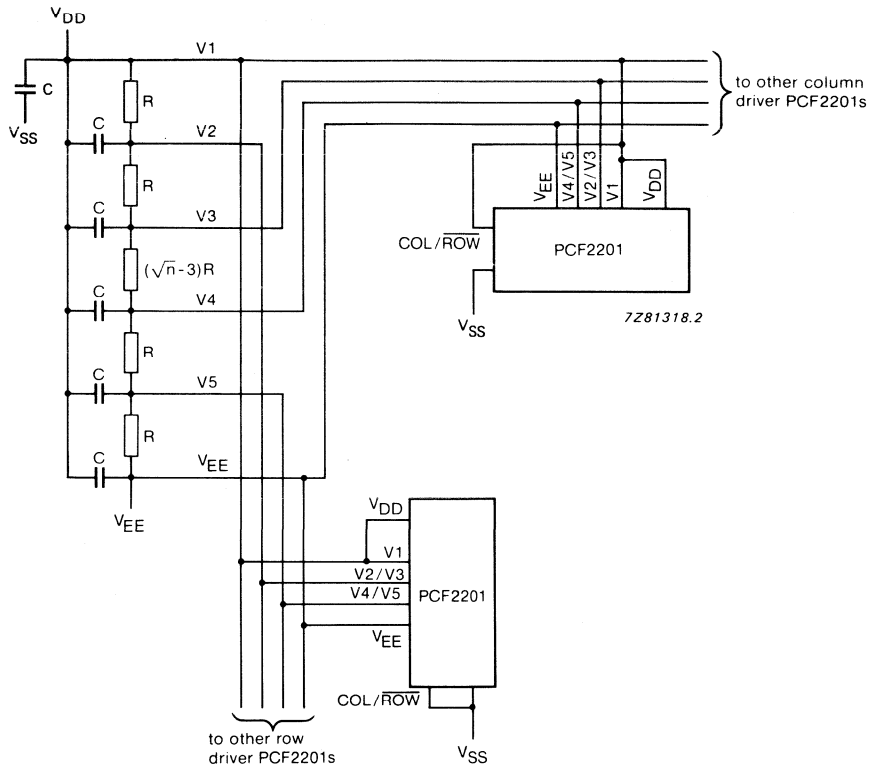


Fig. 6 Unbuffered LCD biasing level generation.

DEVELOPMENT DATA

A better solution for LCD flat-panel biasing is presented in Fig. 7. The operational amplifiers provide low impedance biasing with a low power consumption. The fairly high impedance which can be implemented at the resistive divider, helps maintain low power consumption. One diode voltage drop seperates V1 from V_{DD} to compensate for the limited common mode voltage range (V+ −1,5 V) when the operational amplifiers are powered between V_{DD} and V_{EE}.

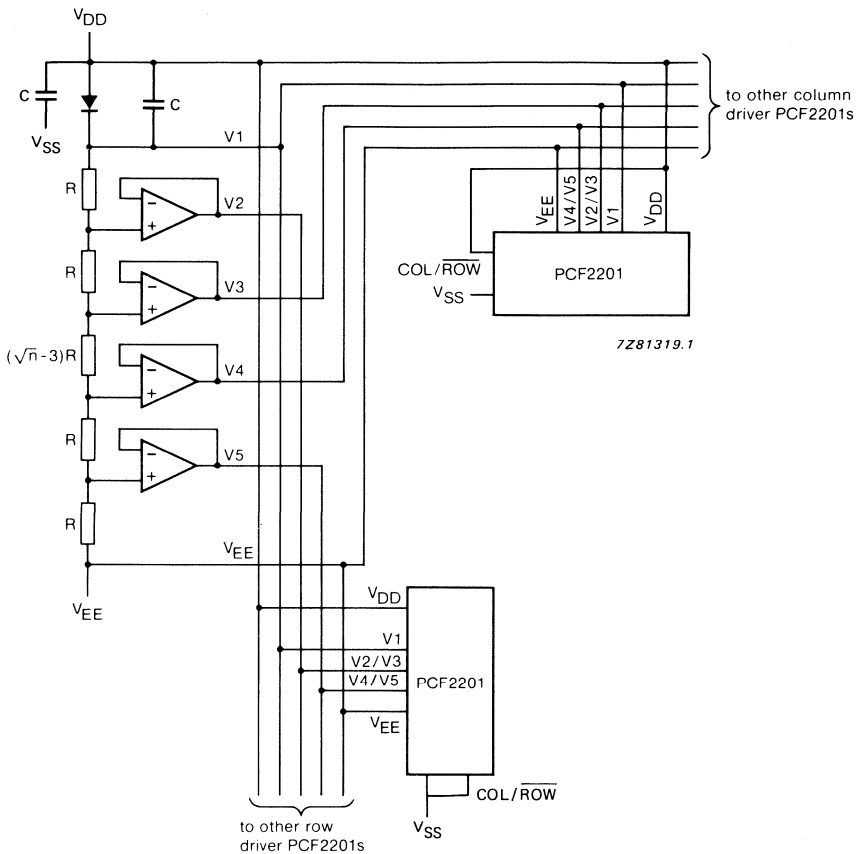


Fig. 7 Buffered LCD bias level generation.

Typical LCD flat-panel application

Alphanumeric/graphic computer terminals with LCD flat-panel screens using 200 x 640 dots are very popular. The format of 200 x 640 is compatible with the standard 25 lines by 80 characters at 8 x 8 dot character fonts. Fig. 8 gives a possible circuit using 19 PCF2201's, with upper and lower half screens used for good contrast. The use of half screens reduces the multiplex rate to 1:100 (Fig. 9 gives the timing information).

DEVELOPMENT DATA

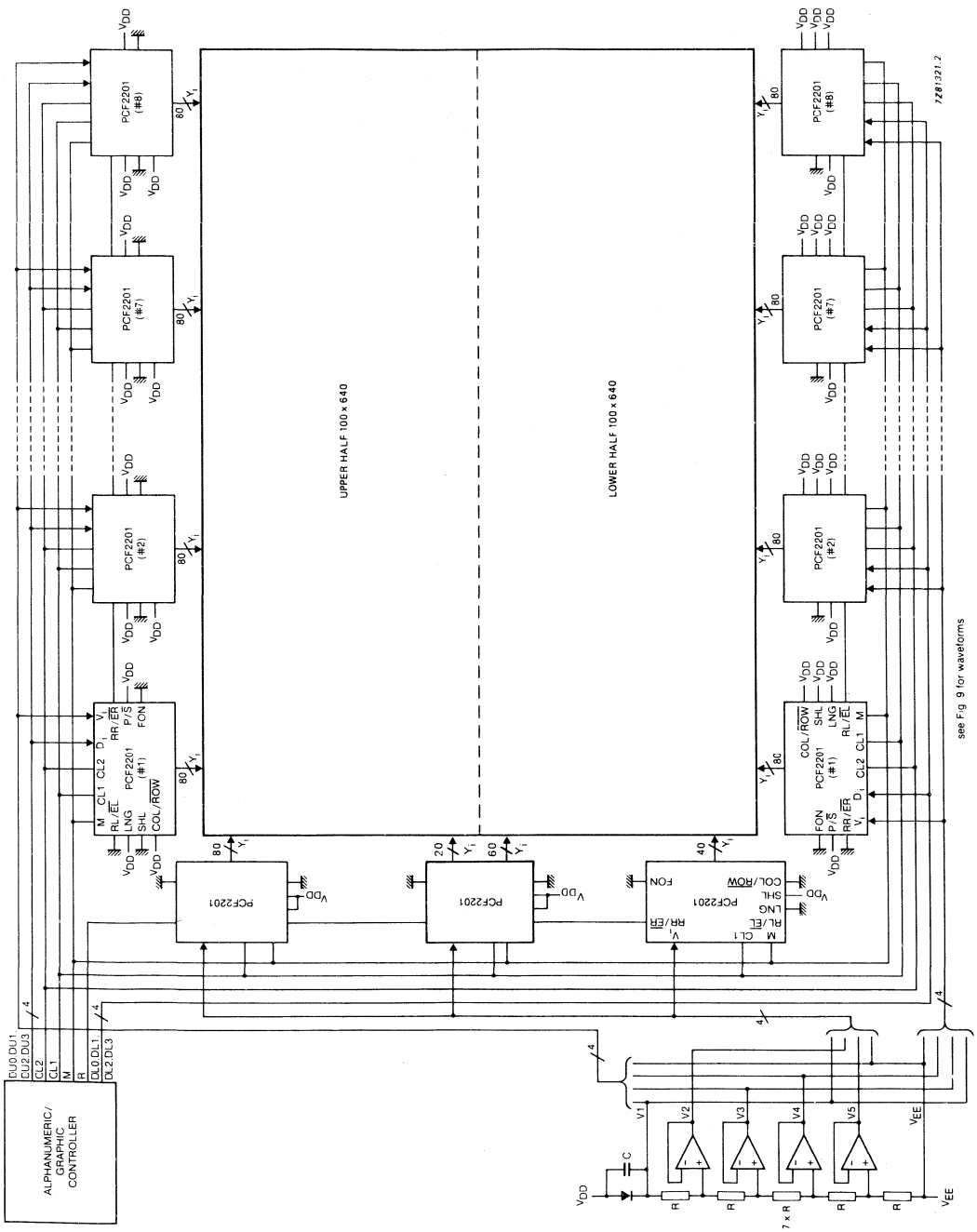


Fig. 8 LCD flat-panel with 1:100 multiplex rate in upper and lower half screens.

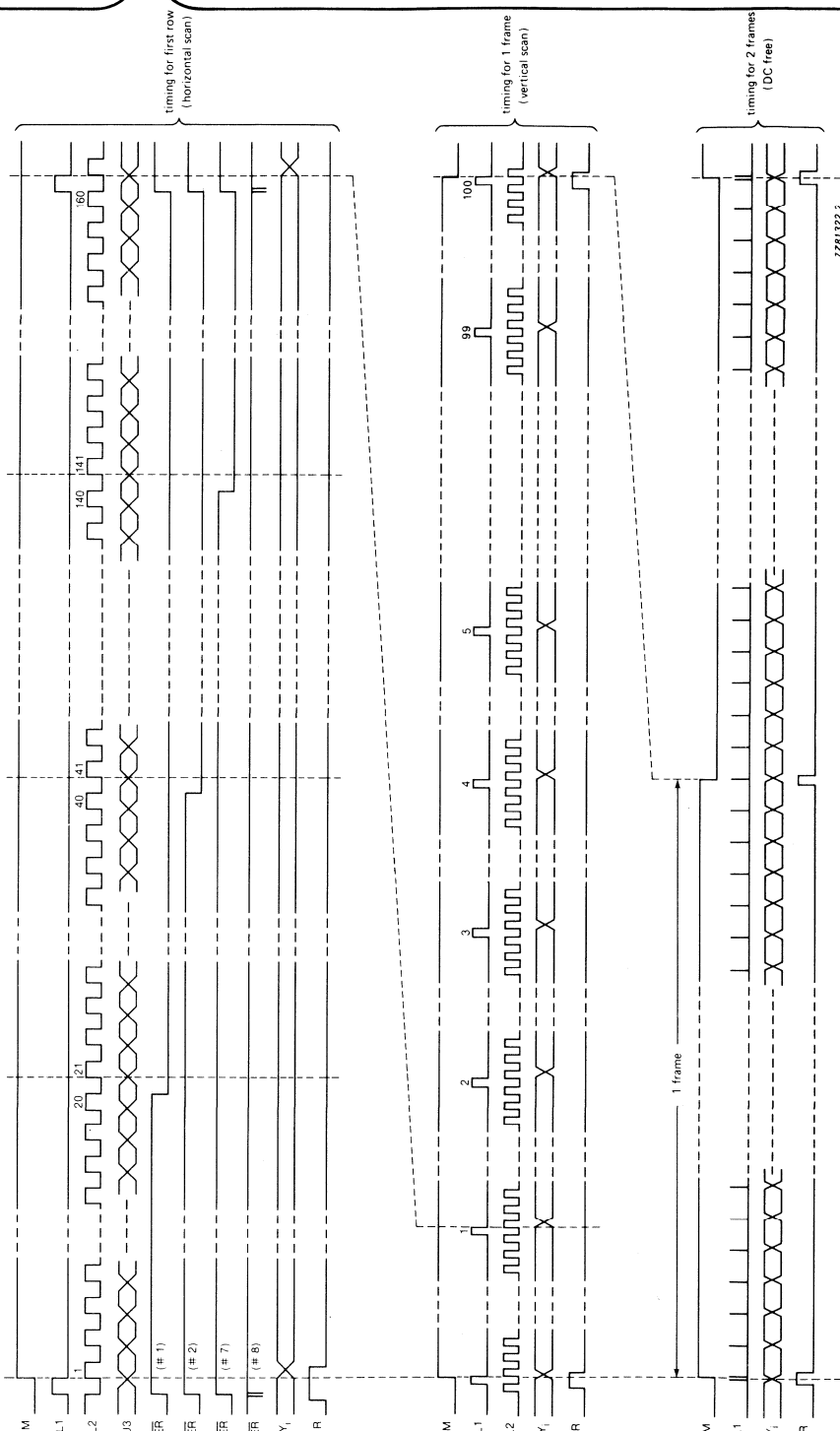
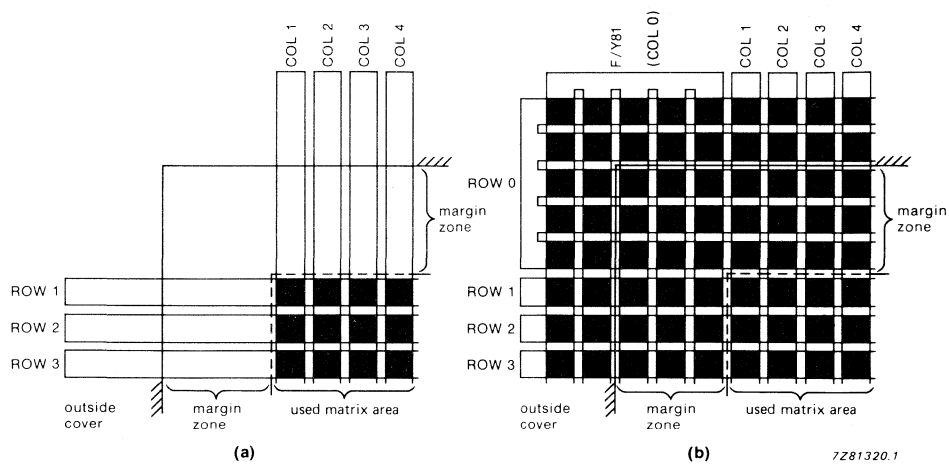


Fig. 9 Timing for the upper half screen of the LCD flat-panel (Fig. 8). For the lower half screen, replace RR/$\overline{ER}$, DU0, DU1, DU2 and DU3 with RL/$\overline{EL}$, DL0, DL1, DL2, DL3.

Margin control

The used area of the flat-panel matrix is normally smaller than the LCD glass surface. Connection lines outside of the used area of the matrix carry row or column LCD signals (see Fig. 10A). This 'null' state differs slightly in colour from the 'OFF' state pixel for twisted nematic LCD. The structural change in the margin zone is noticeable.

When a high contrast Philips LCD flat-panel of the supertwisted birefringence effect (SBE) type is employed, the situation becomes critital. The colour of the 'OFF' state appears blue and the colour of the 'ON' state appears grey or white. Therefore inverted information is sent to the display, generating dark (blue) characters on a light (grey) background. The margin zone is treated as an extension of the used matrix area (see Fig. 10B), to avoid the margin zone appearing as a dark blue frame. This is extended out to a region where the LCD glass can be covered up. The additional row requires an increase in the multiplex rate from n to n + 1, the additional column is realized by the frame output of the furthest left and right column drivers of the flat-panel. This removes the requirement for additional column drivers packages to provide margin control.



(A) without margin control

(B) with margin control

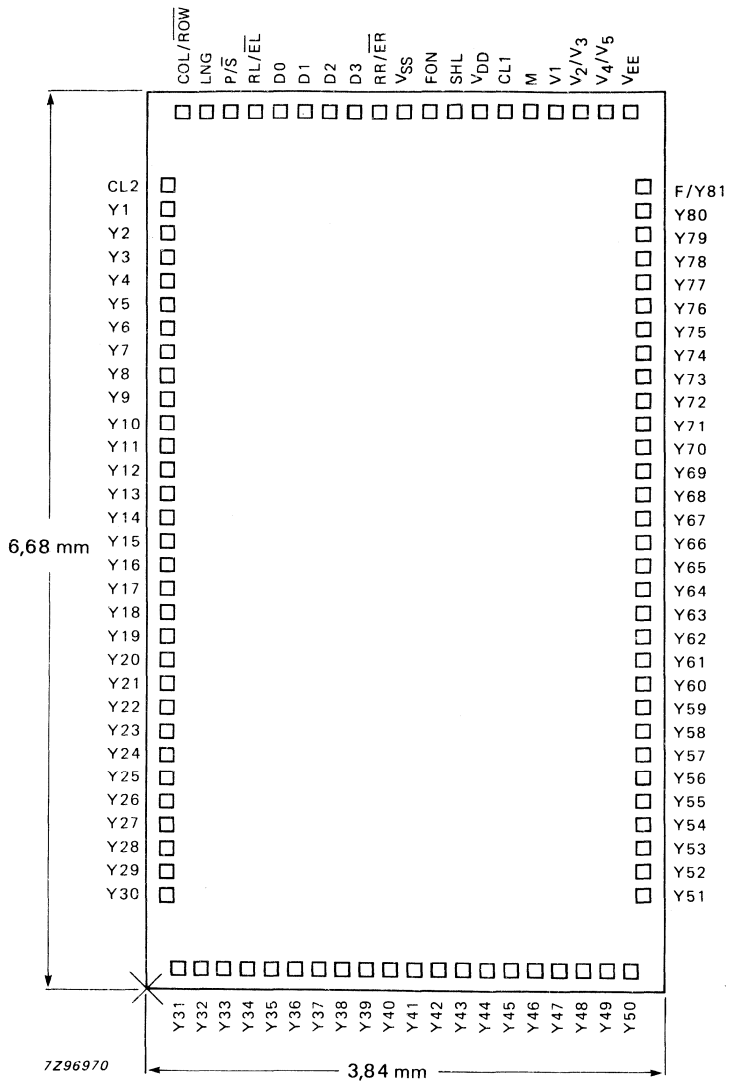
Fig. 10 Upper left corner of the LCD flat-panel.

Single plane wiring

The pinning of the PCF2201 tape-automated bonding package has been selected for ease of wiring. One side of this package contains no pins. The adjacent logic level lines are arranged so that they can be bussed in a single plane on the printed circuit board, which allows single sided substrates to be used.

For ease of wiring layout it is suggested to use the bus-level numbers (see Fig. 2) since most supply lines can be run through at the same level. On the actual package there are 120 pins, of which 19 pins are not internally connected. These extra pins are due to single plane wiring gaps and enhance stability in surface mounting.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 25,65 mm^2

Bonding pad dimensions: 104 μm x 104 μm

Fig. 11 Bonding pad locations.

Table 2 Bonding pad centre locations (dimensions in μm)

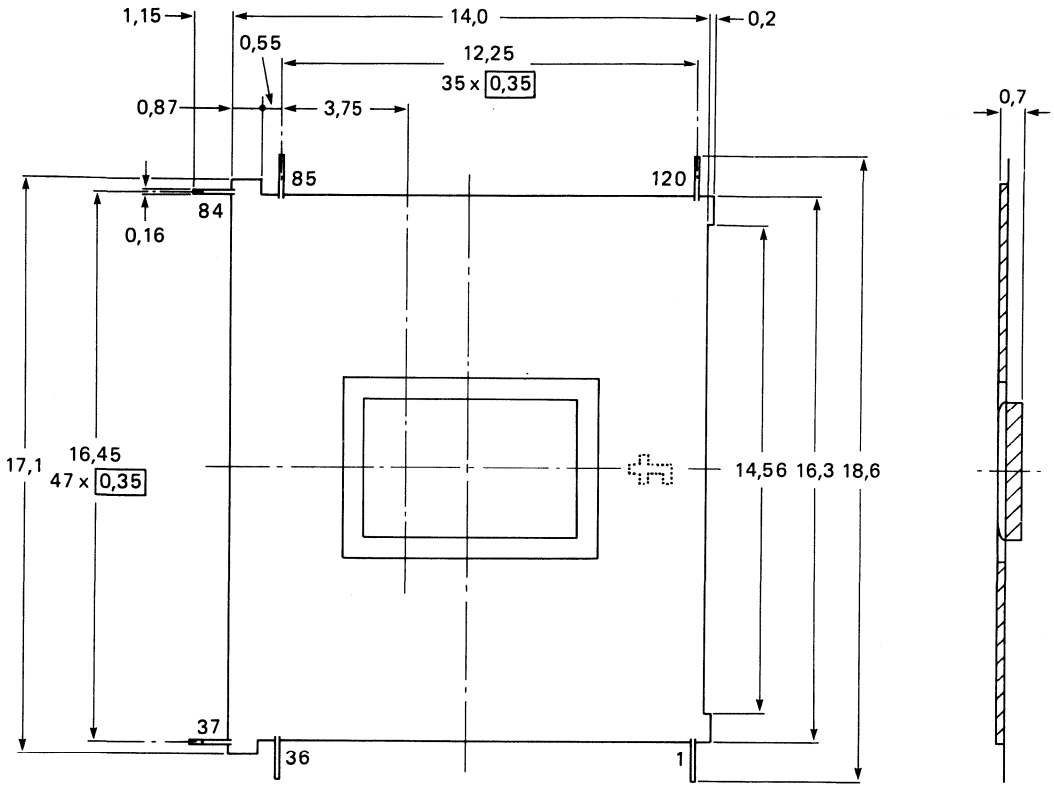
All x/y co-ordinates are referenced to the bottom left corner, see Fig. 11.

pad	X	Y	pad	X	Y
D3	1556	6526	Y43	2364	154
D2	1372	6526	Y44	2540	154
D1	1188	6526	Y45	2716	154
D0	1004	6526	Y46	2892	154
RL/$\overline{EL}$	820	6526	Y47	3068	154
P/$\overline{S}$	636	6526	Y48	3244	154
LNG	452	6526	Y49	3420	154
COL/$\overline{ROW}$	268	6526	Y50	3596	154
CL2	156	5982	Y51	3684	702
Y1	156	5806	Y52	3684	878
Y2	156	5630	Y53	3684	1054
Y3	156	5454	Y54	3684	1230
Y4	156	5278	Y55	3684	1406
Y5	156	5102	Y56	3684	1582
Y6	156	4926	Y57	3684	1758
Y7	156	4750	Y58	3684	1934
Y8	156	4574	Y59	3684	2110
Y9	156	4398	Y60	3684	2286
Y10	156	4222	Y61	3684	2462
Y11	156	4046	Y62	3684	2638
Y12	156	3870	Y63	3684	2814
Y13	156	3694	Y64	3684	2990
Y14	156	3518	Y65	3684	3166
Y15	156	3342	Y66	3684	3342
Y16	156	3166	Y67	3684	3518
Y17	156	2990	Y68	3684	3694
Y18	156	2814	Y69	3684	3870
Y19	156	2638	Y70	3684	4046
Y20	156	2462	Y71	3684	4222
Y21	156	2286	Y72	3684	4398
Y22	156	2110	Y73	3684	4574
Y23	156	1934	Y74	3684	4750
Y24	156	1758	Y75	3684	4926
Y25	156	1582	Y76	3684	5102
Y26	156	1406	Y77	3684	5278
Y27	156	1230	Y78	3684	5454
Y28	156	1054	Y79	3684	5630
Y29	156	878	Y80	3684	5806
Y30	156	702	F/Y81	3684	5982
Y31	252	154	V_{EE}	3580	6526
Y32	428	154	V_4/V_5	3396	6526
Y33	604	154	V_2/V_3	3212	6526
Y34	780	154	V1	3028	6526
Y35	956	154	M	2844	6526
Y36	1132	154	CL1	2660	6526
Y37	1308	154	V_{DD}	2476	6526
Y38	1484	154	SHL	2292	6526
Y39	1660	154	FON	2108	6526
Y40	1836	154	V_{SS}	1924	6526
Y41	2012	154	RR/$\overline{ER}$	1740	6526
Y42	2188	154			

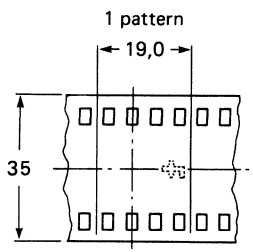
DEVELOPMENT DATA

120-LEAD TAPE-AUTOMATED BONDING PACKAGE

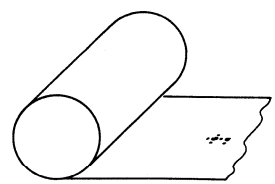
Dimensions in mm



120 lead tab module



tape



orientation on reel

7Z95862.1

LCD ROW/COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8, 1:16, 1:24 or 1:32. The device has 40 outputs, of which 24 are programmable, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (40,960 dots possible)
- 40 driver outputs, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns
- Selectable multiplex rates; 1:8, 1:16, 1:24 or 1:32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8578T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8578V: 64-lead tape-automated-bonding module (SOT267A).
PCF8578U: chip with bumps on-tape.

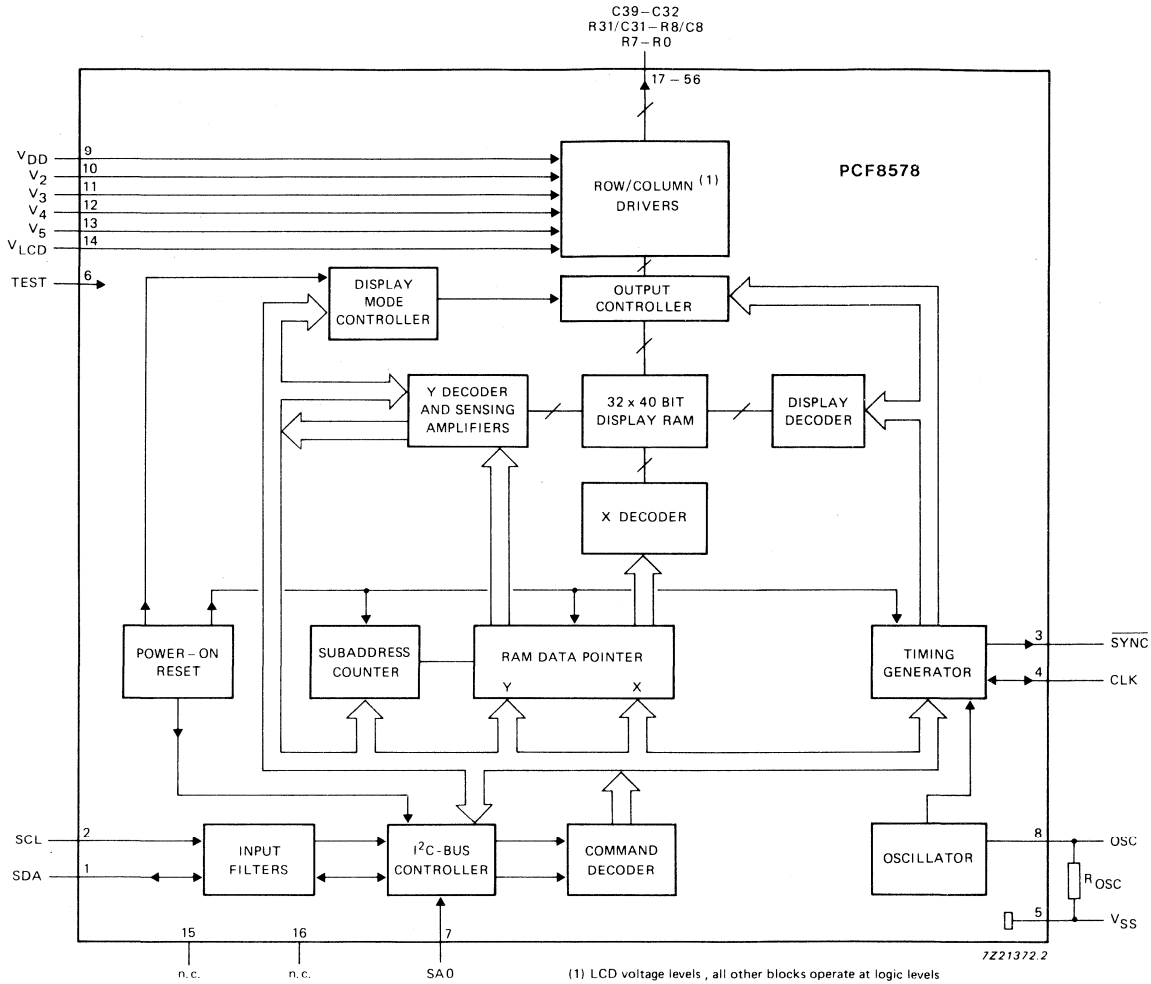


Fig.1 Block diagram.

DEVELOPMENT DATA

PINNING

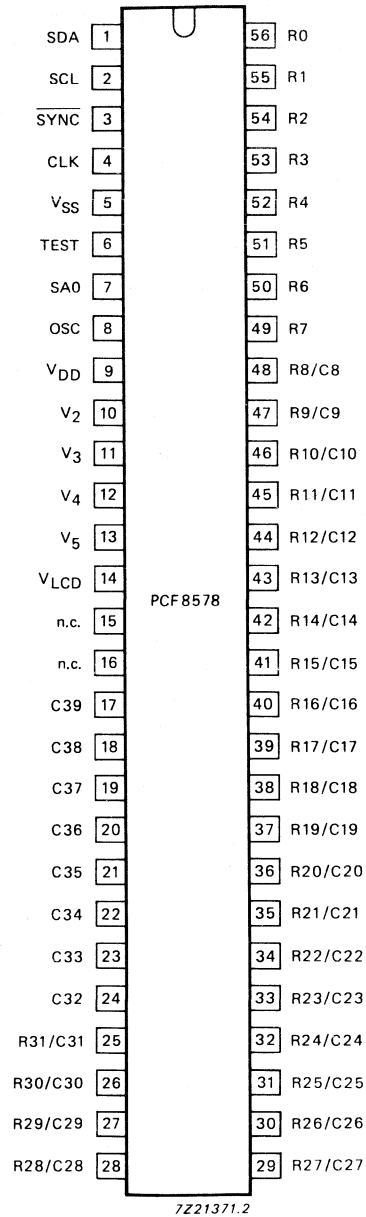
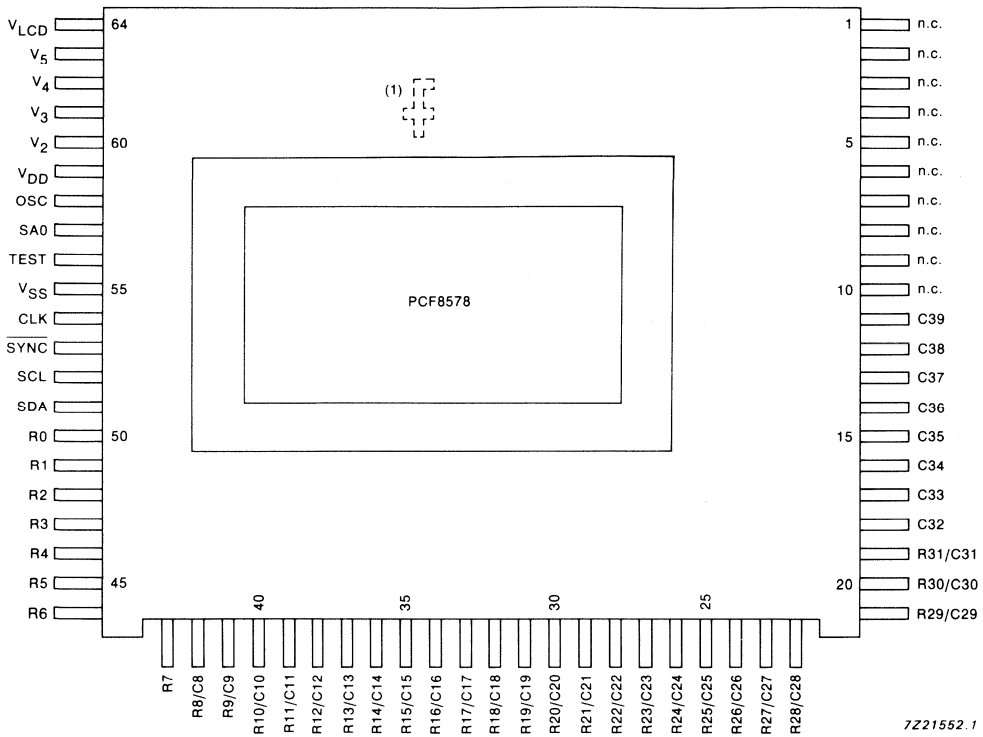


Fig.2 (a) Pinning diagram: VSO56; SOT190.

PINNING (continued)



(1) Orientation mark.

Fig.2 (b) Pinning diagram; SO121.

mnemonic	pin no.		description
	SOT190	SO121	
SDA	1	51	I^2C-bus serial data line
SCL	2	52	I^2C-bus serial clock line
$\overline{SYNC}$	3	53	cascade synchronization output
CLK	4	54	external clock input/output
V_{SS}	5	55	ground (logic)
TEST	6	56	test pin (connect to V_{SS})
SA0	7	57	I^2C-bus slave address input (bit 0)
OSC	8	58	oscillator input
V_{DD}	9	59	positive supply voltage
V_2 to V_5	10 - 13	60 - 63	LCD bias voltage inputs
V_{LCD}	14	64	LCD supply voltage
n.c.	15 - 16	1 - 10	not connected
C39 to C32	17 - 24	11 - 18	LCD column driver outputs
R31/C31 to R8/C8	25 - 48	19 - 42	LCD row/column driver outputs
R7 to R0	49 - 56	43 - 50	LCD row driver outputs

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The PCF8578 row/column driver is designed for use in one of three ways:

- Stand-alone row/column driver for small displays (mixed mode)
- Row/column driver with cascaded PCF8579s (mixed mode)
- Row driver with cascaded PCF8579s (row mode)

Mixed mode

In mixed mode, the device functions as both a row and column driver. It can be used in small stand-alone applications, or for larger displays with up to 15 PCF8579s (31 PCF8579s when two slave addresses are used). See table 1 for common display configurations.

Row mode

In row mode, the device functions as a row driver with up to 32 row outputs and provides the clock and synchronization signals for the PCF8579. Up to 16 PCF8579s can normally be cascaded (32 when two slave addresses are used).

Table 1 Possible display configurations

application	multiplex rate	mixed mode		row mode		typical applications
		rows	columns	rows	columns	
stand-alone	1:8	8	32	–	–	small digital or alphanumeric displays
	1:16	16	24	–	–	
	1:24	24	16	–	–	
	1:32	32	8	–	–	
with PCF8579	1:8	8	632	8 x 4	640	alphanumeric displays and dot matrix graphic displays
	1:16	16	624	16 x 2	640	
	1:24	24	616	24	640	
	1:32	32	608	32	640	
		using 15 PCF8579s		using 16 PCF8579s		

Timing signals are derived from the on-chip oscillator, whose frequency is determined by the value of the resistor connected between OSC and V_{SS}.

Commands sent on the I^2C-bus from the host microprocessor set the mode (row or mixed), configuration (multiplex rate and number of rows and columns) and control the operation of the device. The device may have one of two slave addresses. The only difference between these slave addresses is the least significant bit, which is set by the logic level applied to SA0. The PCF8578 and PCF8579 also have subaddresses. The subaddress of the PCF8578 is only defined in mixed mode and is fixed at 0. The RAM may only be accessed in mixed mode and data is loaded as described for the PCF8579.

Bias levels may be generated by an external potential divider with appropriate decoupling capacitors. For large displays, bias sources with high drive capability should be used. A typical mixed mode system operating with up to 15 PCF8579s is shown in Fig.3 (a stand-alone system would be identical but without the PCF8579s).

DEVELOPMENT DATA

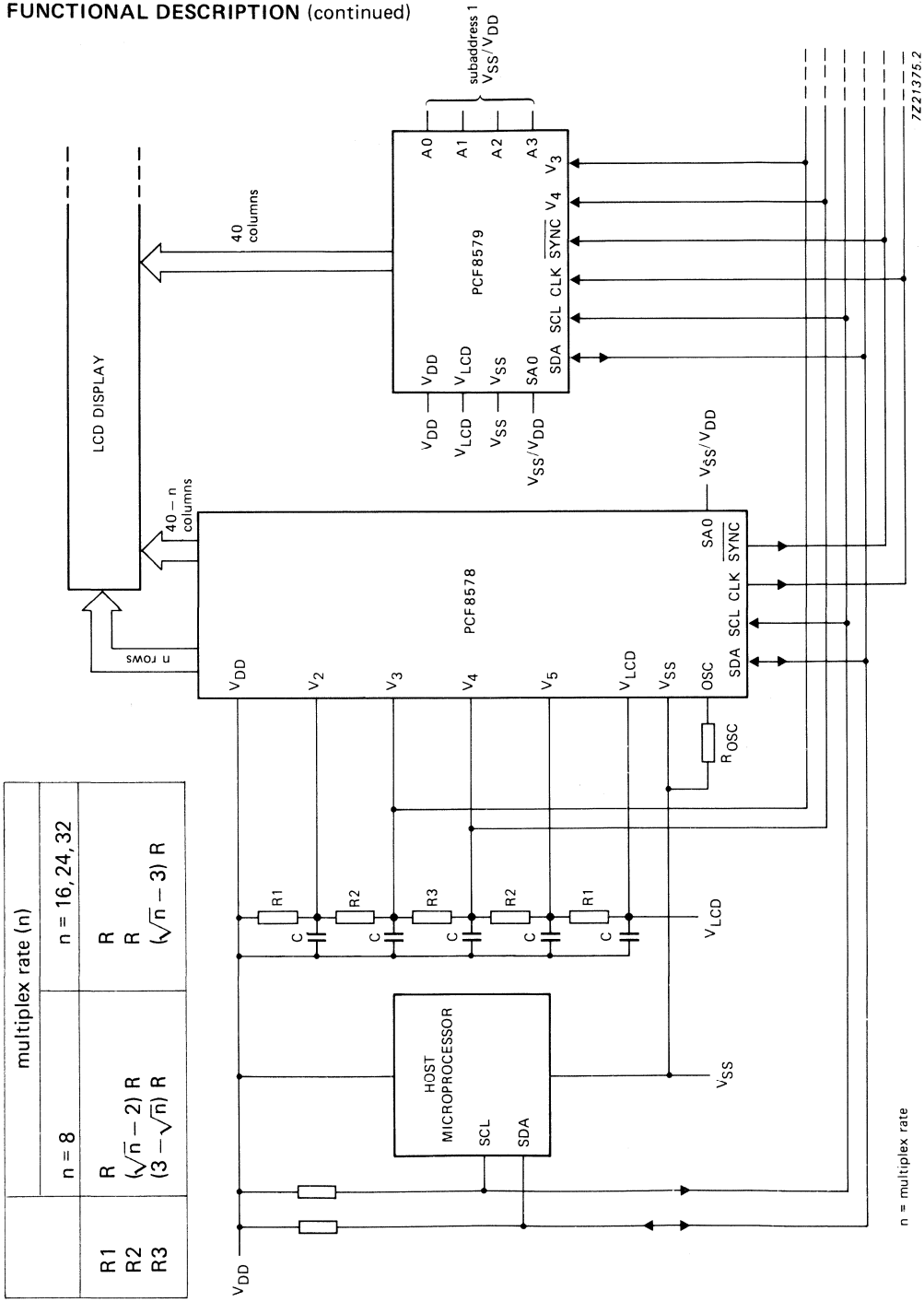
Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the LCD threshold voltage (V_{th}). V_{th} is typically defined as the RMS voltage at which the LCD exhibits 10% contrast. Table 2 shows the optimum voltage bias levels for the PCF8578 as functions of V_{op} ($V_{op} = V_{DD} - V_{LCD}$), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{op} is obtained by equating $V_{off(rms)}$ with V_{th}.

Table 2 Optimum LCD bias voltages

parameter	multiplex rate			
	1:8	1:16	1:24	1:32
$\frac{V_2}{V_{op}}$	0.739	0.800	0.830	0.850
$\frac{V_3}{V_{op}}$	0.522	0.600	0.661	0.700
$\frac{V_4}{V_{op}}$	0.478	0.400	0.339	0.300
$\frac{V_5}{V_{op}}$	0.261	0.200	0.170	0.150
$\frac{V_{off(rms)}}{V_{op}}$	0.297	0.245	0.214	0.193
$\frac{V_{on(rms)}}{V_{op}}$	0.430	0.316	0.263	0.230
$D = \frac{V_{on(rms)}}{V_{off(rms)}}$	1.447	1.291	1.230	1.196
$\frac{V_{op}}{V_{th}}$	3.37	4.08	4.68	5.19

FUNCTIONAL DESCRIPTION (continued)



	multiplex rate (n)	
	n = 8	n = 16, 24, 32
R1	R	R
R2	$(\sqrt{n} - 2)$ R	R
R3	$(3 - \sqrt{n})$ R	$(\sqrt{n} - 3)$ R

Fig.3 Typical mixed mode configuration.

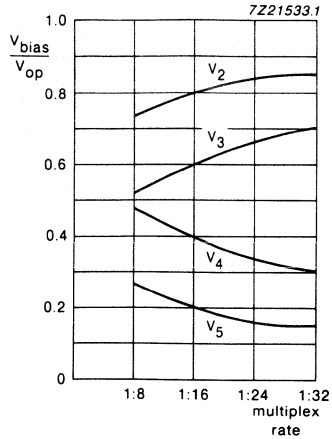


Fig.4 LCD bias voltages as a function of the multiplex rate.

Power-on reset

At power-on the PCF8578 resets to a defined starting condition as follows:

1. Display blank
2. 1:32 multiplex rate, row mode
3. Start bank 0 selected
4. Data pointer is set to X, Y address 0, 0
5. Character mode
6. Subaddress counter is set to 0
7. I^2C-bus interface is initialized.

Data transfers on the I^2C-bus should be avoided for 1 ms following power-on, to allow completion of the reset action.

FUNCTIONAL DESCRIPTION (continued)

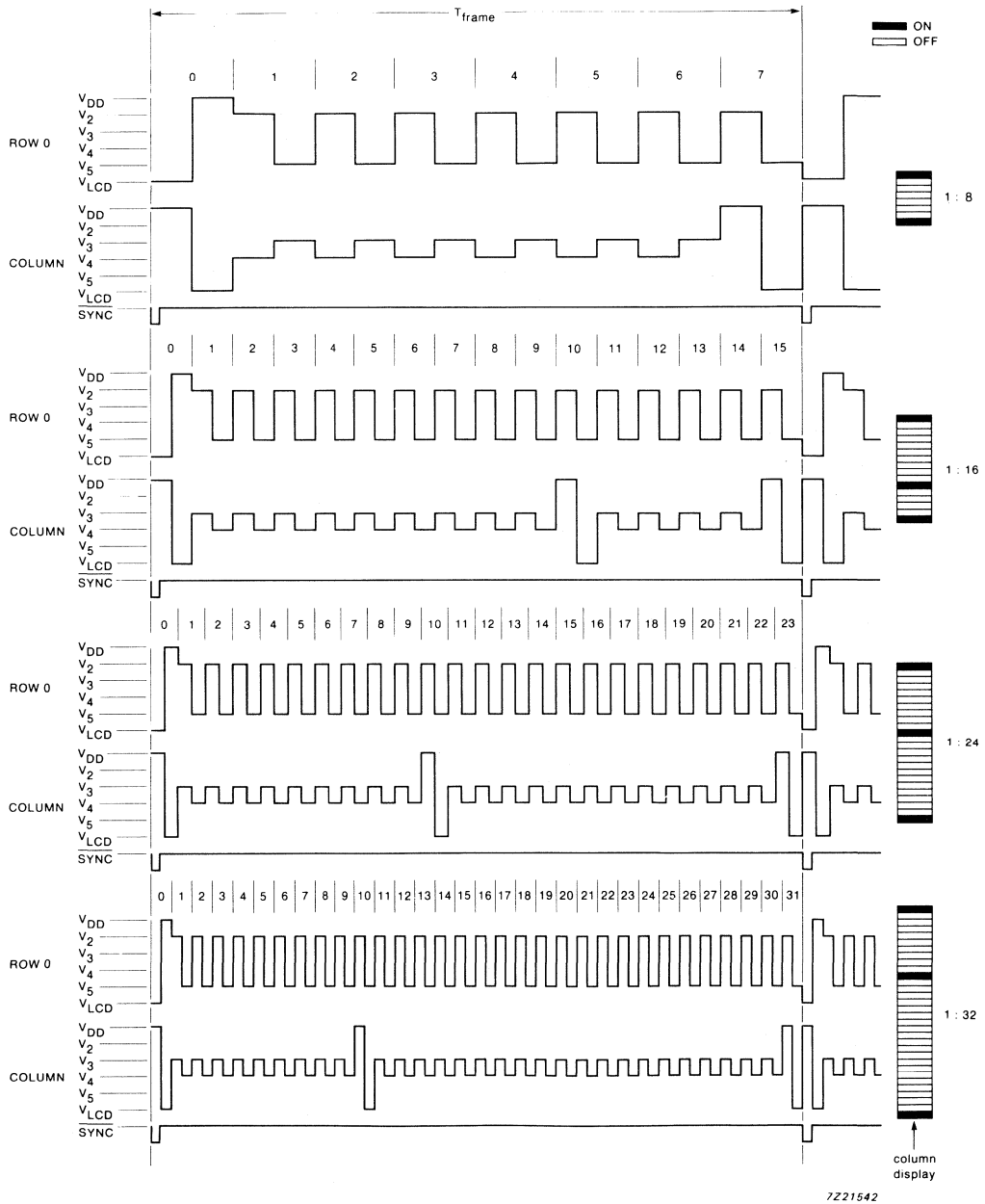
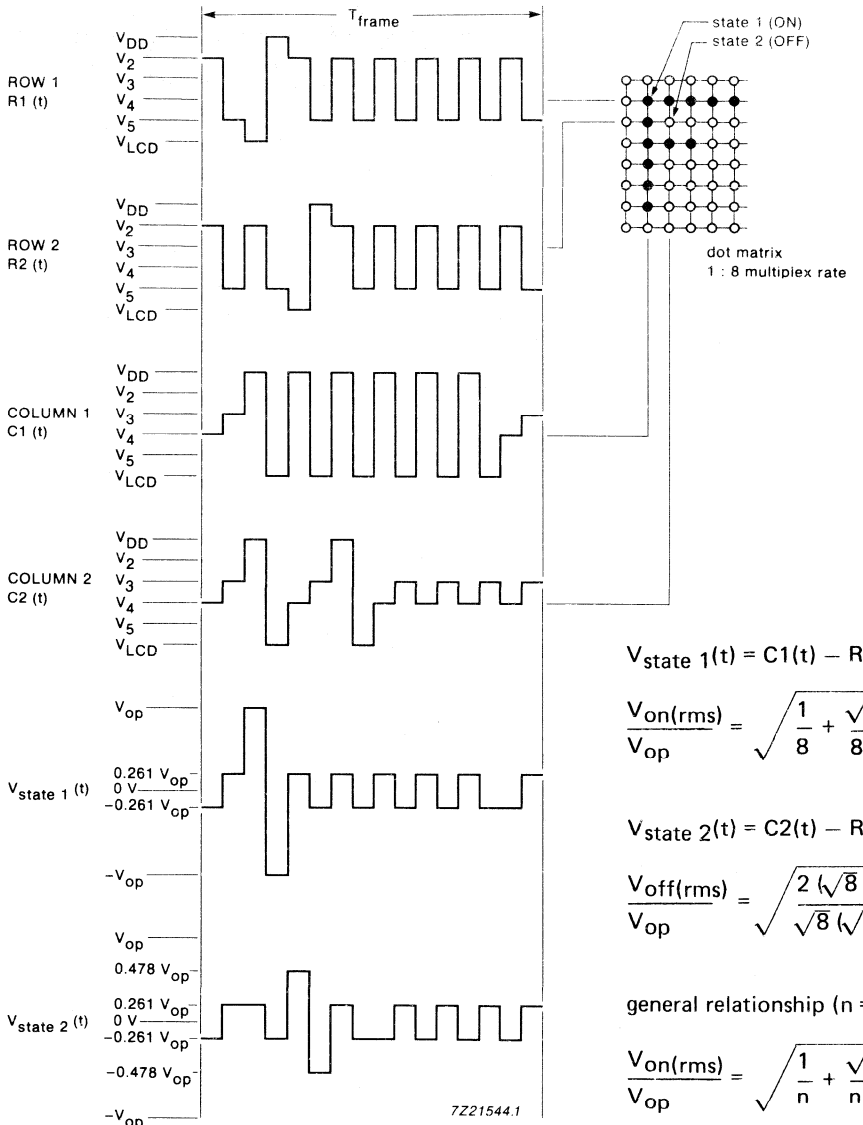


Fig.5 LCD row/column waveforms.

DEVELOPMENT DATA



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{8} + \frac{\sqrt{8}-1}{8(\sqrt{8}+1)}} = 0.430$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{8}-1)}{\sqrt{8}(\sqrt{8}+1)^2}} = 0.297$$

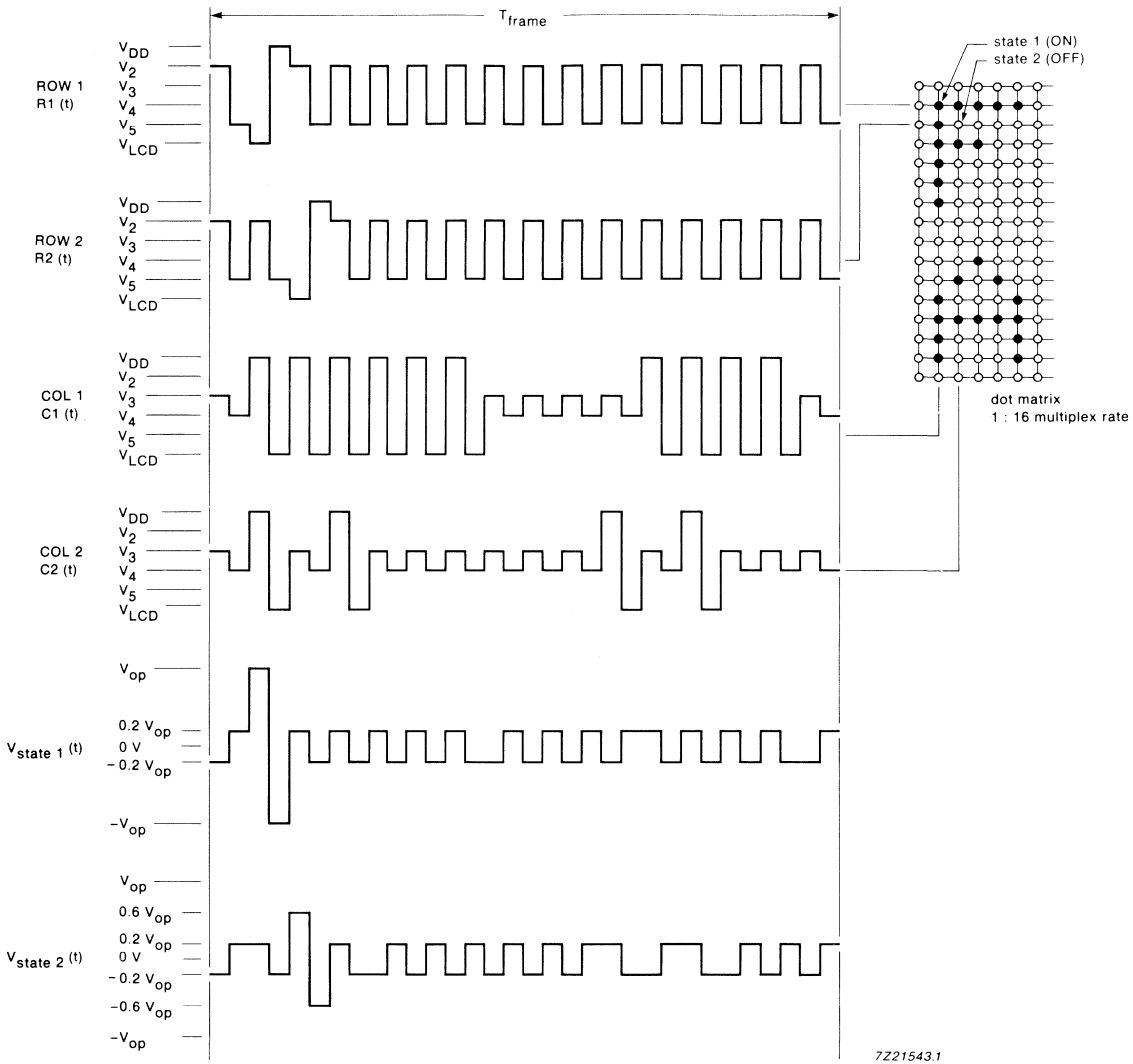
general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n(\sqrt{n}+1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}}$$

Fig.6 LCD drive mode waveforms for 1:8 multiplex rate.

FUNCTIONAL DESCRIPTION (continued)



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{16} + \frac{\sqrt{16} - 1}{16\,(\sqrt{16} + 1)}} = 0.316$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{16} - 1)}{\sqrt{16}\,(\sqrt{16} + 1)^2}} = 0.245$$

general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n} - 1}{n\,(\sqrt{n} + 1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{n} - 1)}{\sqrt{n}\,(\sqrt{n} + 1)^2}}$$

Fig.7 LCD drive mode waveforms for 1:16 multiplex rate.

Internal clock

The clock signal for the system may be generated by the internal oscillator and prescaler. The frequency is determined by the value of the resistor R_{OSC}, see Fig.8. For normal use a value of 330 kΩ is recommended. The clock signal, for cascaded PCF8579s, is output at CLK and has a frequency one-sixth (multiplex rate 1:8, 1:16 and 1:32) or one-eighth (multiplex rate 1:24) of the oscillator frequency.

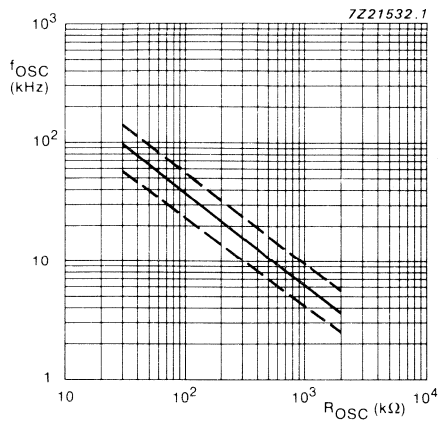


Fig.8 Oscillator frequency as a function of R_{OSC}.

Note

To avoid capacitive coupling, which could adversely affect oscillator stability, R_{OSC} should be placed as closely as possible to the OSC pin. If this proves to be a problem, a filtering capacitor may be connected in parallel to R_{OSC}.

External clock

If an external clock is used, OSC must be connected to V_{DD} and the external clock signal to CLK. Table 3 summarizes the nominal CLK and $\overline{SYNC}$ frequencies.

Table 3 Signal frequencies required for nominal 64 Hz frame frequency

oscillator frequency (R_{OSC} = 330 kΩ) f_{OSC} (Hz)	frame frequency $f_{\overline{SYNC}}$ (Hz)	multiplex rate n	division ratio	clock frequency f_{CLK} (Hz)
12288	64	1:8; 1:16; 1:32	6	2048
12288	64	1:24	8	1536

A clock signal must always be present, otherwise the LCD may be frozen in a DC state.

FUNCTIONAL DESCRIPTION (continued)

Timing generator

The timing generator of the PCF8578 organizes the internal data flow of the device and generates the LCD frame synchronization pulse $\overline{SYNC}$, whose period is an integer multiple of the clock period. In cascaded applications, this signal maintains the correct timing relationship between the PCF8578 and PCF8579s in the system.

Row/column drivers

Outputs R0 to R7 and C32 to C39 are fixed as row and column drivers respectively. The remaining 24 outputs R8/C8 to R31/C31 are programmable and may be configured (in blocks of 8) to be either row or column drivers. The row select signal is produced sequentially at each output from R0 up to the number defined by the multiplex rate (see Table 1). In mixed mode the remaining outputs are configured as columns. In row mode all programmable outputs (R8/C8 to R31/C31) are defined as row drivers and the outputs C32 to C39 should be left open-circuit. Using a 1:16 multiplex rate, two sets of row outputs are driven, thus facilitating split-screen configurations; i.e. a row select pulse appears simultaneously at R0 and R16/C16, R1 and R17/C17 etc. Similarly, using a multiplex rate of 1:8, four sets of row outputs are driven simultaneously. Driver outputs must be connected directly to the LCD. Unused outputs should be left open-circuit.

Display mode controller

The configuration of the outputs (row or column) and the selection of the appropriate driver waveforms are controlled by the display mode controller.

Display RAM

The PCF8578 contains a 32 x 40 bit static RAM which stores the display data. The RAM is divided into 4 banks of 40 bytes (4 x 8 x 40 bits). During RAM access, data is transferred to/from the RAM via the I^2C-bus. The first eight columns of data (0 to 7) cannot be displayed but are available for general data storage and provide compatibility with the PCF8579.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows an individual data byte or a series of data bytes to be written into, or read from, the display RAM, controlled by commands sent on the I^2C-bus.

Subaddress counter

The storage and retrieval of display data is dependent on the content of the subaddress counter. Storage takes place only when the contents of the subaddress counter agree with the hardware subaddress. The hardware subaddress of the PCF8578, valid in mixed mode only, is fixed at 0000.

I^2C-bus controller

The I^2C-bus controller detects the I^2C-bus protocol, slave address, commands and display data bytes. It performs the conversion of the data input (serial-to-parallel) and the data output (parallel-to-serial). The PCF8578 acts as an I^2C-bus slave transmitter/receiver in mixed mode, and as a slave receiver in row mode. A slave device cannot control bus communication.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

RAM access

RAM operations are only possible when the PCF8578 is in mixed mode. In this event its hardware subaddress is internally fixed at 0000 and the hardware subaddresses of any PCF8579 used in conjunction with the PCF8578 must start at 0001.

There are three RAM ACCESS modes:

- Character
- Half-graphic
- Full-graphic

These modes are specified by bits G1 and G0 of the RAM ACCESS command. The RAM ACCESS command controls the order in which data is written to or read from the RAM (see Fig.9).

To store RAM data, the user specifies the location into which the first byte will be loaded (see Fig.10):

- Device subaddress (specified by the DEVICE SELECT command)
- RAM X-address (specified by the LOAD X-ADDRESS command)
- RAM bank (specified by bits Y1 and Y0 of the RAM ACCESS command)

Subsequent data bytes will be written or read according to the chosen RAM access mode. Device subaddresses are automatically incremented between devices until the last device is reached. If the last device has subaddress 15, further display data transfers will lead to a wrap-around of the subaddress to 0.

Display control

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD via the column outputs. The number of rows scanned depends on the multiplex rate set by bits M1 and M0 of the SET MODE command.

The display status (all dots on/off and normal/inverse video) is set by bits E1 and E0 of the SET MODE command. For bank switching, the RAM bank corresponding to the top of the display is set by bits B1 and B0 of the SET START BANK command. This is shown in Fig.11. This feature is useful when scrolling in alphanumeric applications.

FUNCTIONAL DESCRIPTION (continued)

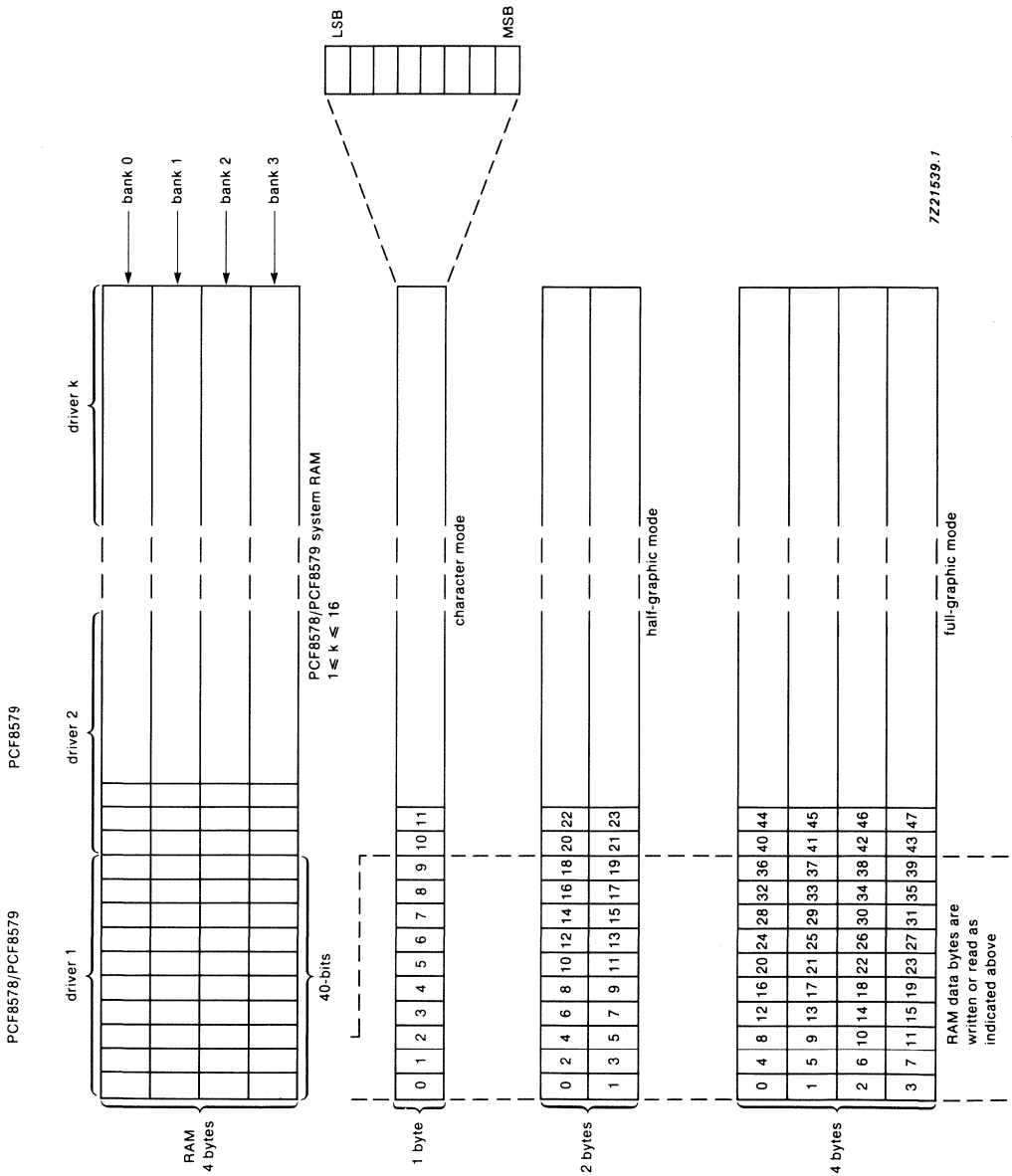


Fig.9 RAM access mode.

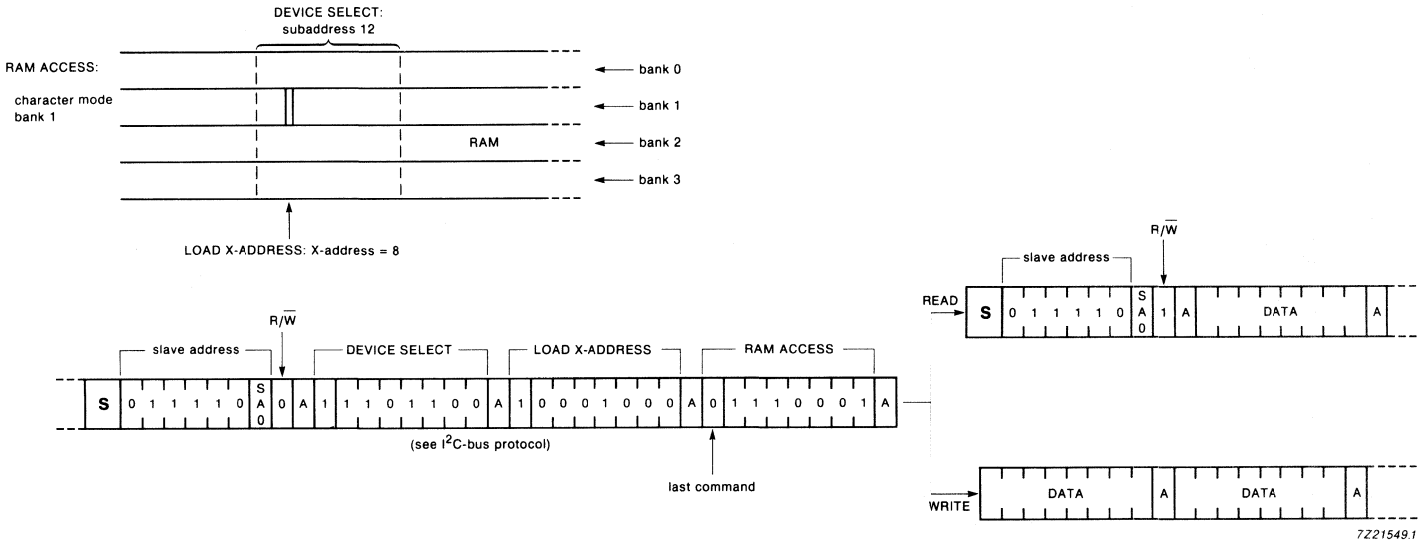


Fig.10 Example of commands specifying initial data byte RAM locations.

FUNCTIONAL DESCRIPTION (continued)

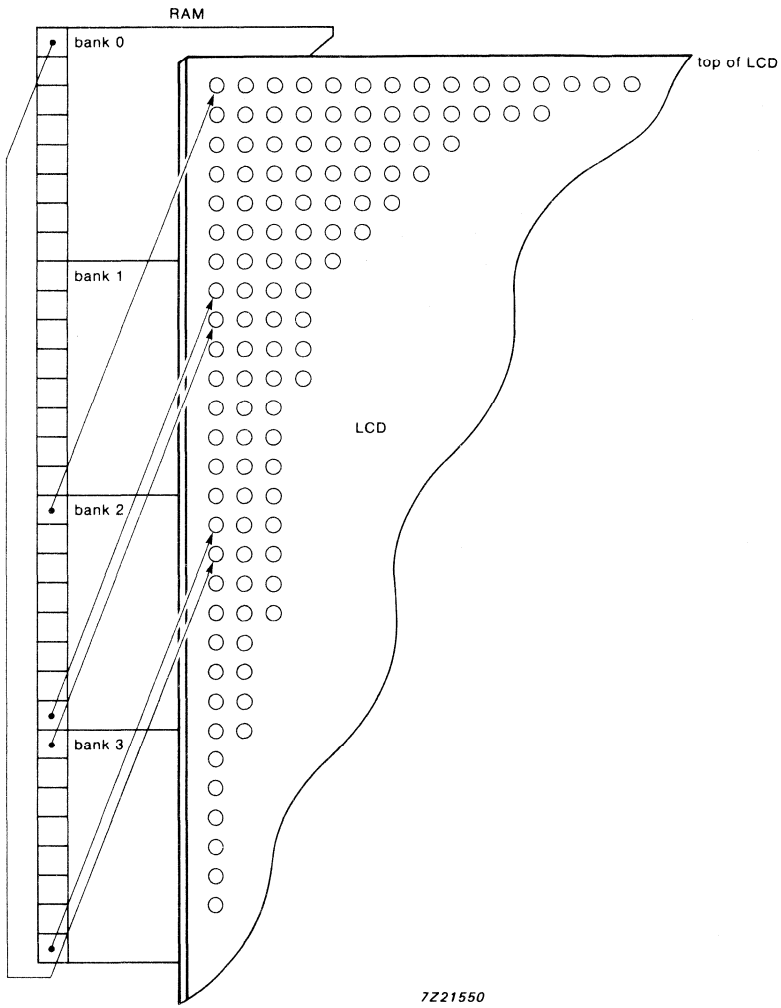


Fig.11 Relationship between display and SET START BANK; 1:32 multiplex rate and start bank = 2.

I²C-BUS PROTOCOL

Two 7-bit slave addresses (0111100 and 0111101) are reserved for both the PCF8578 and PCF8579. The least-significant bit of the slave address is set by connecting input SA0 to either 0 (V_{SS}) or 1 (V_{DD}). Therefore, two types of PCF8578 or PCF8579 can be distinguished on the same I²C-bus which allows:

(a) one PCF8578 to operate with up to 32 PCF8579s on the same I²C-bus for very large applications
(b) the use of two types of LCD multiplex schemes on the same I²C-bus.

In most applications the PCF8578 will have the same slave address as the PCF8579.

The I²C-bus protocol is shown in Fig. 12. All communications are initiated with a start condition (S) from the I²C-bus master, which is followed by the desired slave address and read/write bit. All devices with this slave address acknowledge in parallel. All other devices ignore the bus transfer.

In WRITE mode (indicated by setting the read/write bit LOW) one or more commands follow the slave address acknowledgement. The commands are also acknowledged by all addressed devices on the bus. The last command must clear the continuation bit C. After the last command a series of data bytes may follow. The acknowledgement after each byte is made only by the (A0, A1, A2 and A3) addressed PCF8579 or PCF8578 with its implicit subaddress 0. After the last data byte has been acknowledged, the I²C-bus master issues a stop condition (P).

In READ mode, indicated by setting the read/write bit HIGH, data bytes may be read from the RAM following the slave address acknowledgement. After this acknowledgement the master transmitter becomes a master receiver and the PCF8578 becomes a slave transmitter. The master receiver must acknowledge the reception of each byte in turn. The master receiver must signal an end of data to the slave transmitter, by **not** generating an acknowledge on the last byte clocked out of the slave. The slave transmitter then leaves the data line HIGH, enabling the master to generate a stop condition (P).

Display bytes are written into, or read from, the RAM at the address specified by the data pointer and subaddress counter. Both the data pointer and subaddress counter are automatically incremented, enabling a stream of data to be transferred either to, or from, the intended devices.

In multiple device applications, the hardware subaddress pins of the PCF8579s (A_0 to A_3) are connected to V_{SS} or V_{DD} to represent the desired hardware subaddress code. If two or more devices share the same slave address, then each device **must** be allocated a unique hardware subaddress.

I²C-BUS PROTOCOL (continued)

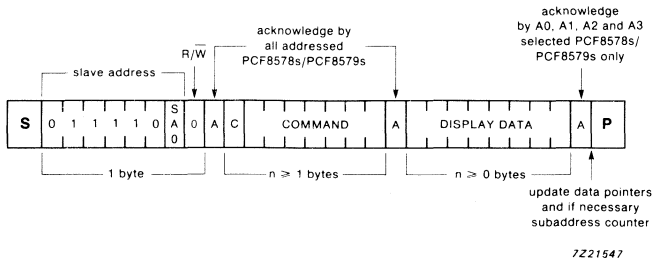


Fig.12(a) Master transmits to slave receiver (WRITE mode).

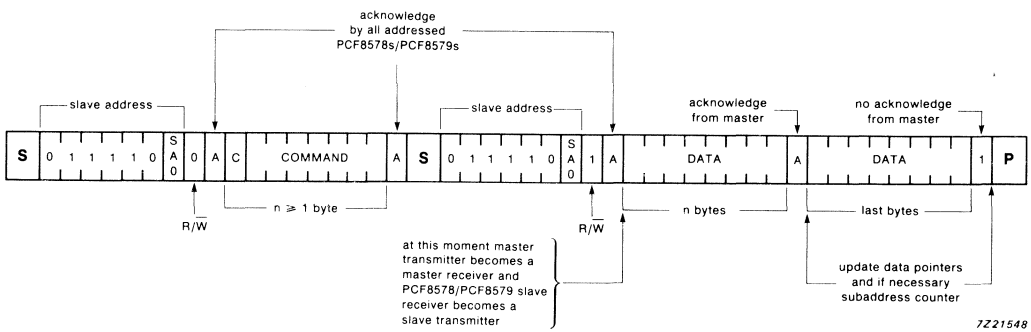


Fig.12(b) Master reads after sending command string (WRITE commands; READ data).

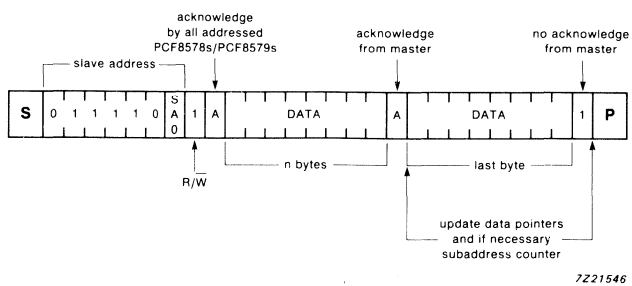
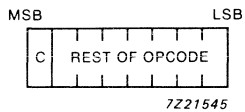


Fig.12(c) Master reads slave immediately after sending slave address (READ mode).

Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. The most-significant bit of a command is the continuation bit C (see Fig.13). When this bit is set, it indicates that the next byte to be transferred will also be a command. If the bit is reset, it indicates the conclusion of the command transfer. Further bytes will be regarded as display data. Commands are transferred in WRITE mode only.



C = 0; last command
C = 1; commands continue

Fig.13 General format of command byte.

The five commands available to the PCF8578 are defined in Tables 4 and 5.

Table 4 Summary of commands

code	command	description
C 0 D D D D D D	LOAD X-ADDRESS	0 to 39
C 1 0 D D D D D	SET MODE	multiplex rate, display status, system type
C 1 1 0 D D D D	DEVICE SELECT	defines device subaddress
C 1 1 1 D D D D	RAM ACCESS	graphic mode, bank select (D D D D ⩾ 12 is not allowed; see SET START BANK opcode)
C 1 1 1 1 1 D D	SET START BANK	defines bank at top of LCD

Where:

C = command continuation bit
D = may be a logic 1 or 0.

I²C-BUS PROTOCOL (continued)

Table 5 Definition of PCF8578/PCF8579 commands

command / opcode	options	description
SET MODE C 1 0 T E1 E0 M1 M0	LCD drive mode bits M1 M0 1:8 MUX (8 rows) 0 1 1:16 MUX (16 rows) 1 0 1:24 MUX (24 rows) 1 1 1:32 MUX (32 rows) 0 0	defines LCD drive mode
	display status bits E1 E0 blank 0 0 normal 0 1 all segments on 1 0 inverse video 1 1	defines display status
	system type bit T PCF8578 row only 0 PCF8578 mixed mode 1	defines system type
SET START BANK C 1 1 1 1 1 B1 B0	start bank pointer bits B1 B0 bank 0 0 0 bank 1 0 1 bank 2 1 0 bank 3 1 1	defines pointer to RAM bank corresponding to the top of the LCD. Useful for scrolling, pseudo-motion and background preparation of new display
DEVICE SELECT C 1 1 0 A3 A2 A1 A0	bits A3 A2 A1 A0 4-bit binary value of 0 to 15	four bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of sixteen hardware subaddresses

command / opcode	options	description
RAM ACCESS C 1 1 1 G1 G0 Y1 Y0	RAM access mode bits G1 G0 character 0 0 half graphic 0 1 full graphic 1 0 not allowed * 1 1	defines the auto-increment behaviour of the address for RAM access
	bits Y1 Y0 2-bit binary value of 0 to 3	two bits of immediate data, bits Y0 to Y1, are transferred to the Y-address pointer to define one of four banks for RAM access
LOAD X-ADDRESS C 0 X5 X4 X3 X2 X1 X0	bits X5 X4 X3 X2 X1 X0 6-bit binary value of 0 to 39	six bits of immediate data, bits X0 to X5, are transferred to the X-address pointer to define one of forty display RAM columns

DEVELOPMENT DATA

* See opcode for SET START BANK.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL) which must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this moment will be interpreted as control signals.

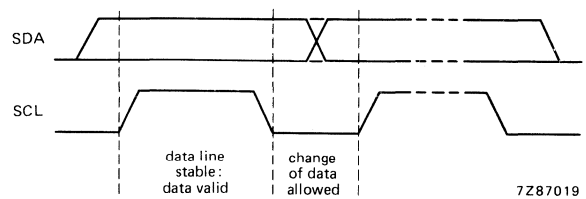


Fig.14 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

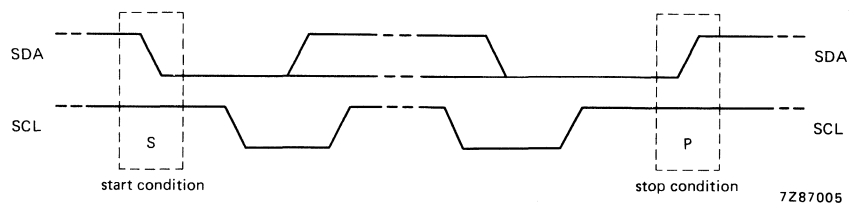


Fig.15 Definition of start and stop condition.

System configuration

A device transmitting a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message flow is the "master" and the devices which are controlled by the master are the "slaves".

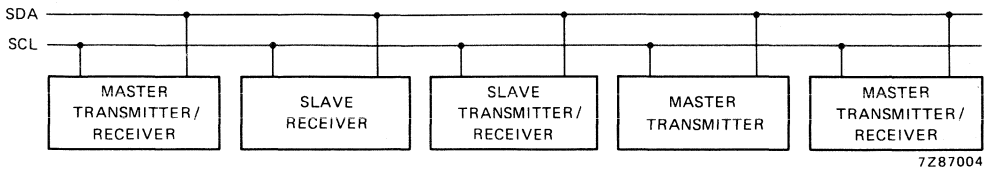


Fig.16 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal the end of a data transmission to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

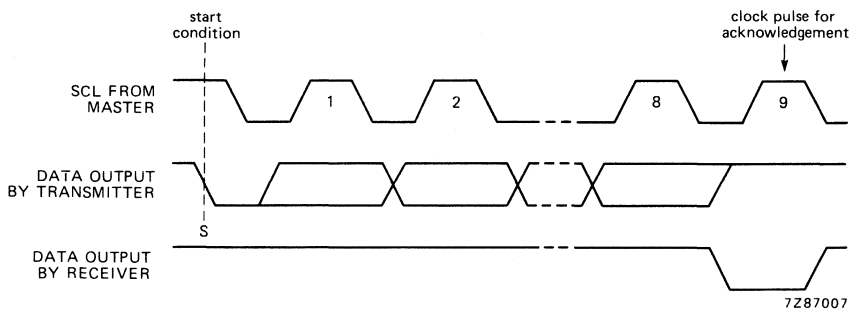


Fig.17 Acknowledgement on the I^2C-bus.

Note

The general characteristics and detailed specification of the I^2C-bus are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	+8.0	V
LCD supply voltage range	V_{LCD}	V_{DD} −11	V_{DD}	V
Input voltage range at SDA, SCL, CLK, TEST, SA0 and OSC	V_{I1}	V_{SS} −0.5	V_{DD} +0.5	V
V_2 to V_5	V_{I2}	V_{LCD} −0.5	V_{DD} +0.5	V
Output voltage range at $\overline{SYNC}$ and CLK	V_{O1}	V_{SS} −0.5	V_{DD} +0.5	V
R0 to R7, R8/C8 to R31/C31, and C32 to C39	V_{O2}	V_{LCD} −0.5	V_{DD} +0.5	V
DC input current	I_I	−10	10	mA
DC output current	I_O	−10	10	mA
V_{DD}, V_{SS} or V_{LCD} current	I_{DD}, I_{SS}, I_{LCD}	−50	50	mA
Power dissipation per package	P_{tot}	−	400	mW
Power dissipation per output	P_o	−	100	mW
Storage temperature range	T_{stg}	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{DD} = 2.5 V to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9 V; T_{amb} = −40 °C to + 85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
LCD supply voltage		V_{LCD}	V_{DD} −9	–	V_{DD} −3.5	V
Supply current	note 1;					
external clock	f_{CLK} = 2 kHz	I_{DD1}	–	6	15	μA
internal clock	R_{OSC} = 330 kΩ	I_{DD2}	–	20	50	μA
Power-on reset level	note 2	V_{POR}	0.8	1.3	1.8	V
Logic						
Input voltage LOW		V_{IL}	V_{SS}	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Output current LOW at $\overline{SYNC}$ and CLK	V_{OL} = 1.0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH at $\overline{SYNC}$ and CLK	V_{OH} = 4.0 V; V_{DD} = 5 V	I_{OH1}	–	–	−1	mA
SDA output current LOW	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL2}	3.0	–	–	mA
Leakage current at SDA, SCL, $\overline{SYNC}$, CLK, TEST and SA0	V_I = V_{DD} or V_{SS}	I_{L1}	−1	–	1	μA
Leakage current at OSC	V_I = V_{DD}	I_{L2}	−1	–	1	μA
Input capacitance at SCL and SDA	note 3	C_I	–	–	5	pF
LCD outputs						
Leakage current at V_2 to V_5	V_I = V_{DD} or V_{LCD}	I_{L3}	−2	–	2	μA
DC component of LCD drivers R0 to R7, R8/C8 to R31/C31, and C32 to C39		± V_{DC}	–	20	–	mV
Output resistance at R0 to R7 and R8/C8 to R31/C31	note 4; row mode	R_{ROW}	–	1.5	3.0	kΩ
R8/C8 to R31/C31 and C32 to C39	column mode	R_{COL}	–	3	6	kΩ

AC CHARACTERISTICS (note 5)

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9 V; T_{amb} = − 40 to +85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Clock frequency at multiplex rates of 1:8, 1:16 and 1:32	R_{OSC} = 330 kΩ; V_{DD} = 6 V	f_{CLK1}	1.2	2.1	3.3	kHz
1:24		f_{CLK2}	0.9	1.6	2.5	kHz
$\overline{SYNC}$ propagation delay		t_{PSYNC}	–	–	500	ns
Driver delays	V_{DD} − V_{LCD} = 9 V; with test loads	t_{PLCD}	–	–	100	μs
I²C-bus						
SCL clock frequency		f_{SCL}	–	–	100	kHz
Tolerable spike width on bus		t_{SW}	–	–	100	ns
Bus free time		t_{BUF}	4.7	–	–	μs
Start condition set-up time	repeated start codes only	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time		$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time		t_{LOW}	4.7	–	–	μs
SCL HIGH time		t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time		t_r	–	–	1.0	μs
SCL and SDA fall time		t_f	–	–	0.3	μs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Data hold time		$t_{HD;DAT}$	0	–	–	ns
Stop condition set-up time		$t_{SU;STO}$	4.0	–	–	μs

Notes to the characteristics

1. Outputs are open; inputs at V_{DD} or V_{SS}; I^2C-bus inactive; external clock with 50% duty factor, (I_{DD1} only).
2. Resets all logic when $V_{DD} < V_{POR}$.
3. Periodically sampled; not 100% tested.
4. Resistance measured between output terminal (R0 to R7, R8/C8 to R31/C31 and C32 to C39) and bias input (V_2 to V_5, V_{DD} and V_{LCD}) when the specified current flows through one output under the following conditions (see Table 2):

   $V_{OP} = V_{DD} - V_{LCD} = 9$ V;

   row mode, R0 to R7 and R8/C8 to R31/C31 (row mode):
   $V_2 - V_{LCD} \geqslant 6.65$ V; $V_5 - V_{LCD} \leqslant 2.35$ V; $I_{LOAD} = 150\ \mu$A

   column mode, R8/C8 to R31/C31 (column mode) and C32 to C39:
   $V_3 - V_{LCD} \geqslant 4.70$ V; $V_4 - V_{LCD} \leqslant 4.30$ V; $I_{LOAD} = 100\ \mu$A.
5. All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

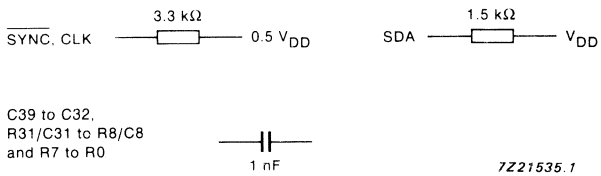


Fig.18 Test loads.

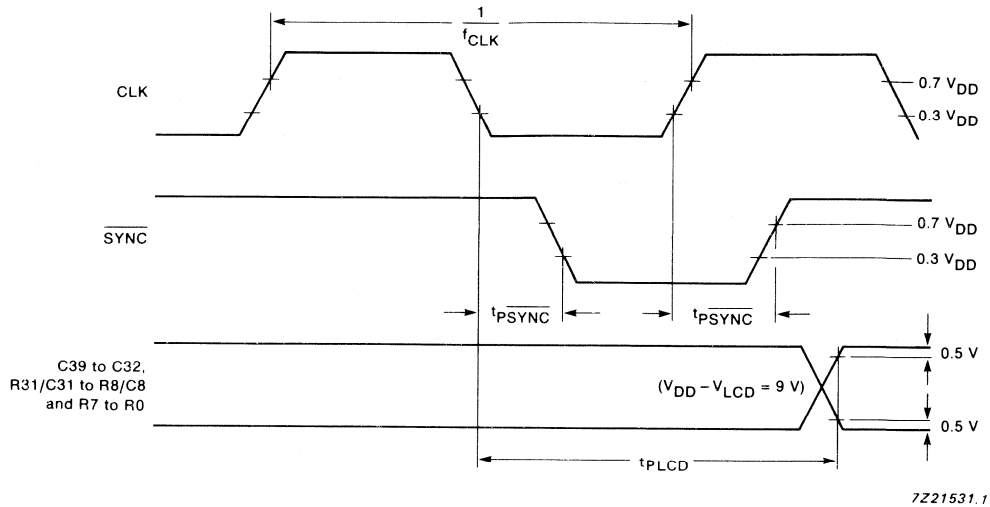


Fig.19 Driver timing waveforms.

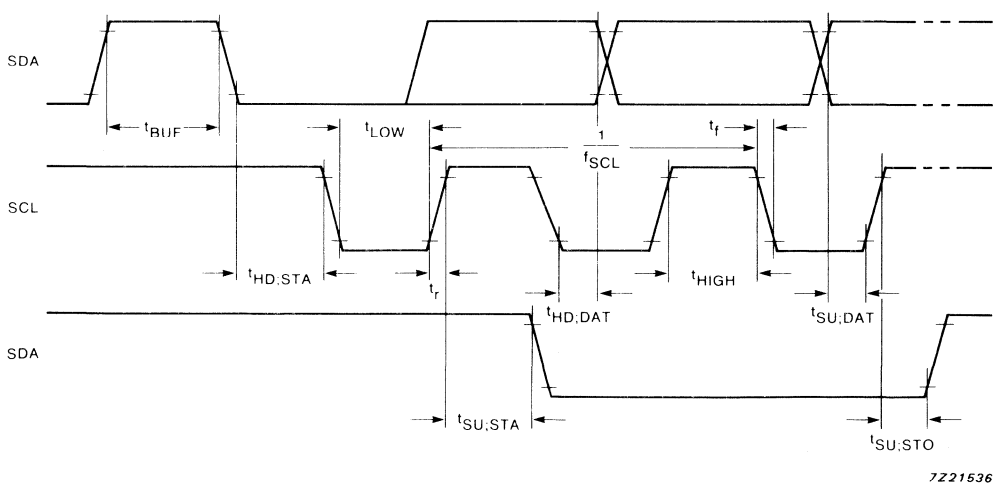


Fig.20 I^2C-bus timing waveforms.

APPLICATION INFORMATION

DEVELOPMENT DATA

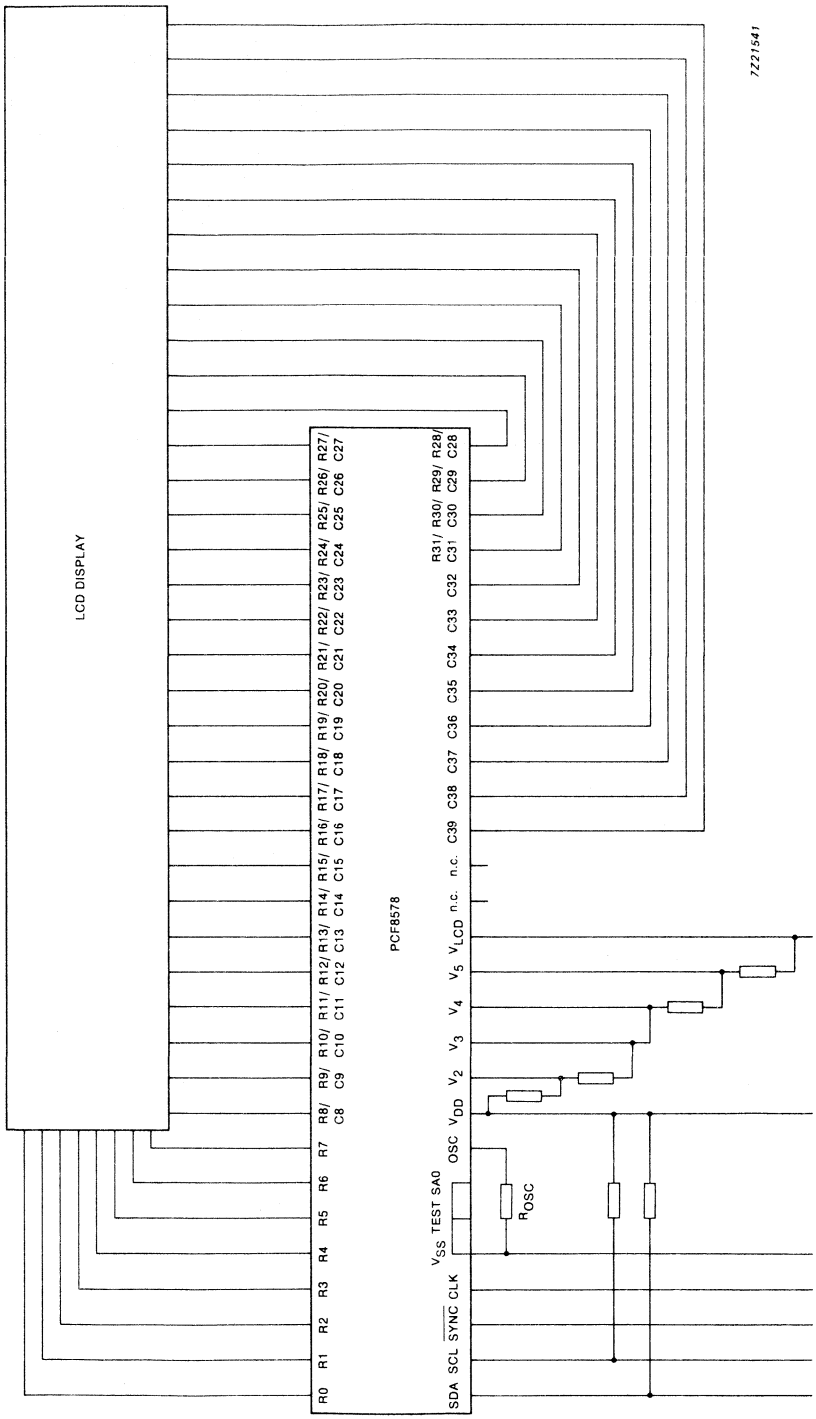


Fig.21 Stand-alone application using 8 rows and 32 columns.

APPLICATION INFORMATION (continued)

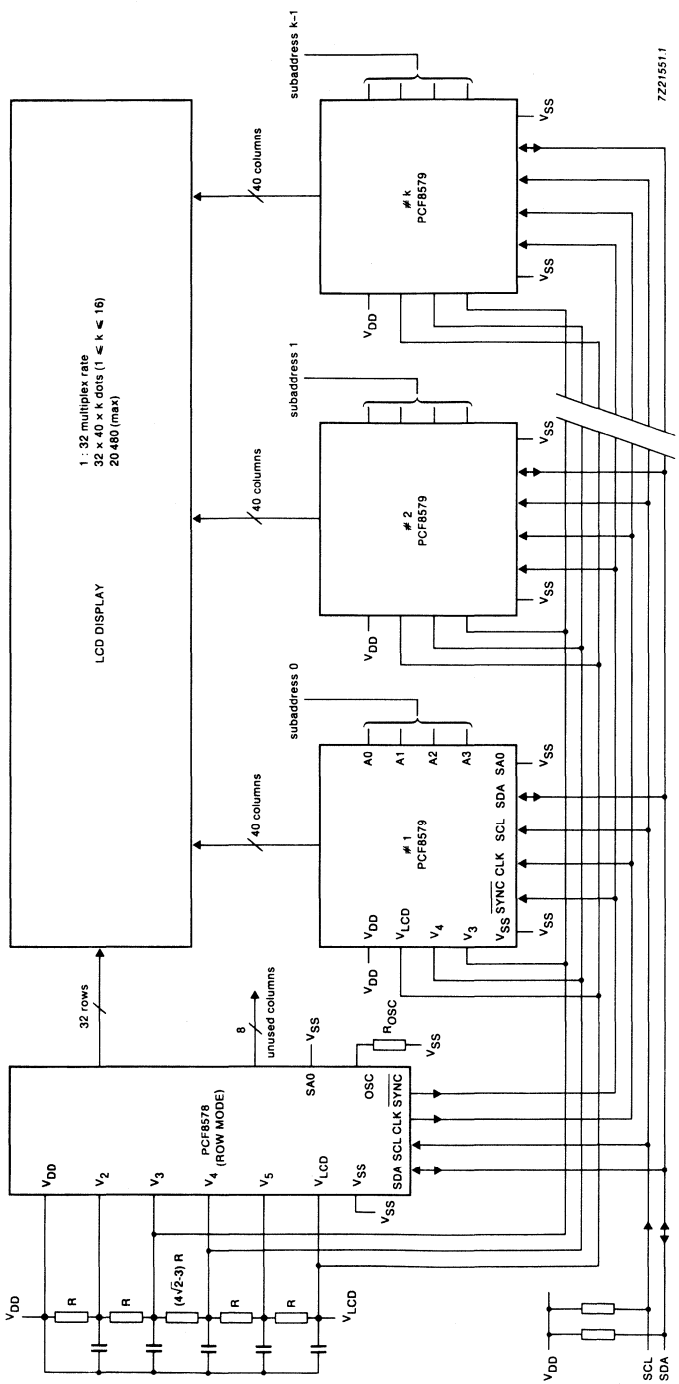


Fig.22 Typical LCD driver system with 1:32 multiplex rate.

DEVELOPMENT DATA

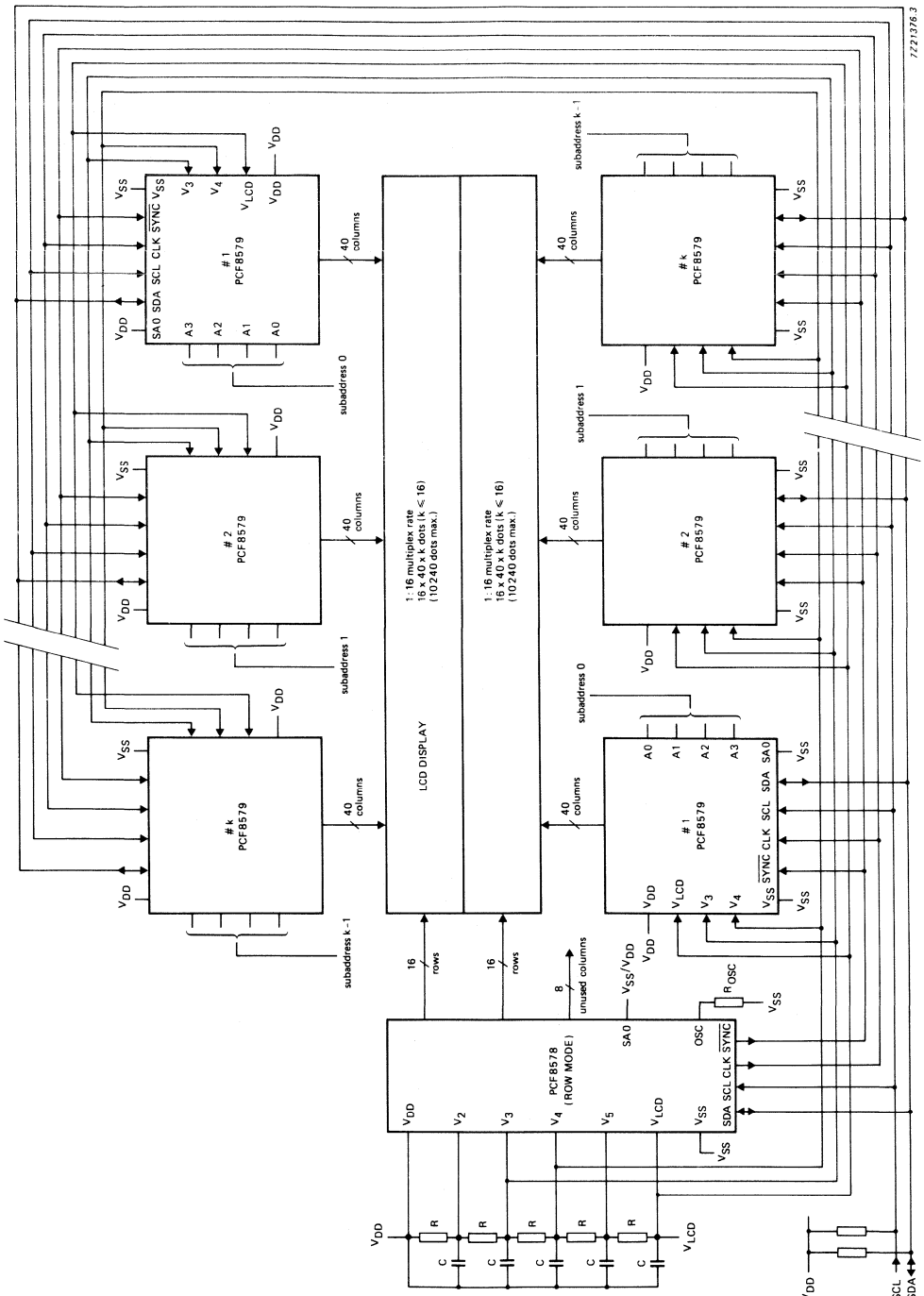


Fig.23 Split screen application with 1:16 multiplex rate for improved contrast.

APPLICATION INFORMATION (continued)

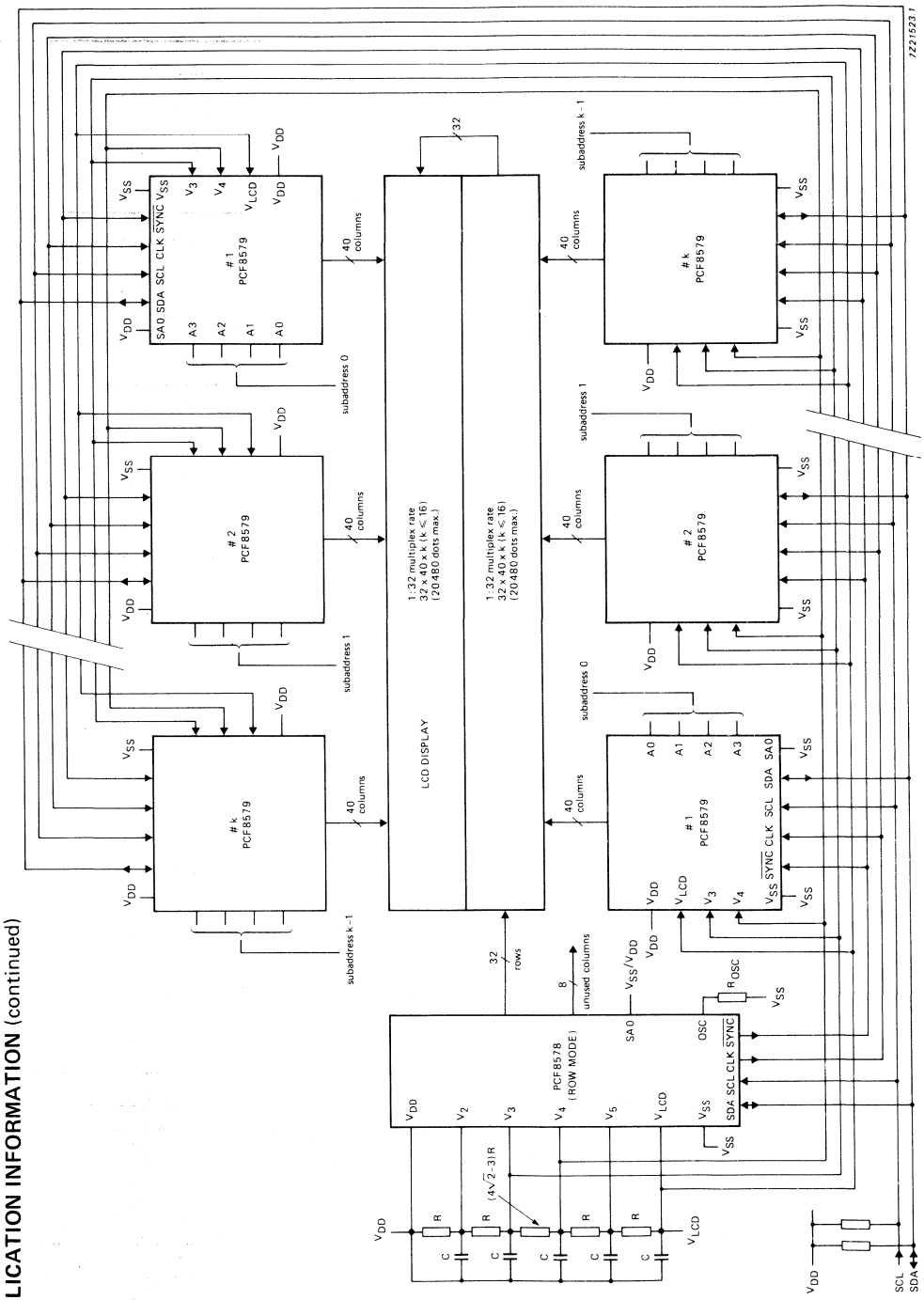


Fig.24 Split screen application with 1:32 multiplex rate.

DEVELOPMENT DATA

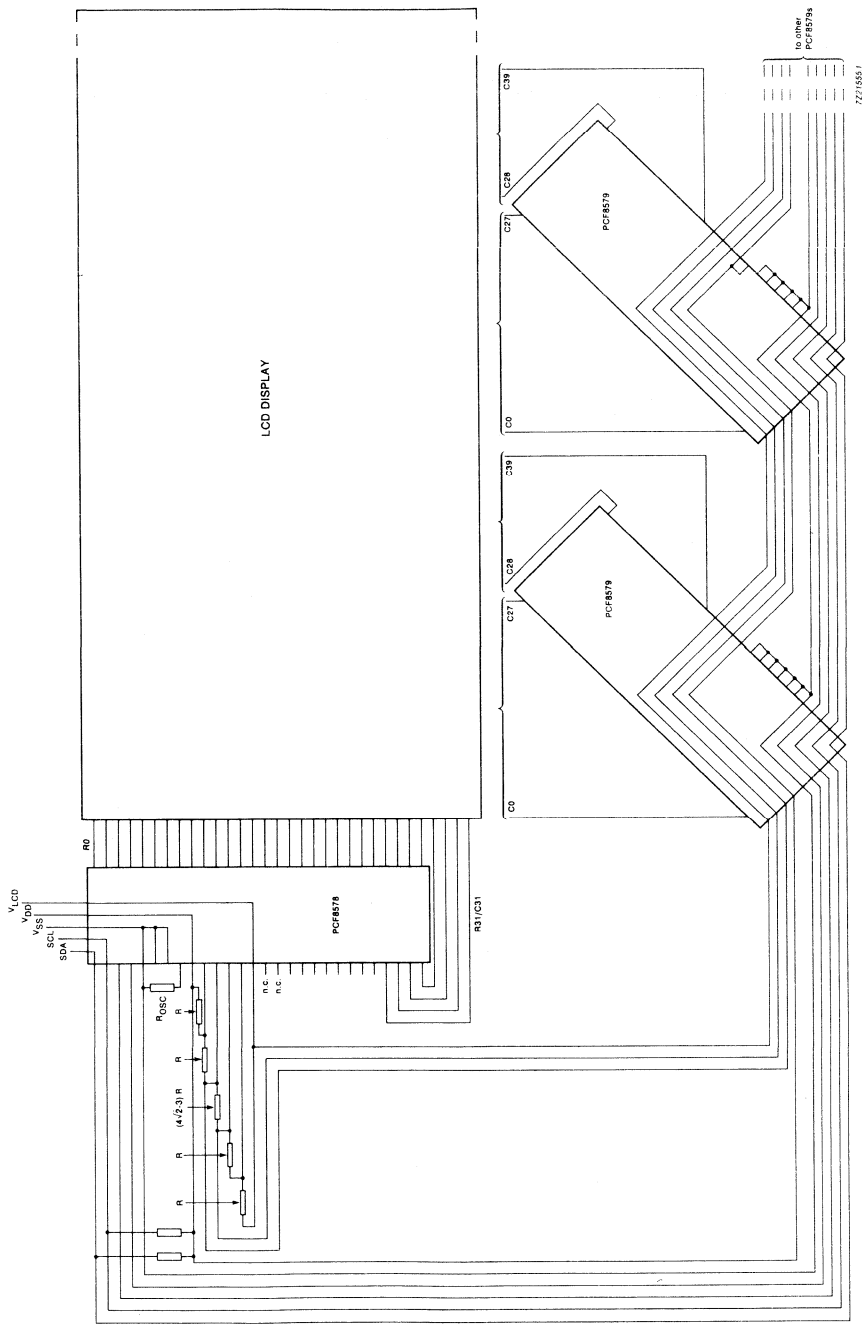
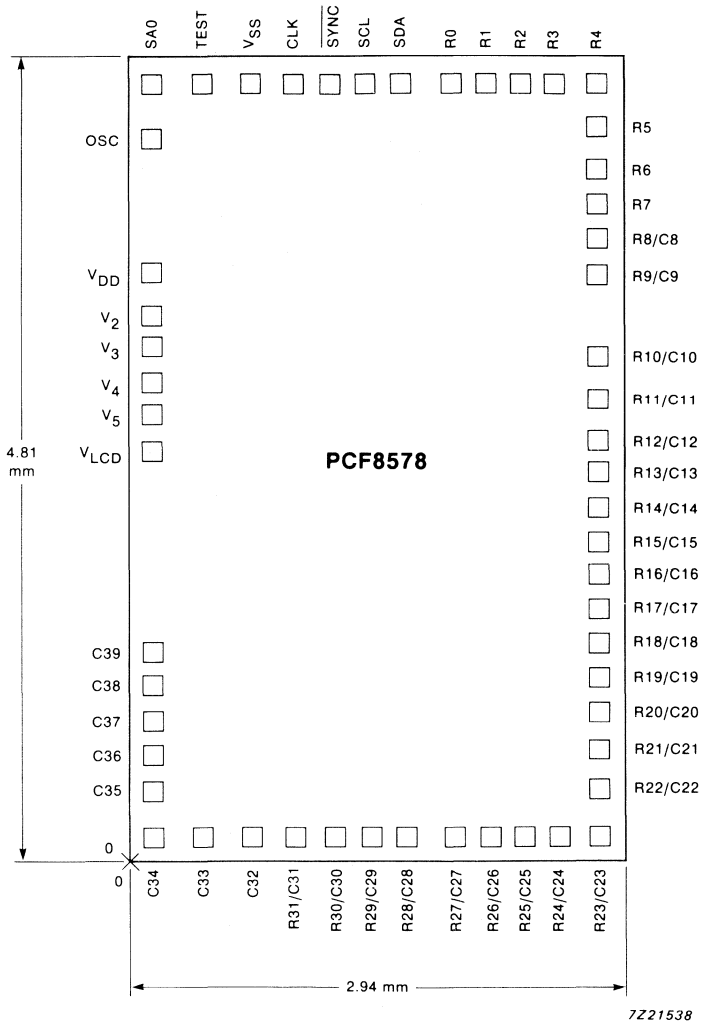


Fig.25 Example of single plane wiring, single screen with 1:32 multiplex rate (PCF8578 in row driver mode).

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 14.14 mm^2
Bonding pad dimensions: 120 μm x 120 μm.

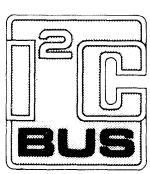
Fig.26 Bonding pad locations.

Table 6 Bonding pad locations (dimensions in μm)

All x/y co-ordinates are referenced to the bottom left corner, see Fig.26.

pad	X	Y	pad	X	Y
SDA	1642	4642	R27/C27	1936	160
SCL	1438	4642	R26/C26	2140	160
$\overline{SYNC}$	1234	4642	R25/C25	2344	160
CLK	1000	4642	R24/C24	2548	160
V_{SS}	742	4642	R23/C23	2776	160
TEST	454	4642	R22/C22	2776	424
SA0	160	4642	R21/C21	2776	670
OSC	160	4318	R20/C20	2776	886
V_{DD}	160	3514	R19/C19	2776	1096
V_2	160	3274	R18/C18	2776	1300
V_3	160	3064	R17/C17	2776	1504
V_4	160	2860	R16/C16	2776	1708
V_5	160	2656	R15/C15	2776	1912
V_{LCD}	160	2452	R14/C14	2776	2116
n.c.	–	–	R13/C13	2776	2320
n.c.	–	–	R12/C12	2776	2524
C39	160	1252	R11/C11	2776	2752
C38	160	1048	R10/C10	2776	3004
C37	160	844	R9/C9	2776	3502
C36	160	628	R8/C8	2776	3706
C35	160	406	R7	2776	3916
C34	160	160	R6	2776	4132
C33	454	160	R5	2776	4378
C32	742	160	R4	2776	4642
R31/C31	1000	160	R3	2548	4642
R30/C30	1234	160	R2	2344	4642
R29/C29	1438	160	R1	2140	4642
R28/C28	1642	160	R0	1936	4642

DEVELOPMENT DATA



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CHIP-ON GLASS INFORMATION

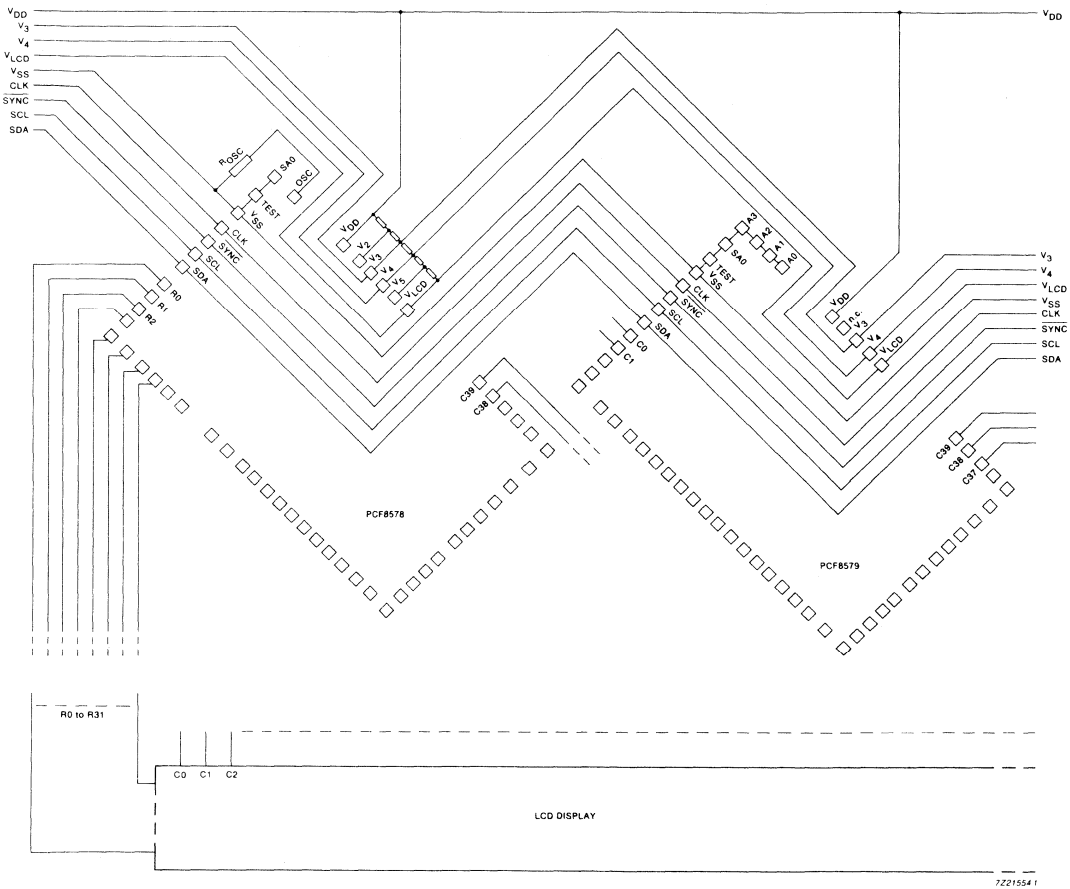


Fig.27 Typical chip-on glass application (viewed from underside of chip).

Note to Fig.27

If inputs SA0 and A0 to A3 are left unconnected they are internally pulled-up to V_{DD}.

LCD COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8, 1:16, 1:24 or 1:32. The device has 40 outputs and can drive 32 x 40 dots in a 32 row multiplexed LCD. Up to 16 PCF8579s can be cascaded and up to 32 devices may be used on the same I²C-bus (using the two slave addresses). The device is optimized for use with the PCF8578 LCD row/column driver. Together these two devices form a general LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40,960 dots
- 40 column outputs
- Selectable multiplex rates; 1:8, 1:16, 1:24 or 1:32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8579T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8579V: 64-lead tape-automated-bonding module (SOT267A).
PCF8579U: chip with bumps on-tape.

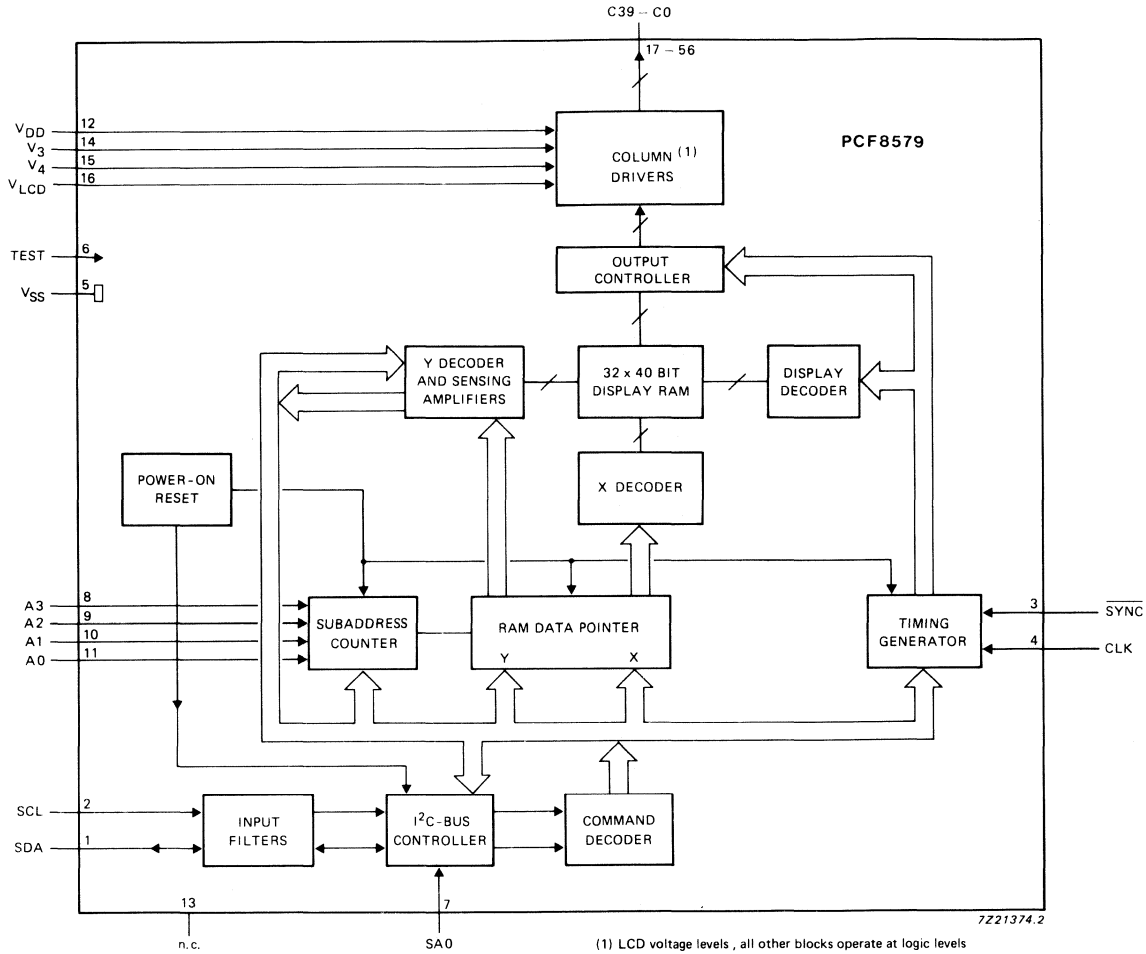


Fig.1 Block diagram.

DEVELOPMENT DATA

PINNING

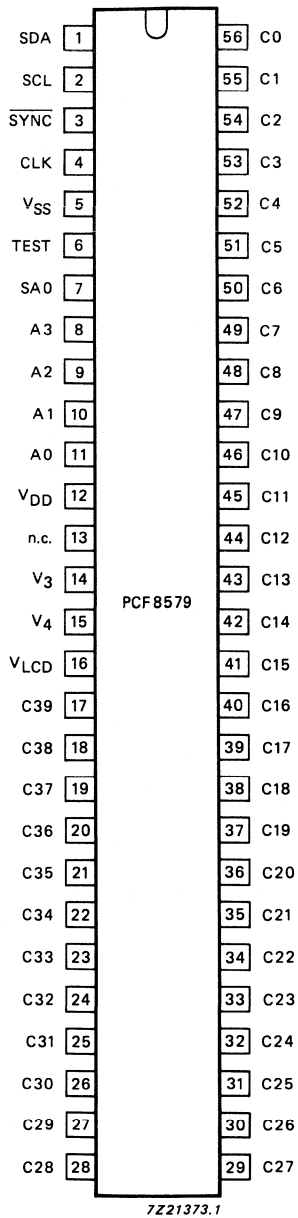
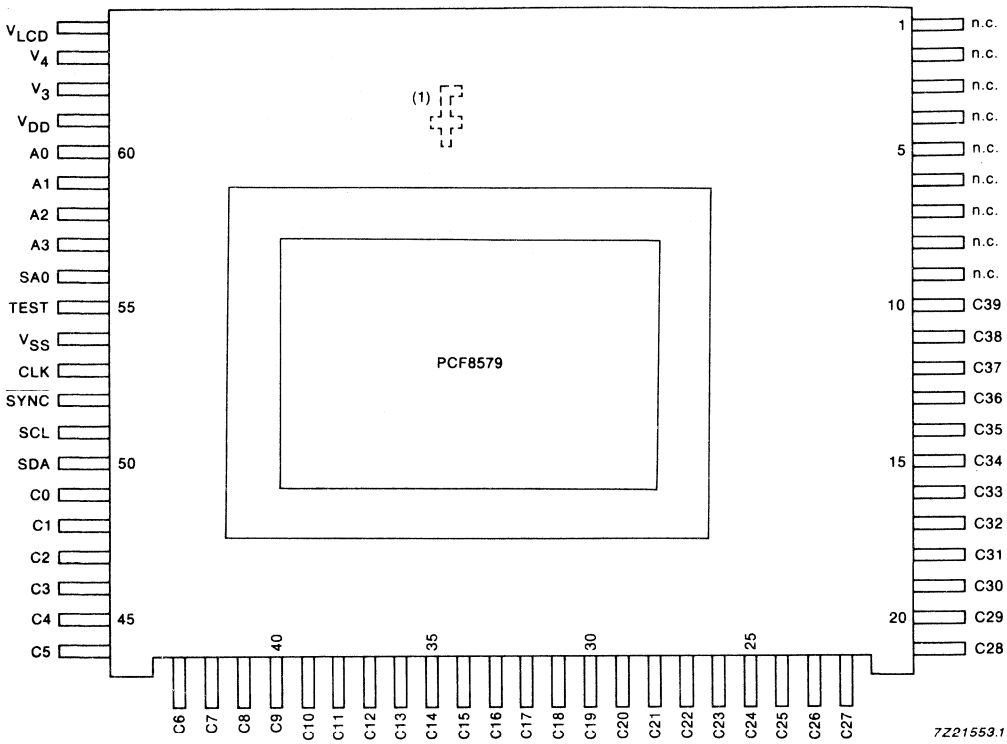


Fig.2 (a) Pinning diagram: VSO56; SOT190.

PINNING (continued)



(1) Orientation mark.

Fig.2 (b) Pinning diagram: SO122.

mnemonic	pin no.		description
	SOT190	SO122	
SDA	1	50	I^2C-bus serial data line
SCL	2	51	I^2C-bus serial clock line
$\overline{SYNC}$	3	52	cascade synchronization input
CLK	4	53	external clock input
V_{SS}	5	54	ground (logic)
TEST	6	55	test pin (connect to V_{SS})
SA0	7	56	I^2C-bus slave address input (bit 0)
A3 to A0	8 - 11	57 - 60	I^2C-bus subaddress inputs
V_{DD}	12	61	positive supply voltage
n.c.	13 *	1 - 9	not connected
V_3 to V_4	14 - 15	62 - 63	LCD bias voltage inputs
V_{LCD}	16	64	LCD supply voltage
C39 to C0	17 - 56	10 - 49	LCD column driver outputs

DEVELOPMENT DATA

* Do not connect, this pin is reserved.

FUNCTIONAL DESCRIPTION

The PCF8579 column driver is designed for use with the PCF8578. Together they form a general purpose LCD dot matrix chip set.

Typically up to 16 PCF8579s may be used with one PCF8578. Each of the PCF8579s is identified by a unique 4-bit hardware subaddress, set by pins A0 to A3. The PCF8578 can operate with up to 32 PCF8579s when using two I^2C-bus slave addresses. The two slave addresses are set by the logic level on input SA0.

Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the LCD threshold voltage (V_{th}). V_{th} is typically defined as the RMS voltage at which the LCD exhibits 10% contrast. Table 1 shows the optimum voltage bias levels for the PCF8578/PCF8579 chip set as functions of V_{op} ($V_{op} = V_{DD} - V_{LCD}$), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{op} is obtained by equating $V_{off(rms)}$ with V_{th}.

Table 1 Optimum LCD bias voltages

parameter	multiplex rate			
	1:8	1:16	1:24	1:32
$\frac{V_2}{V_{op}}$	0.739	0.800	0.830	0.850
$\frac{V_3}{V_{op}}$	0.522	0.600	0.661	0.700
$\frac{V_4}{V_{op}}$	0.478	0.400	0.339	0.300
$\frac{V_5}{V_{op}}$	0.261	0.200	0.170	0.150
$\frac{V_{off(rms)}}{V_{op}}$	0.297	0.245	0.214	0.193
$\frac{V_{on(rms)}}{V_{op}}$	0.430	0.316	0.263	0.230
$D = \frac{V_{on(rms)}}{V_{off(rms)}}$	1.447	1.291	1.230	1.196
$\frac{V_{op}}{V_{th}}$	3.37	4.08	4.68	5.19

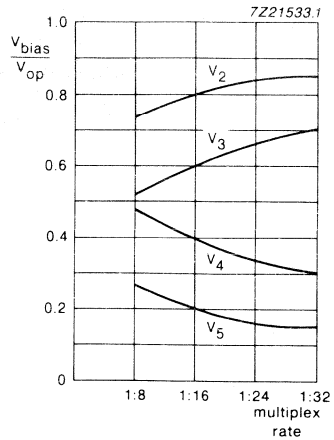


Fig.3 LCD bias voltage as a function of the multiplex rate.

DEVELOPMENT DATA

Power-on reset

At power-on the PCF8579 resets to a defined starting condition as follows.

1. Display blank (in conjunction with PCF8578)
2. 1:32 multiplex rate
3. start bank 0 selected
4. Data pointer is set to X, Y address 0, 0
5. Character mode
6. Subaddress counter is set to 0
7. I^2C-bus is initialized.

Data transfers on the I^2C-bus should be avoided for 1 ms following power-on, to allow completion of the reset action.

FUNCTIONAL DESCRIPTION (continued)

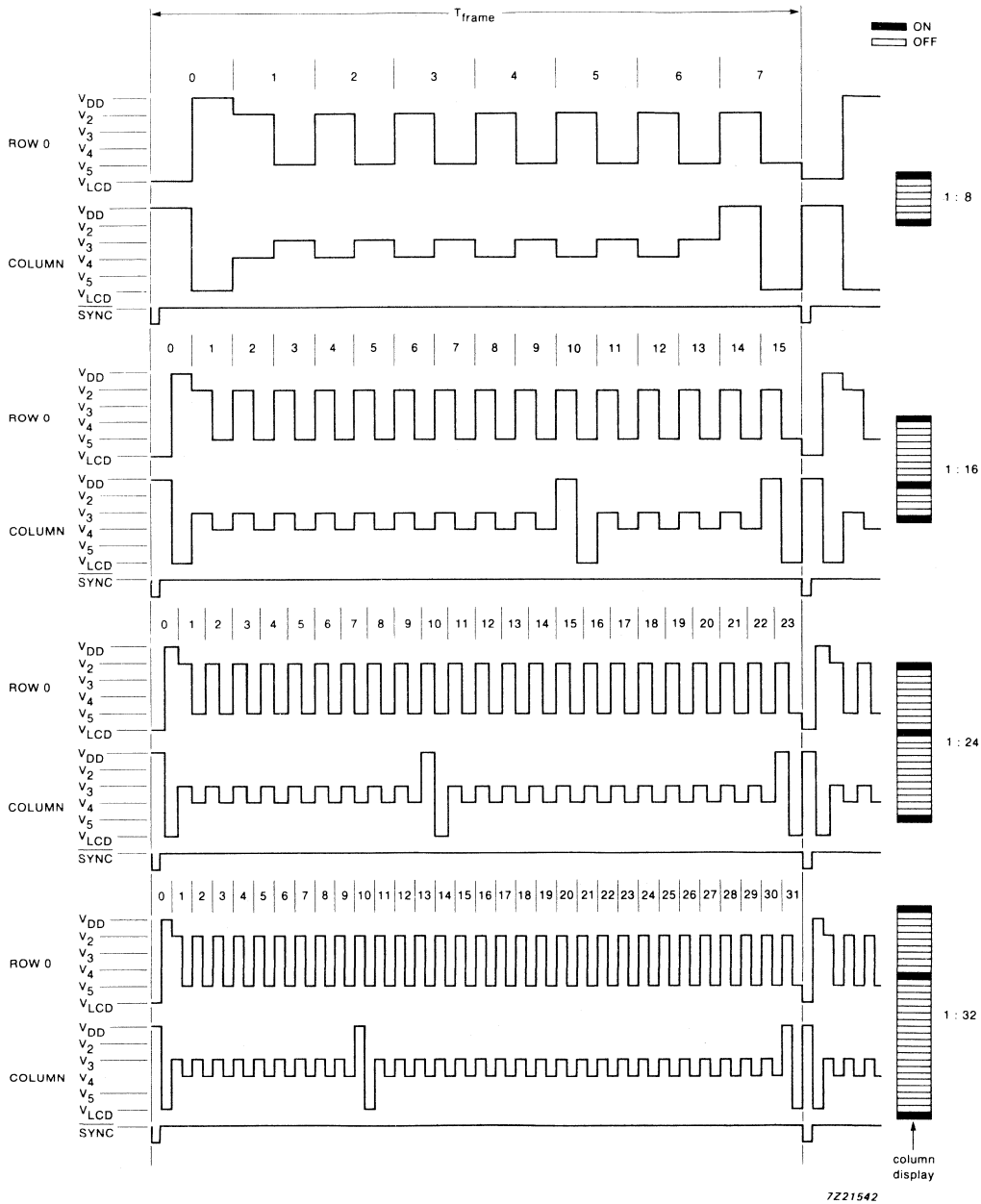
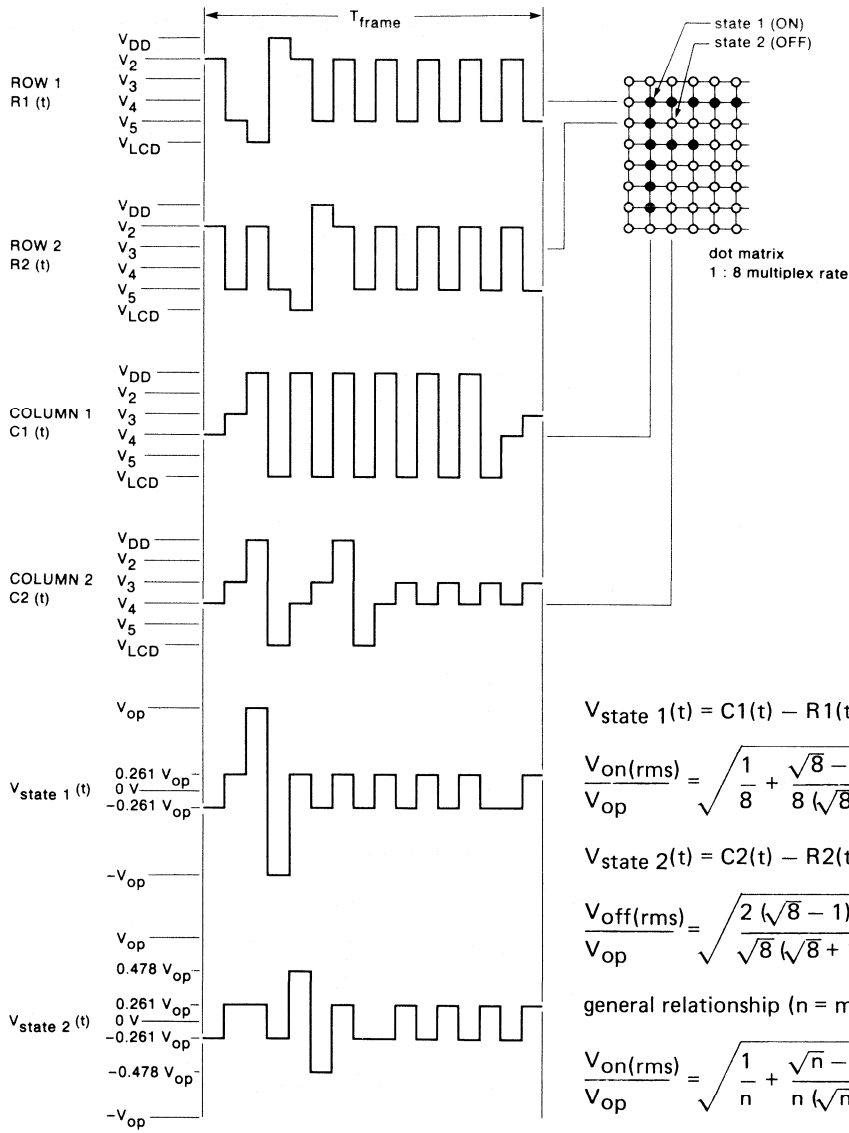


Fig.4 LCD row/column waveforms.

DEVELOPMENT DATA



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{8} + \frac{\sqrt{8}-1}{8(\sqrt{8}+1)}} = 0.430$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{8}-1)}{\sqrt{8}(\sqrt{8}+1)^2}} = 0.297$$

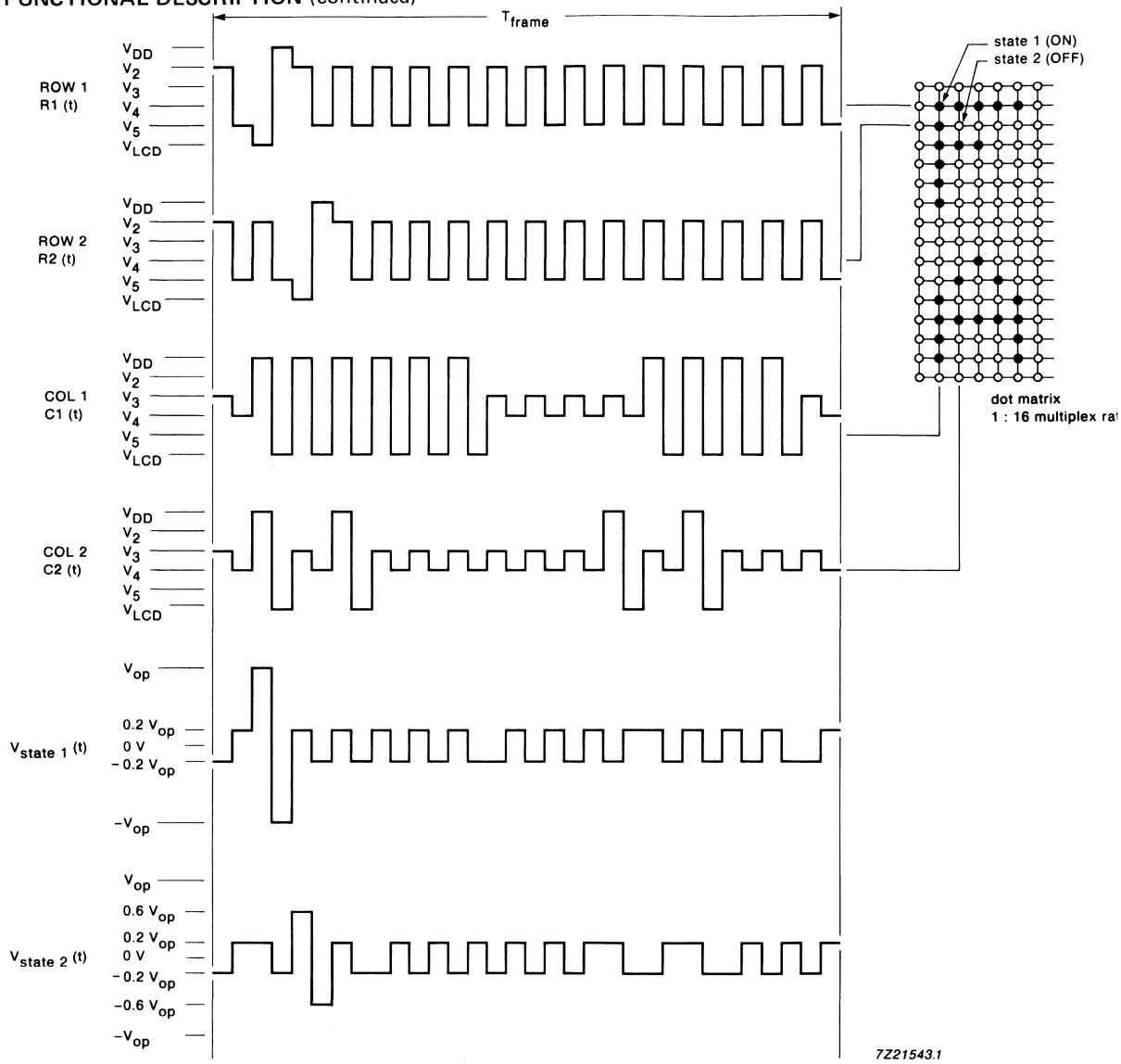
general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n(\sqrt{n}+1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}}$$

Fig.5 LCD drive mode waveforms for 1:8 multiplex rate.

FUNCTIONAL DESCRIPTION (continued)



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{16} + \frac{\sqrt{16} - 1}{16\,(\sqrt{16} + 1)}} = 0.316$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{16} - 1)}{\sqrt{16}\,(\sqrt{16} + 1)^2}} = 0.245$$

general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n} - 1}{n\,(\sqrt{n} + 1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{n} - 1)}{\sqrt{n}\,(\sqrt{n} + 1)^2}}$$

Fig.6 LCD drive mode waveforms for 1:16 multiplex rate.

Timing generator

The timing generator of the PCF8579 organizes the internal data flow from the RAM to the display drivers. An external synchronization pulse $\overline{\text{SYNC}}$ is received from the PCF8578. This signal maintains the correct timing relationship between cascaded devices.

Column drivers

Outputs C0 to C39 are column drivers which must be connected to the LCD. Unused outputs should be left open-circuit.

Display RAM

The PCF8579 contains a 32 x 40 bit static RAM which stores the display data. The RAM is divided into 4 banks of 40 bytes (4 x 8 x 40 bits). During RAM access, data is transferred to/from the RAM via the I^2C-bus.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows an individual data byte or a series of data bytes to be written into or read from the display RAM, as specified by commands sent on the I^2C-bus.

Subaddress counter

The storage and retrieval of display data is dependent on the content of the subaddress counter. Storage and retrival take place, only when the contents of the subaddress counter agree with the hardware subaddress at pins A0, A1, A2 and A3.

I^2C-bus controller

The I^2C-bus controller detects the I^2C-bus protocol, slave address, commands and display data bytes. It performs the conversion of the data input (serial-to-parallel) and the data output (parallel-to-serial). The PCF8579 acts as an I^2C-bus slave transmitter/receiver. Device selection depends on the I^2C-bus slave address, the hardware subaddress and the commands transmitted.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

FUNCTIONAL DESCRIPTION (continued)

RAM access

There are three RAM ACCESS modes:

- Character
- Half-graphic
- Full-graphic

These modes are specified by bits G1 and G0 of the RAM ACCESS command. The RAM ACCESS command controls the order in which data is written to or read from the RAM (see Fig.7).

To store RAM data, the user specifies the location into which the first byte will be loaded (see Fig.8):

- Device subaddress (specified by the DEVICE SELECT command)
- RAM X-address (specified by the LOAD X-ADDRESS command)
- RAM bank (specified by bits Y1 and Y0 of the RAM ACCESS command)

Subsequent data bytes will be written or read according to the chosen RAM access mode. Device subaddresses are automatically incremented between devices until the last device is reached. If the last device has subaddress 15, further display data transfers will lead to a wrap-around of the subaddress to 0.

Display control

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD, via the column outputs. The number of rows scanned depends on the multiplex rate set by bits M1 and M0 of the SET MODE command.

The display status (all dots on/off and normal/inverse video) is set by bits E1 and E0 of the SET MODE command. For bank switching, the RAM bank corresponding to the top of the display is set by bits B1 and B0 of the SET START BANK command. This is shown in Fig.9. This feature is useful when scrolling in alphanumeric applications.

DEVELOPMENT DATA

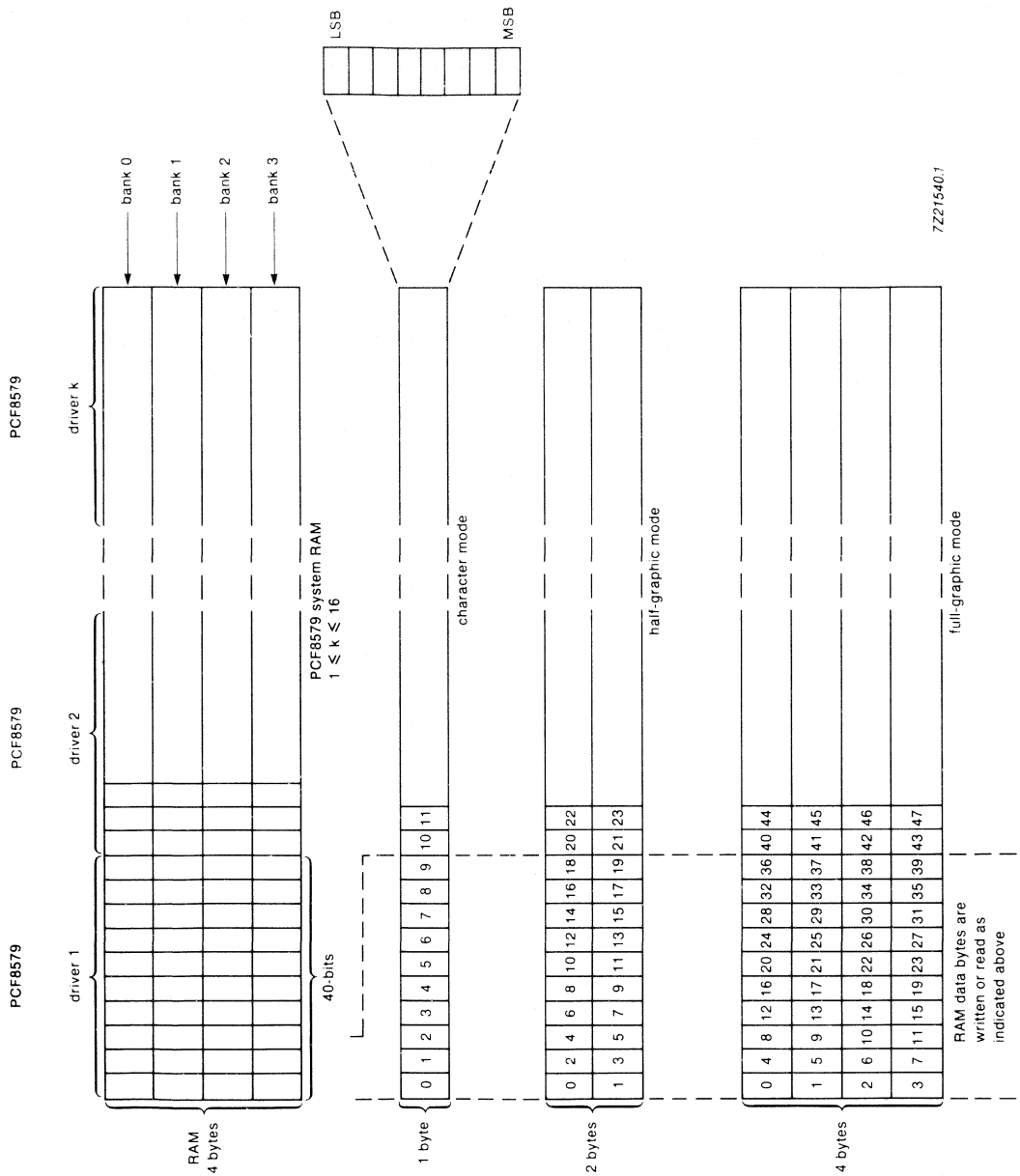


Fig.7 RAM ACCESS mode.

FUNCTIONAL DESCRIPTION (continued)

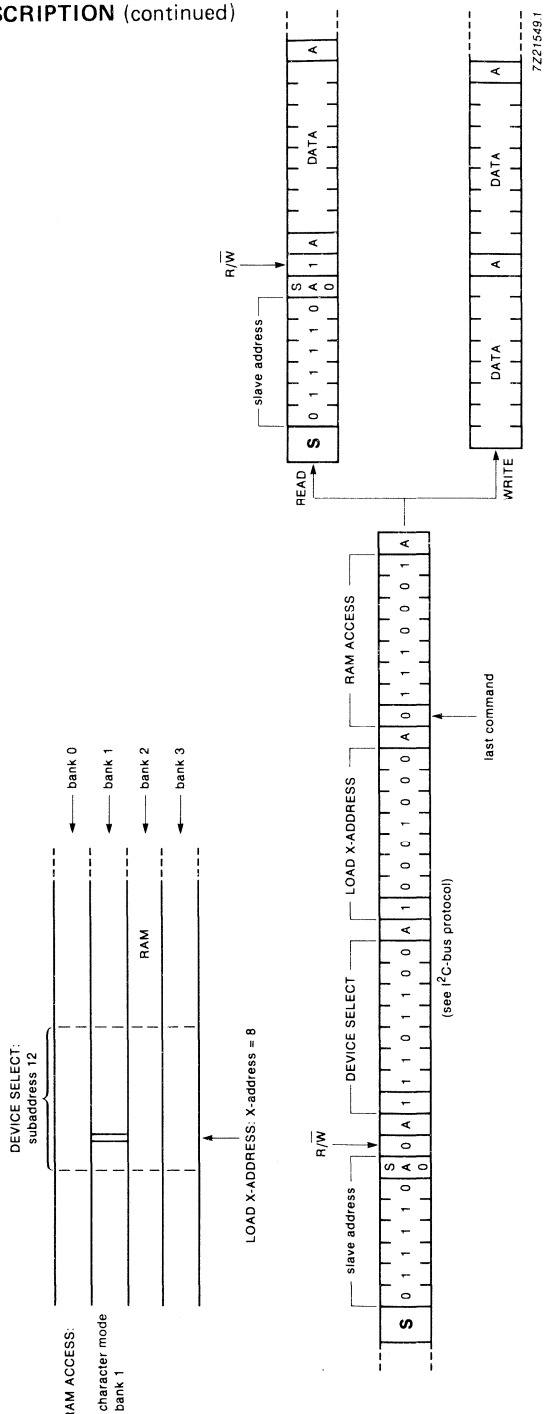


Fig.8 Example of commands specifying initial data byte RAM locations.

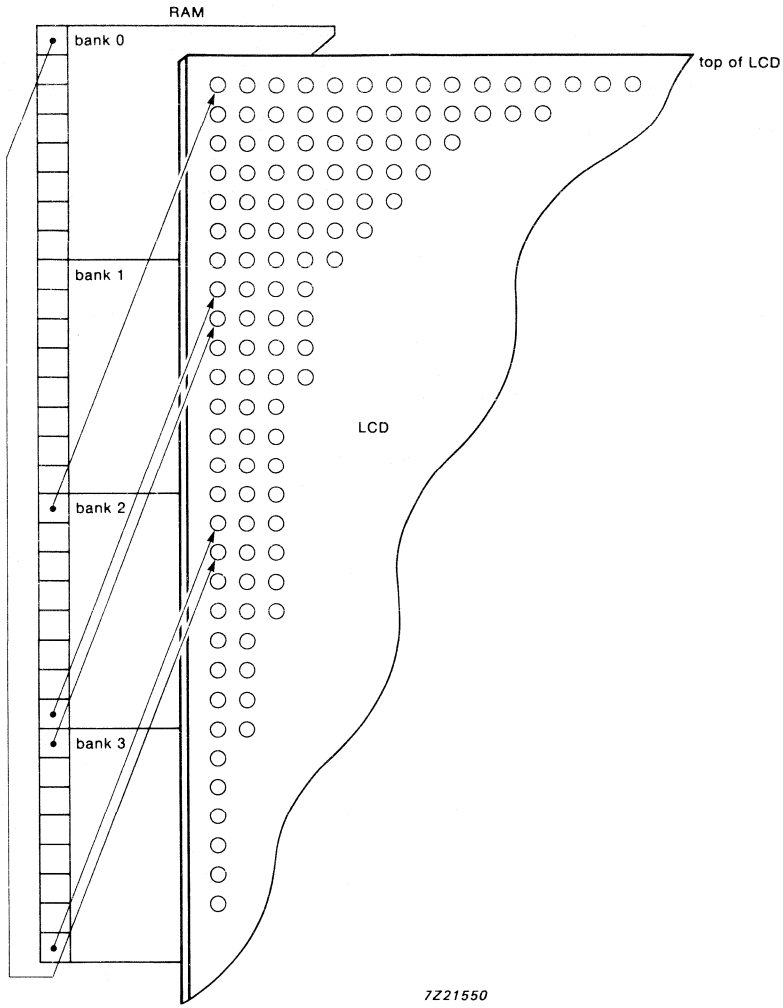


Fig.9 Relationship between display and SET START BANK; 1:32 multiplex rate and start bank = 2.

I²C-BUS PROTOCOL

Two 7-bit slave addresses (0111100 and 0111101) are reserved for both the PCF8578 and PCF8579. The least-significant bit of the slave address is set by connecting input SA0 to either 0 (V_{SS}) or 1 (V_{DD}). Therefore, two types of PCF8578 or PCF8579 can be distinguished on the same I²C-bus which allows:

(a) one PCF8578 to operate with up to 32 PCF8579s on the same I²C-bus for very large applications.
(b) the use of two types of LCD multiplex schemes on the same I²C-bus.

In most applications the PCF8578 will have the same slave address as the PCF8579.

The I²C-bus protocol is shown in Fig. 10. All communications are initiated with a start condition (S) from the I²C-bus master, which is followed by the desired slave address and read/write bit. All devices with this slave address acknowledge in parallel. All other devices ignore the bus transfer.

In WRITE mode (indicated by setting the read/write bit LOW) one or more commands follow the slave address acknowledgement. The commands are also acknowledged by all addressed devices on the bus. The last command must clear the continuation bit C. After the last command a series of data bytes may follow. The acknowledgement after each byte is made only by the (A0, A1, A2 and A3) addressed PCF8579 or PCF8578 with its implicit subaddress 0. After the last data byte has been acknowledged, the I²C-bus master issues a stop condition (P).

In READ mode, indicated by setting the read/write bit HIGH, data bytes may be read from the RAM following the slave address acknowledgement. After this acknowledgement the master transmitter becomes a master receiver and the PCF8579 becomes a slave transmitter. The master receiver must acknowledge the reception of each byte in turn. The master receiver must signal an end of data to the slave transmitter, by **not** generating an acknowledge on the last byte clocked out of the slave. The slave transmitter then leaves the data line HIGH, enabling the master to generate a stop condition (P).

Display bytes are written into, or read from, the RAM at the address specified by the data pointer and subaddress counter. Both the data pointer and subaddress counter are automatically incremented, enabling a stream of data to be transferred either to, or from, the intended devices.

In multiple device applications, the hardware subaddress pins of the PCF8579s (A0, A1, A2 and A3) are connected to V_{SS} or V_{DD} to represent the desired hardware subaddress code. If two or more devices share the same slave address, then each device **must** be allocated with an unique hardware subaddress.

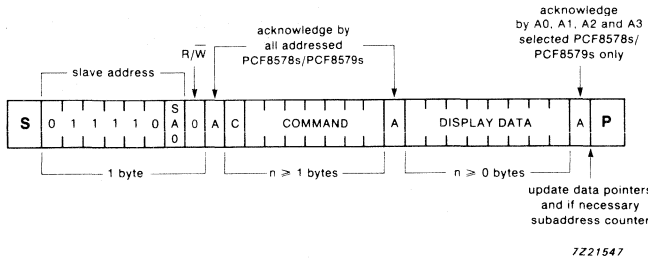


Fig.10(a) Master transmits to slave receiver (WRITE mode).

DEVELOPMENT DATA

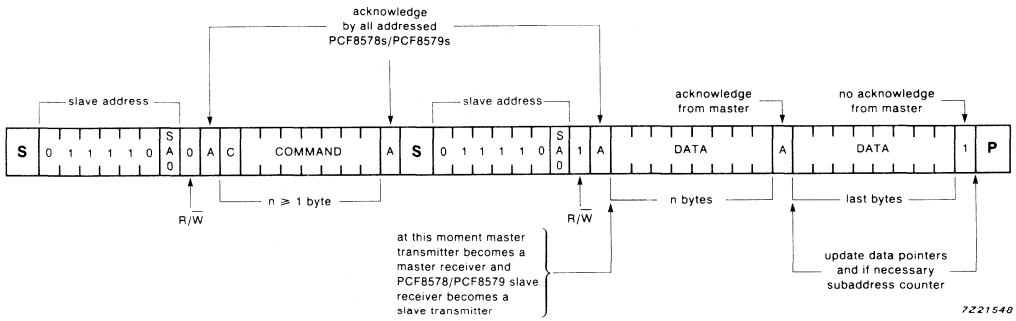


Fig.10(b) Master reads after sending command string (WRITE commands; READ data).

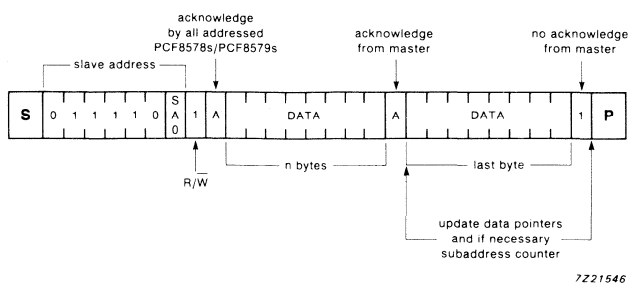
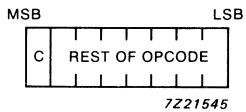


Fig.10(c) Master reads-slave immediately after sending slave address (READ mode).

I²C-BUS PROTOCOL (continued)

Command decoder

The command decoder indentifies command bytes that arrive on the I²C-bus. The most-significant bit of a command is the continuation bit C (see Fig.11). When this bit is set, it indicates that the next byte to be transferred will be a command. If the bit is reset, it indicates the conclusion of the command transfer. Further bytes will be regarded as display data. Commands are transferred in WRITE mode only.



C = 0; last command
C = 1; commands continue

Fig.11 General format of command byte.

The five commands available to the PCF8579 are defined in Table 2.

Table 2 Summary of commands

code	command	description
C 0 D D D D D D	LOAD X-ADDRESS	0 to 39
C 1 0 D D D D D	SET MODE	multiplex rate, display status, system type
C 1 1 0 D D D D	DEVICE SELECT	defines device subaddress
C 1 1 1 D D D D	RAM ACCESS	graphic modes, bank select (D D D D $\geqslant$ 12 is not allowed; see SET START BANK opcode)
C 1 1 1 1 1 D D	SET START BANK	defines bank at top of LCD

Where:

C = command continuation bit
D = may be a logic 1 or 0.

Table 3 Definition of PCF8578/PCF8579 commands

command / opcode	options	description
SET MODE C 1 0 T E1 E0 M1 M0	LCD drive mode bits M1 M0 1:8 MUX (8 rows) 0 1 1:16 MUX (16 rows) 1 0 1:24 MUX (24 rows) 1 1 1:32 MUX (32 rows) 0 0	defines LCD drive mode
	display status bits E1 E0 blank 0 0 normal 0 1 all segments on 1 0 inverse video 1 1	defines display status
	system type bit T PCF8578 row only 0 PCF8578 mixed mode 1	defines system type
SET START BANK C 1 1 1 1 1 B1 B0	start bank pointer bits B1 B0 bank 0 0 0 bank 1 0 1 bank 2 1 0 bank 3 1 1	defines pointer to RAM bank corresponding to the top of the LCD. Useful for scrolling, pseudo-motion and background preparation of new display
DEVICE SELECT C 1 1 0 A3 A2 A1 A0	bits A3 A2 A1 A0 4-bit binary value of 0 to 15	four bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of sixteen hardware subaddresses

DEVELOPMENT DATA

I²C BUS PROTOCOL (continued)

Table 3 (continued)

command / opcode	options	description
RAM ACCESS C 1 1 1 G1 G0 Y1 Y0	RAM access mode bits G1 G0 character 0 0 half graphic 0 1 full graphic 1 0 not allowed* 1 1	defines the auto-increment behaviour of the address for RAM access
	bits Y1 Y0 2-bit binary value of 0 to 3	two bits of immediate data, bits Y0 to Y1, are transferred to the Y-address pointer to define one of four banks for RAM access
LOAD X-ADDRESS C 0 X5 X4 X3 X2 X1 X0	bits X5 X4 X3 X2 X1 X0 6-bit binary value of 0 to 39	six bits of immediate data, bits X0 to X5, are transferred to the X-address pointer to define one of forty display RAM columns

* See opcode for SET START BANK.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

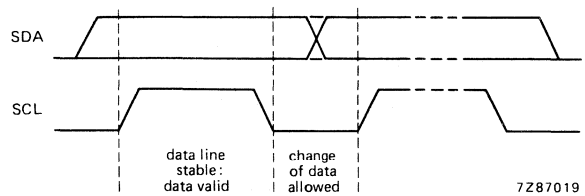


Fig.12 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

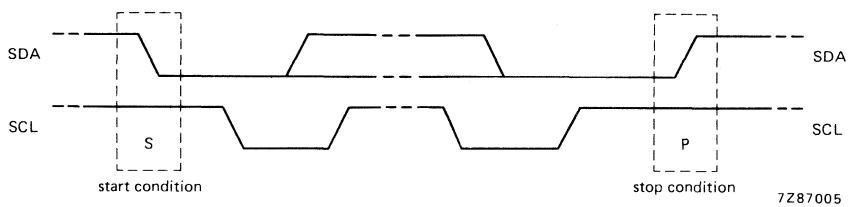


Fig.13 Definition of start and stop condition.

CHARACTERISTICS OF THE I²C-BUS (continued)

System configuration

A device transmitting a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message flow is the "master" and the devices which are controlled by the master are the "slaves".

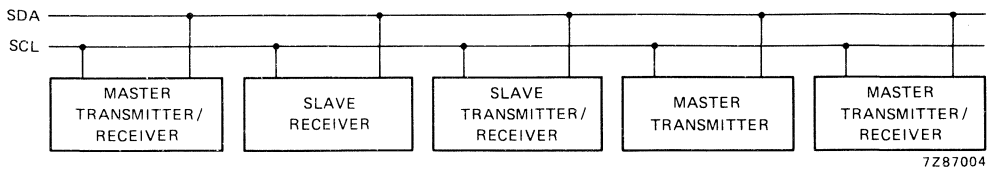


Fig.14 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal the end of a data transmission to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

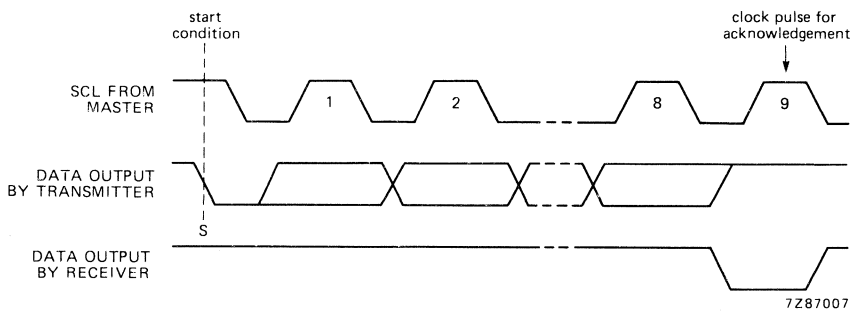


Fig.15 Acknowledgement on the I²C-bus.

Note

The general characteristics and detailed specification of the I²C-bus is available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	+8.0	V
LCD supply voltage range	V_{LCD}	V_{DD} −11	V_{DD}	V
Input voltage range at				
SDA, SCL, $\overline{SYNC}$, CLK, TEST, SA0, A0, A1, A2 and A3	V_{I1}	V_{SS} −0.5	V_{DD} + 0.5	V
V_3 to V_4	V_{I2}	V_{LCD} −0.5	V_{DD} + 0.5	V
Output voltage range at				
SDA	V_{O1}	V_{SS} −0.5	V_{DD} + 0.5	V
C0 to C39	V_{O2}	V_{LCD} −0.5	V_{DD} + 0.5	V
DC input current	I_I	−10	10	mA
DC output current	I_O	−10	10	mA
V_{DD}, V_{SS} or V_{LCD} current	I_{DD}, I_{SS}, I_{LCD}	−50	50	mA
Power dissipation per package	P_{tot}	−	400	mW
Power dissipation per output	P_o	−	100	mW
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{DD} = 2.5 V to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
LCD supply voltage		V_{LCD}	V_{DD} −9	–	V_{DD} −3.5	V
Supply current	note 1; f_{CLK} = 2 kHz	I_{DD1}	–	9	20	μA
Power-on reset level	note 2	V_{POR}	–	1.3	1.8	V
Logic						
Input voltage LOW		V_{IL}	V_{SS}	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Leakage current at SDA, SCL, $\overline{SYNC}$, CLK, TEST, SA0, A0, A1, A2 and A3	V_I = V_{DD} or V_{SS}	I_{L1}	−1	–	1	μA
SDA output current LOW	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL}	3	–	–	mA
Input capacitance	note 3	C_I	–	–	5	pF
LCD outputs						
Leakage current at V_3 to V_4	V_I = V_{DD} or V_{LCD}	I_{L2}	−2	–	2	μA
DC component of LCD drivers C0 to C39		± V_{DC}	–	20	–	mV
Output resistance at C0 to C39	note 4	R_{COL}	–	3	6	kΩ

AC CHARACTERISTICS (note 5)

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9 V; T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Clock frequency	50% duty factor	f_{CLK}	–	*	10	kHz
Driver delays	$V_{DD} - V_{LCD}$ = 9 V; with test loads	t_{PLCD}	–	–	100	μs
I²C-bus						
SCL clock frequency		f_{SCL}	–	–	100	kHz
Tolerable spike width on bus		t_{SW}	–	–	100	ns
Bus free time		t_{BUF}	4.7	–	–	μs
Start condition set-up time	repeated start codes only	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time		$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time		t_{LOW}	4.7	–	–	μs
SCL HIGH time		t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time		t_r	–	–	1.0	μs
SCL and SDA fall time		t_f	–	–	0.3	μs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Data hold time		$t_{HD;DAT}$	0	–	–	ns
Stop condition set-up time		$t_{SU;STO}$	4.0	–	–	μs

DEVELOPMENT DATA

* Typically 0.9 to 3.3 kHz.

Notes to the characteristics

1. Outputs are open; inputs at V_{DD} or V_{SS}; I^2C-bus inactive; clock with 50% duty cycle.
2. Resets all logic when $V_{DD} < V_{POR}$.
3. Periodically sampled; not 100% tested.
4. Resistance measured between output terminal (C0 to C39) and bias input (V_3 to V_4, V_{DD} and V_{LCD}) when the specified current flows through one output under the following conditions (see Table 1):

   $V_{OP} = V_{DD} - V_{LCD} = 9$ V;

   $V_3 - V_{LCD} \geqslant 4.70$ V; $V_4 - V_{LCD} \leqslant 4.30$ V; $I_{LOAD} = 100\ \mu$A.
5. All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

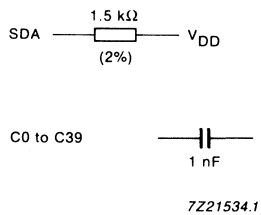


Fig.16 Test loads.

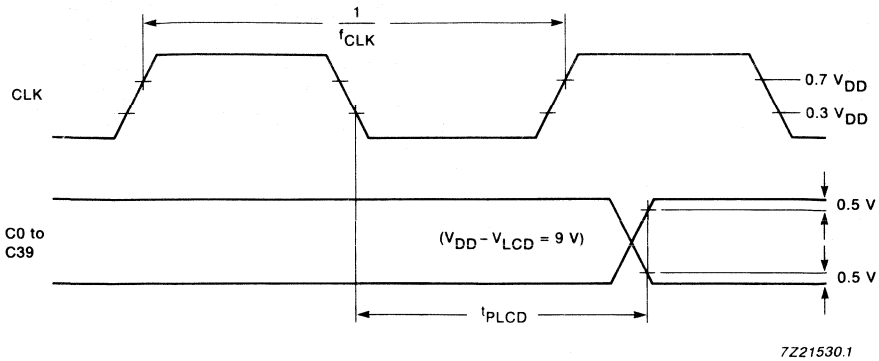


Fig.17 Driver timing waveforms.

DEVELOPMENT DATA

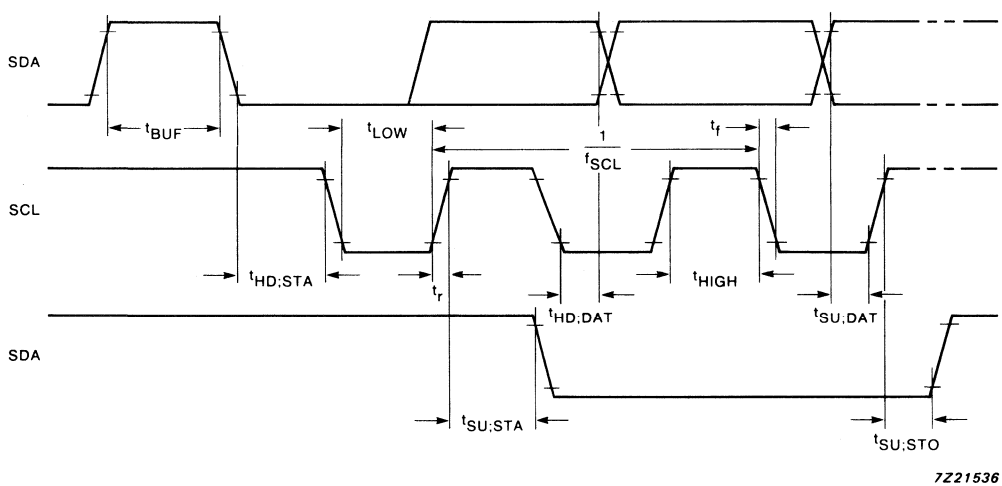


Fig.18 I^2C-bus timing waveforms.

APPLICATION INFORMATION

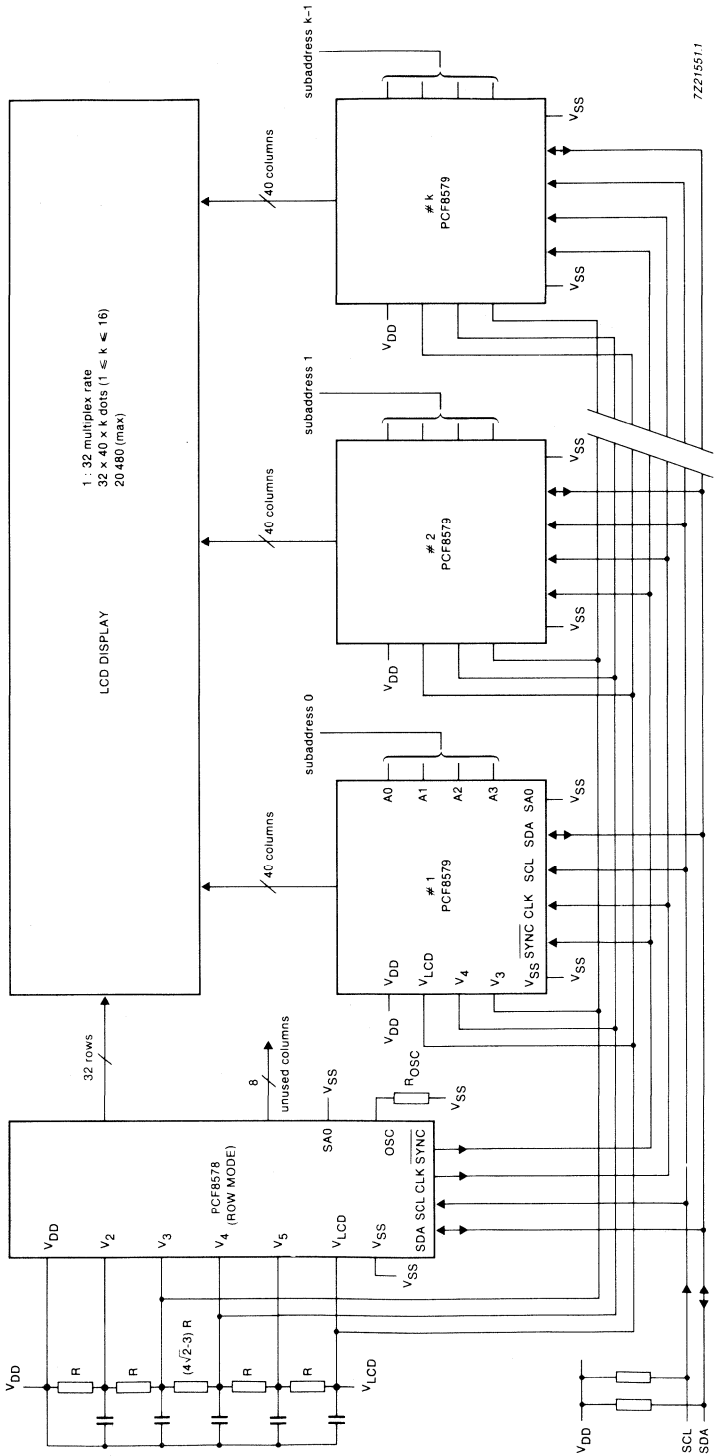


Fig.19 Typical LCD driver system with 1:32 multiplex rate.

DEVELOPMENT DATA

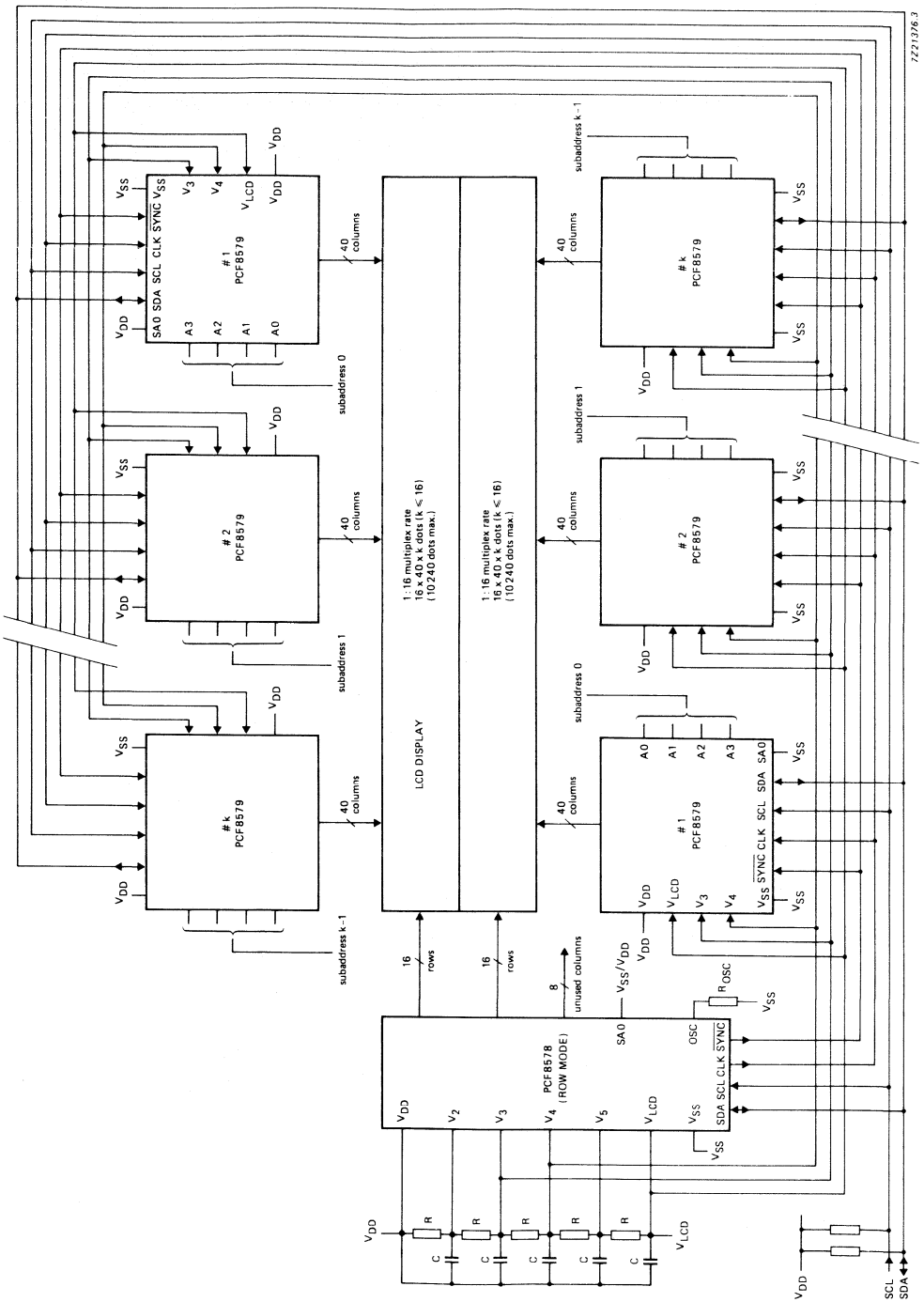


Fig.20 Split screen application with 1:16 multiplex rate for improved contrast.

APPLICATION INFORMATION (continued)

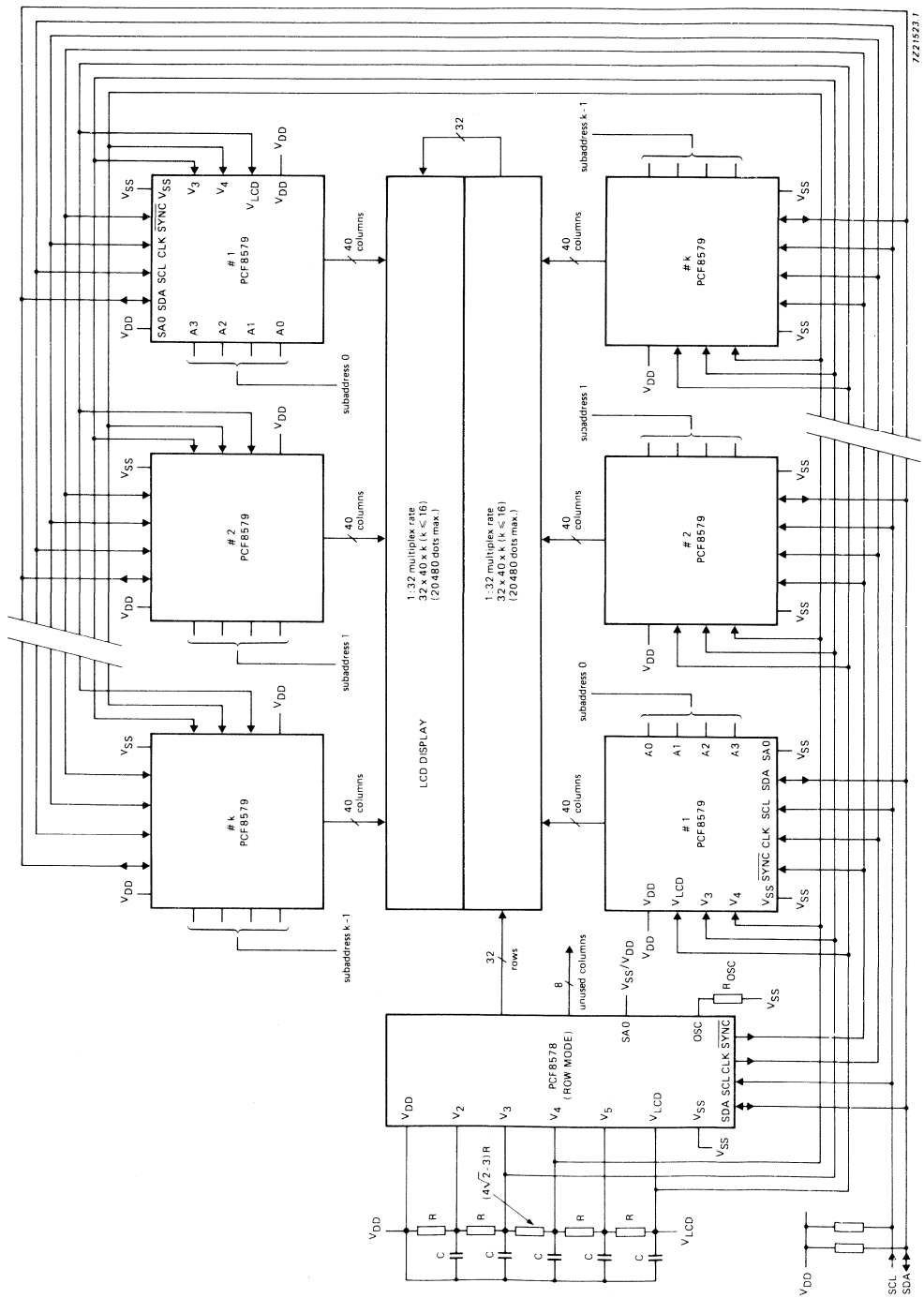


Fig.21 Split screen application using double screen with 1:32 multiplex rate.

DEVELOPMENT DATA

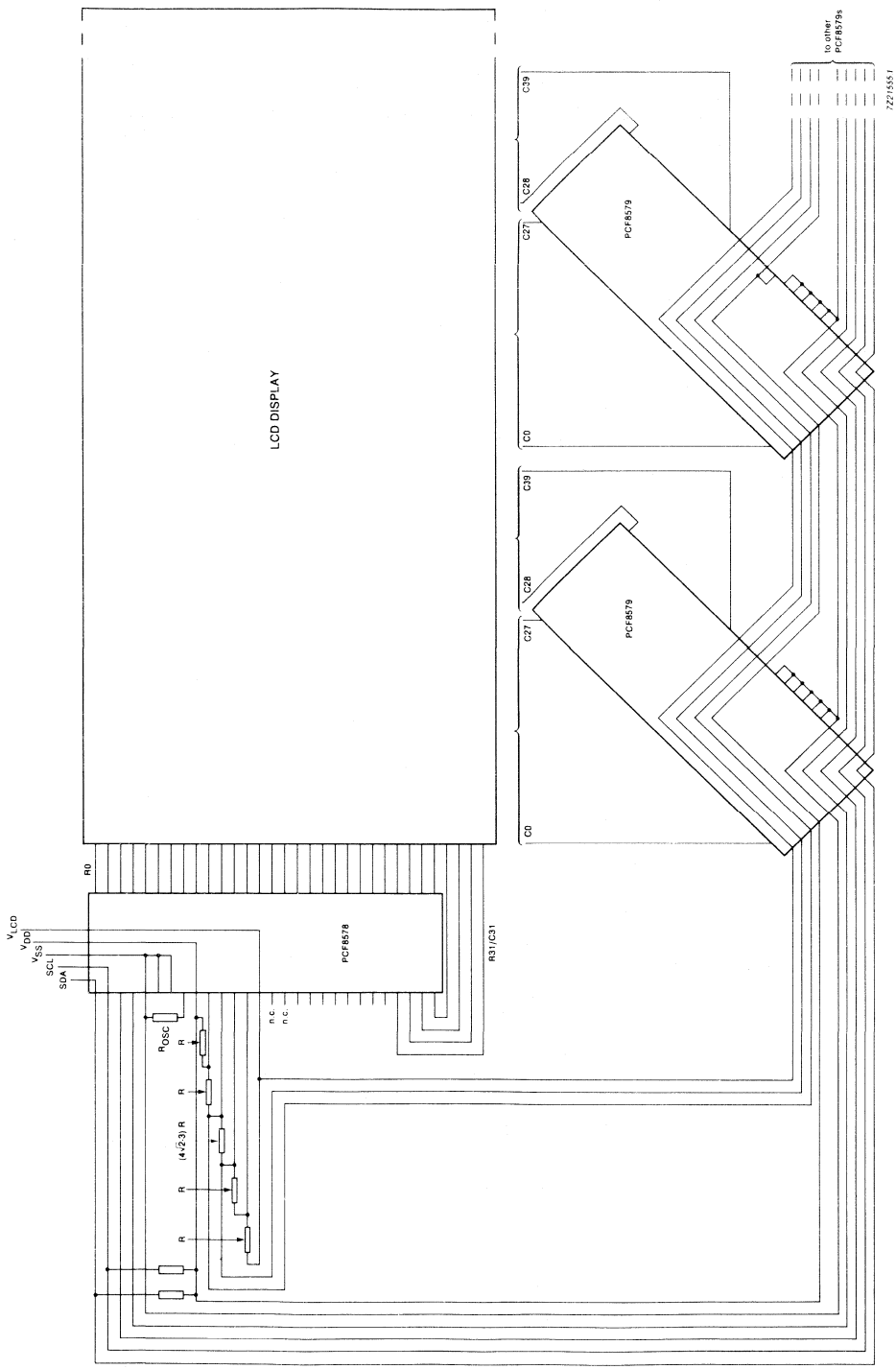
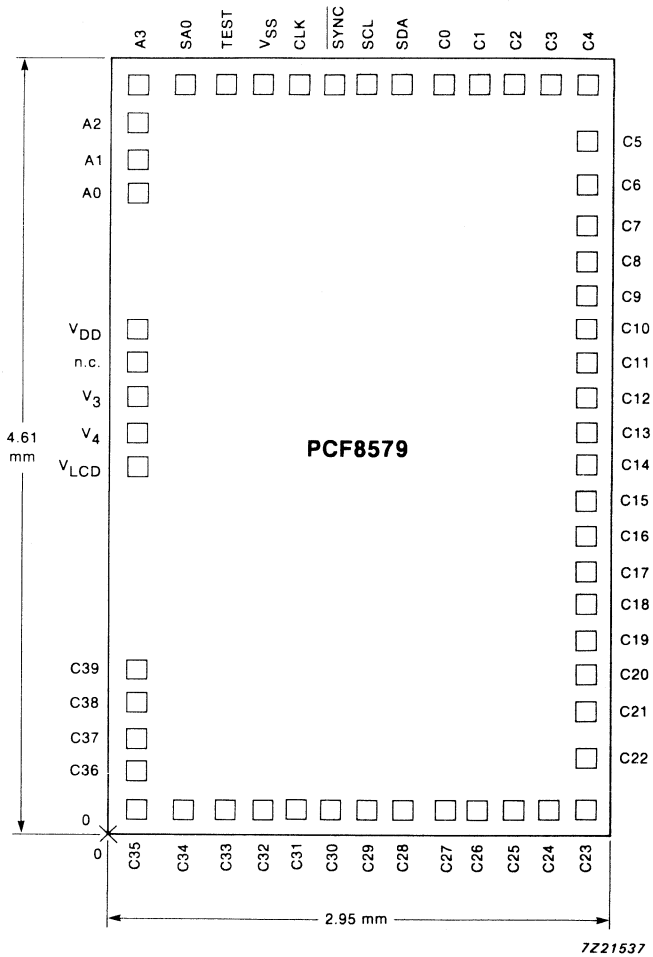


Fig.22 Example of single plane wiring, single screen with 1:32 multiplex rate (PCF8578 in row driver mode).

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 13.6 mm^2
Bonding pad dimensions: 120 μm x 120 μm

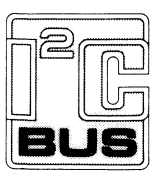
Fig.23 Bonding pad locations.

Table 4 Bonding pad locations (dimensions in μm)

All x/y co-ordinates are referenced to the bottom left corner, see Fig.23.

pad	X	Y	pad	X	Y
SDA	1726	4444	C27	1972	160
SCL	1522	4444	C26	2176	160
$\overline{SYNC}$	1318	4444	C25	2380	160
CLK	1114	4444	C24	2584	160
V_{SS}	910	4444	C23	2788	160
TEST	688	4444	C22	2788	472
SA0	442	4444	C21	2788	736
A3	160	4444	C20	2788	976
A2	160	4222	C19	2788	1180
A1	160	4018	C18	2788	1384
A0	160	3814	C17	2788	1588
V_{DD}	160	3010	C16	2788	1792
n.c.	160	2806	C15	2788	1996
V_2	160	2602	C14	2788	2200
V_3	160	2398	C13	2788	2404
V_{LCD}	160	2194	C12	2788	2608
C39	160	994	C11	2788	2812
C38	160	790	C10	2788	3016
C37	160	586	C9	2788	3220
C36	160	382	C8	2788	3424
C35	160	160	C7	2788	3628
C34	442	160	C6	2788	3868
C33	688	160	C5	2788	4132
C32	910	160	C4	2788	4444
C31	1114	160	C3	2584	4444
C30	1318	160	C2	2380	4444
C29	1522	160	C1	2176	4444
C28	1726	160	C0	1972	4444

DEVELOPMENT DATA



CHIP-ON GLASS INFORMATION

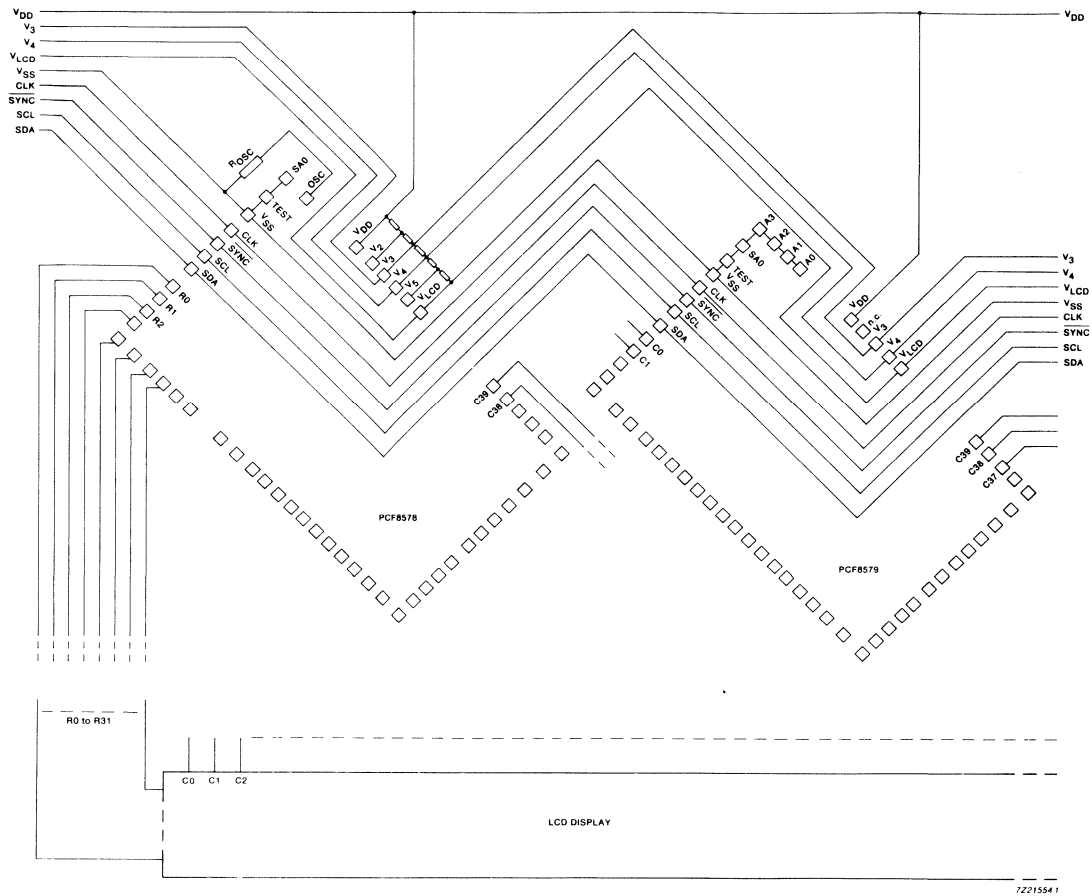


Fig.24 Typical chip-on glass application (viewed from underside of chip).

Note to Fig.24

If inputs SA0 and A0 to A3 are left unconnected they are internally pulled-up to V_{DD}.

18-ELEMENT BAR GRAPH LCD DRIVER

GENERAL DESCRIPTION

The PCF1303T is an 18-element bar graph LCD driver with linear relation to control voltage (V_c) when in pointer or thermometer mode.

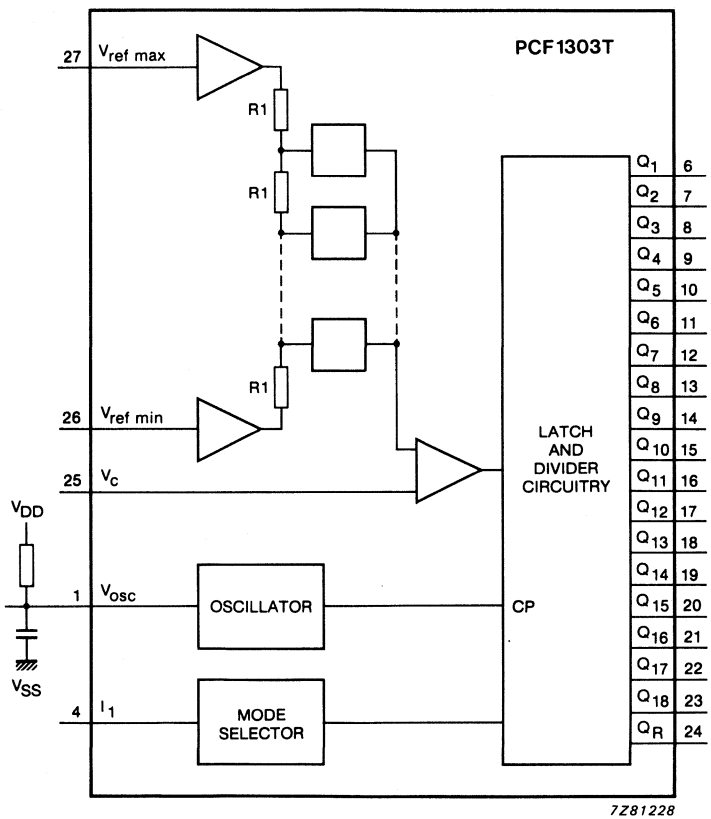
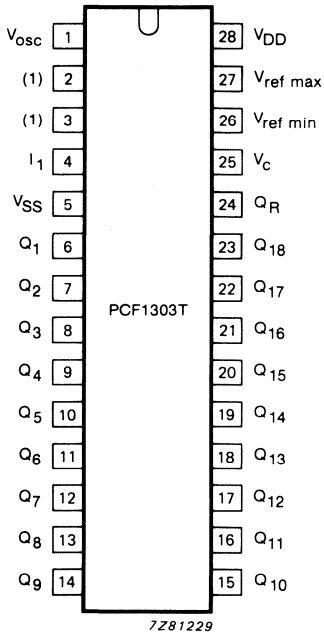


Fig. 1 Block diagram.

PACKAGE OUTLINE

PCF1303T: 28-lead mini-pack; plastic (SO28; SOT136A).



(1) Pins 2 and 3 should be connected to V_{SS}.

Fig. 2 Pin configuration.

PIN DESCRIPTION

pin no.	symbol	name and function
1	V_{osc}	oscillator pin
4	I_1	mode select input
5	V_{SS}	ground (0 V)
6 to 23	Q_1 to Q_{18}	segment outputs
24	Q_R	back-plane output
25	V_c	control voltage
26 27	$V_{ref\ min}$ $V_{ref\ max}$	reference voltage inputs
28	V_{DD}	positive supply voltage

FUNCTION TABLE

I_1	mode
L	pointer
H	thermometer

H = HIGH voltage level
L = LOW voltage level

FUNCTIONAL DESCRIPTION

The PCF1303T is an 18-element bar graph LCD driver with linear relation to the control voltage when in pointer or thermometer mode.

The first segment will energize when the control voltage is less than the trigger voltage ($V_{T(bar)2}$ see equation [3]).

The circuit has analogue and digital sections.

The analogue section consists of a comparator with the inverting input coupled to the input control voltage. The non-inverting input of the comparator is connected via 17 analogue switches to the nodes of an 18-element resistor divider. The extremities of the resistor divider are coupled via high-input impedance amplifiers to the maximum reference voltage input and the minimum reference voltage input.

The control input functions with Schmitt trigger action.

The digital section has one reference output (Q_R) to drive the back-plane and 18 outputs (Q_1 to Q_{18}) to drive the segments.

The segment outputs incorporate two latches and some gates.

The circuit is driven by an on-chip oscillator with external resistors and capacitors. The outputs are driven at typical 100 Hz.

LINEARITY

$$V_{step} = V_{step'} \pm \Delta V_{step} \qquad [1]$$

$V_{step'}$ is the voltage drop (internal) across the resistor-ladder network.
ΔV_{step} is the differential on V_{step}.

$$V_{step'} = \frac{(V_{ref\,max} \pm \Delta V_{2'}) - (V_{ref\,min} \pm \Delta V_2)}{18} \qquad [2]$$

ΔV_2 and $\Delta V_{2'}$ are the maximum offset voltage spread of the on-chip voltage followers.

ABSOLUTE VOLTAGE TRIGGER LEVEL

The absolute voltage trigger level at the V_c pin is $V_{T(bar)n}$;

$$V_{T(bar)n} = (V_{ref\,min} \pm \Delta V_{2}{}^{*}) + \{(n-1)V_{step'} \pm \Delta V_R\} \pm \Delta V_1 \pm V_H \qquad [3]$$

n = number of segments; $2 \leqslant n \leqslant 18$.

ΔV_R is the voltage deviation at step n of the resistor-ladder network (for n = 2 or 18, $\Delta V_R = \Delta V_{step}$).

ΔV_1 is the offset voltage for the on-chip comparator.

V_H is the hysteresis voltage: $30\%\ V_{step} \geqslant V_H \geqslant 10\%\ V_{step}$.

* For ΔV_2 the same sign (+ or −) should be used as in equation [2].

RATINGS

Limiting values as in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,5 to + 15	V
Voltage on any input	V_I	−0,5 to V_{DD} + 0,5	V
D.C. current into any input or output	$\pm I_I$	max. 10	mA
Storage temperature range	T_{stg}	−25 to + 125	°C
Operating ambient temperature range	T_{amb}	−40 to + 85	°C

D.C. CHARACTERISTICS

V_{SS} = 0 V

parameter	V_{DD} V	symbol	T_{amb} (°C)							unit	notes
			−40		+ 25			+ 85			
			min.	max.	min.	typ.	max.	min.	max.		
Quiescent device current	10,0	I_{DD}		1200			1200		1200	µA	1
Operating supply current	8,2	I_{DD}		2,0			2,0		2,0	mA	2
Input leakage current	6,0 8,2 10,0	$\pm I_I$ $\pm I_I$ $\pm I_I$		300 300 300			300 300 300		1000 1000 1000	nA nA nA	3
HIGH level input voltage select input I_1	6,0 8,2 10,0	V_{IH} V_{IH} V_{IH}	4,2 5,8 7,0		4,2 5,8 7,0			4,2 5,8 7,0		V V V	
LOW level input voltage select input I_1	6,0 8,2 10,0	V_{IL} V_{IL} V_{IL}		1,8 2,4 3,0	2,4		1,8 2,4 3,0		1,8 3,0	V V V	
HIGH level output voltage	6,0 8,2 10,0	V_{OH} V_{OH} V_{OH}	5,95 8,15 9,95		5,95 8,15 9,95			5,95 8,15 9,95		V V V	4
LOW level output voltage	6,0 8,2 10,0	V_{OL} V_{OL} V_{OL}		0,05 0,05 0,05			0,05 0,05 0,05		0,05 0,05 0,05	V V V	4
Output current HIGH	6,0 8,2 10,0	$-I_{OH}$ $-I_{OH}$ $-I_{OH}$	0,6 0,85 1,0		0,5 0,7 0,85			0,35 0,45 0,6		mA mA mA	5
Output current LOW	6,0 8,2 10,0	I_{OL} I_{OL} I_{OL}	0,65 1,0 1,3		0,5 0,8 1,0			0,4 0,6 0,8		mA mA mA	6

For notes see page 6.

parameter	V_{DD} V	symbol	T_{amb} (°C)							unit	notes
			−40		+ 25			+ 85			
			min.	max.	min.	typ.	max.	min.	max.		
Input voltage control input V_c	6,0	V_{IC}	0,0	6,0	0,0		6,0	0,0	6,0	V	
	8,2	V_{IC}	0,0	8,2	0,0		8,2	0,0	8,2	V	
	10,0	V_{IC}	0,0	10,0	0,0		10,0	0,0	10,0	V	
Input voltage $V_{ref\,max}$ input	6,0	$V_{IR\,max}$	3,6	5,5	3,6		5,5	3,6	5,5	V	
	8,2	$V_{IR\,max}$	3,6	7,7	3,6		7,7	3,6	7,7	V	
	10,0	$V_{IR\,max}$	3,6	9,5	3,6		9,5	3,6	9,5	V	
Input voltage $V_{ref\,min}$ input	6,0	$V_{IR\,min}$	0,5	1,0	0,5		1,0	0,5	1,0	V	
	8,2	$V_{IR\,min}$	0,5	4,5	0,5		4,5	0,5	4,5	V	
	10,0	$V_{IR\,min}$	0,5	6,0	0,5		6,0	0,5	6,0	V	
$V_{ref\,max} - V_{ref\,min}$	6,0	ΔV_I	3,0		3,0			3,0		V	
	8,2	ΔV_I	3,0		3,0			3,0		V	
	10,0	ΔV_I	3,0		3,0			3,0		V	
DC component bar output to back-plane output	8,2	$\pm V_{BP}$		25		10	25		25	mV	7
Back-plane frequency	8,2	f_{BP}	90	110		100		90	110	Hz	8
Input offset voltage	8,2	$\pm V_{IO}$		120			120		120	mV	9
Step voltage variation	8,2	$\pm \Delta V_{step}$		50			50		50	mV	10
Input voltage slew rate V_c input	6,0	SR		50			50		50	V/s	11
	8,2	SR		50			50		50	V/s	
	10,0	SR		50			50		50	V/s	

For notes see next page.

Notes to D.C. characteristics

1. $V_{ref\,min}$ = 0,5 V, $V_{ref\,max}$ = 9,5 V, $V_c = V_{osc}$ = 0 V, I_1 at V_{SS} or V_{DD}.
2. See Fig. 2.
3. Pin under test at V_{SS} or V_{DD}. All other inputs simultaneously at V_{SS} or V_{DD}.
4. I_O = 0, all inputs at V_{SS} or V_{DD}.
5. $V_{OH} = V_{DD} - 0{,}5$ V, all inputs at V_{SS} or V_{DD}.
6. V_{OL} = 0,4 V, all inputs at V_{SS} or V_{DD}.
7. f_{BP} = 100 Hz, load segment outputs to back-plane output.
   $C_1 - C_{18} \leqslant 0{,}01\ \mu F$, $C_{BP} = C_1 + C_2 + \ldots C_{18} \leqslant 0{,}05\ \mu F$, $R_1 - R_{18} \geqslant 2\ M\Omega$.
8. R_{osc} = 0,1 MΩ, C_{osc} = 390 pF.
9. Number of segments 2 or 18.
   For n = 2:

$$V_{IO} = V_c - V_{ref\,min} - \frac{(V_{ref\,max}) - (V_{ref\,min})}{18} \pm V_H$$

   For n = 18:

$$V_{IO} = V_c - V_{ref\,max} + \frac{(V_{ref\,max}) - (V_{ref\,min})}{18} \pm V_H$$

10. See equation [1].
11. Condition applies with clock oscillator such that f_{BP} = 100 Hz.

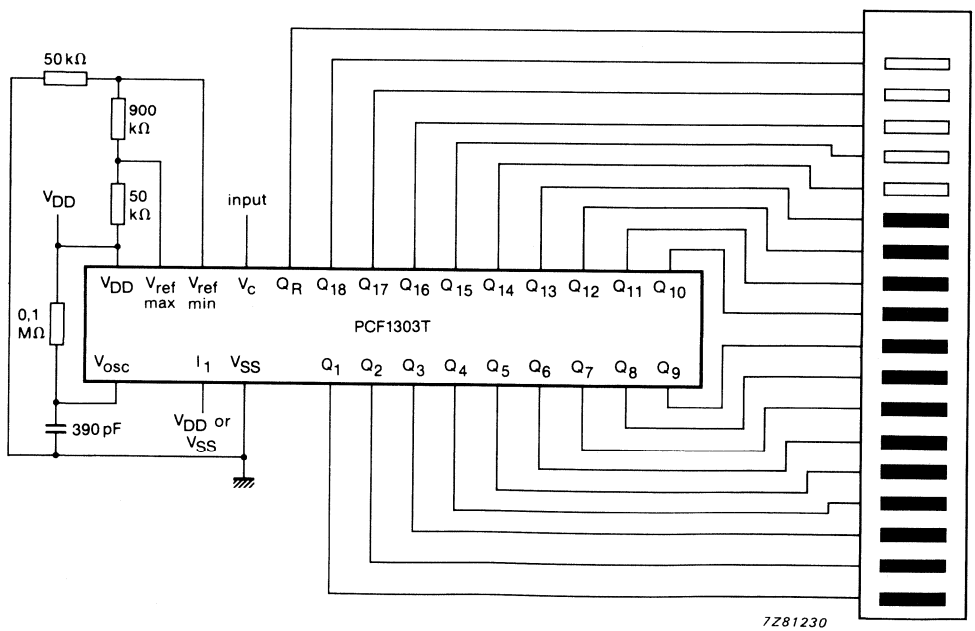


Fig. 3 Typical application.

18-ELEMENT BAR GRAPH LCD DRIVER

The HEF4754V drives an 18-element bar graph LCD in linear relation to the control voltage (V_c) in a pointer or thermometer mode.

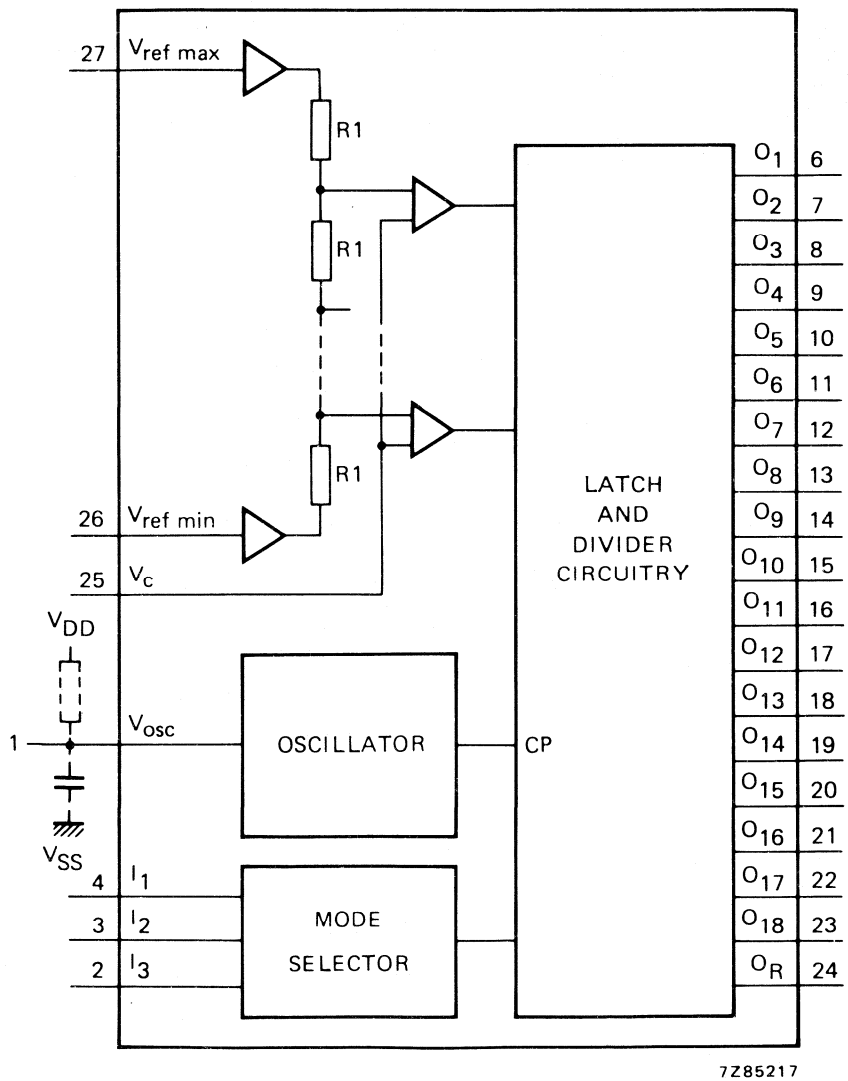


Fig. 1 Functional diagram.

FAMILY DATA see Family Specifications

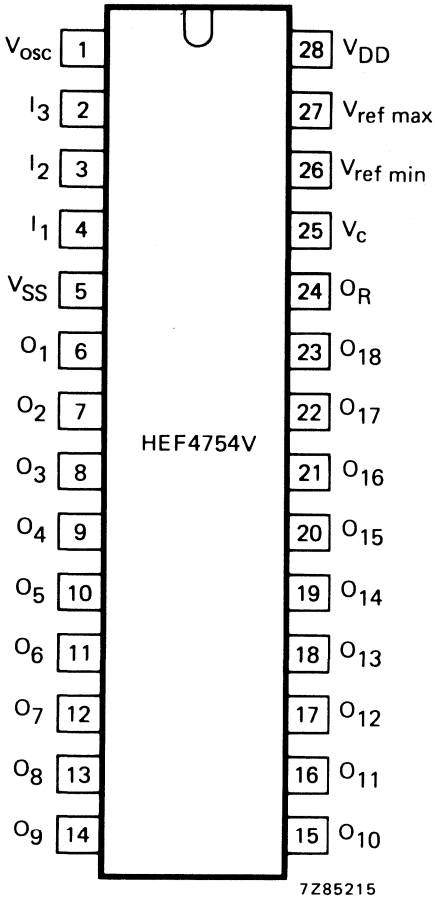


Fig. 2 Pinning diagram.

PINNING

V_{osc}	oscillator terminal
V_c	control voltage input
$V_{ref\ min}$, $V_{ref\ max}$	reference voltage inputs
I_1	thermometer/pointer (choice select input)
I_2	peak value; reset/9 or 18 bars (choice select input)
I_3	reset; repetitively reset (choice select input)
O_1 to O_{18}	bar outputs
O_R	back plate output

HEF4754VP : 28-lead DIL; plastic (SOT-117).
HEF4754VD: 28-lead DIL; ceramic (cerdip) SOT-135A).
HEF4754VT : 28-lead mini-pack; plastic (SO-28; SOT-136A).

FUNCTION TABLE

I_1	I_2	I_3	mode
L	L	X	pointer; 18 bars
L	H	X	pointer; 9 bars
H	L	X	thermometer; no peak value
H	H	L	thermometer; peak value, repetitively reset
H	H	H	thermometer; peak value, manually reset

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

GENERAL DESCRIPTION

The HEF4754V drives an 18-element bar graph LCD in linear relation to the control voltage (V_c) in a pointer or thermometer mode. The first bar lights up when V_c is smaller than $V_{T(bar)2}$ (see equation [3] below).

In the pointer mode, the circuit can drive 9 or 18 bars; in the thermometer mode, the circuit also drives the peak value indication. This can be reset or repetitively reset, after 1,5 to 2 seconds.

The circuit has analogue and digital parts. The analogue part consists of 17 comparators, with their non-inverting inputs connected together and coupled to the control input V_c. The inverting inputs of the comparators are connected in succession to the nodes of an 18-part resistor divider. The distance between the switching levels of the comparators is defined by the voltage difference across this divider. The extremities of the resistor divider are coupled via high-input amplifiers to the maximum reference voltage input and the minimum reference voltage input.

The digital part has one reference output (O_R) to drive the back plate, and 18 outputs (O_1 to O_{18}) to drive each bar. Three latches and some gates are incorporated for each bar output. An on-chip oscillator (1024 Hz) with external R and C drives the circuit. The outputs are driven at 64 Hz. The select inputs I_1 to I_3 are provided with an on-chip pull-up element, and they may therefore be left floating (equals HIGH state).

LINEARITY

V_{DD} = 10 V; $V_{ref\ max}$ = 9,5 V; $V_{ref\ min}$ = 0,5 V; T_{amb} = 25 °C

ΔV_1 = 250 mV (this is the tolerance of the step voltage).

$$V_{step} = V_{step}' + \Delta V_1 \qquad [1]$$

V_{step}' is the (internal) voltage drop across the resistor-ladder network.

$$V_{step}' = \frac{(V_{ref\ max} \pm \Delta V_2) - (V_{ref\ min} \pm \Delta V_2)}{18} \qquad [2]$$

ΔV_2 is the maximum offset voltage spread of the on-chip voltage follower.

ΔV_2 = 250 mV.

The linearity is guaranteed for $V_{DD} > 10$ V.
The monotony between V_{DD} = 5 V and 10 V is guaranteed. During ramping-up of the input voltage a maximum of two bars might be activated simultaneously.

ABSOLUTE VOLTAGE TRIGGER LEVEL

The absolute voltage trigger level at the V_c pin is $V_{T(bar)n}$;

$$V_{T(bar)n} = (V_{ref\ min} \pm \Delta V_2^*) + \{ (n-1)\ V_{step}' \pm \Delta V_1 \}, \text{ in which} \qquad [3]$$

n = number of bars; $2 \leqslant n \leqslant 18$.

For n = 1 (first bar) see text above.

* For ΔV_2 the same sign (+ or −) should be used as in equation [2].

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,5 to + 18	V
Voltage on any input	V_I	−0,5 to V_{DD} + 0,5	V
D.C. current into any input or output	$\pm I_I$	max. 10	mA
Storage temperature	T_{stg}	−25 to + 125	°C
Operating ambient temperature	T_{amb}	−20 to + 85	°C

NOTES (to D.C. CHARACTERISTICS)

1. $V_{ref\ min}$ = 0,5 V; $V_{ref\ max}$ = 9,5 V; $V_{osc} = V_c$ = 0 V; I_1, I_2 and I_3 at V_{DD}.
2. Pin under test at V_{SS} or V_{DD}, all other inputs simultaneously at V_{SS} or V_{DD}.
3. I_O = 0; all inputs at V_{SS} or V_{DD}.
4. At V_{DD} = 5 V: V_{OH} = 4,5 V.
   At V_{DD} = 10 V: V_{OH} = 9,5 V.
   At V_{DD} = 15 V: V_{OH} = 13,5 V.
5. At V_{DD} = 5 V: V_{OL} = 0,4 V; inputs at V_{SS} or V_{DD}.
   At V_{DD} = 10 V: V_{OL} = 0,5 V; inputs at V_{SS} or V_{DD}.
   At V_{DD} = 15 V: V_{OL} = 1,5 V; inputs at V_{SS} or V_{DD}.
6. $V_{ref\ min} + 4\ V < V_{ref\ max}$.

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	symbol	T_{amb} (°C)								notes
			−40		+ 25			+ 85			
			min.	max.	min.	typ.	max.	min.	max.		
Quiescent device current	5	I_{DD}	–	–	–	–	–	–	–	μA	
	10		–	–	–	–	1000	–	–	μA	1
	15		–	–	–	–	1600	–	–	μA	
Input leakage current (except select inputs)	5	$\pm I_{IN}$	–	–	–	–	100	–	–	nA	
	10		–	–	–	–	100	–	–	nA	2
	15		–	–	–	–	100	–	–	nA	
Input voltage HIGH select inputs	5	V_{IH}	3,5	–	3,5	–	–	3,5	–	V	
	10		7,0	–	7,0	–	–	7,0	–	V	
	15		11,0	–	11,0	–	–	11,0	–	V	
Input voltage LOW select inputs	5	V_{IL}	–	1,5	–	–	1,5	–	1,5	V	
	10		–	3,0	–	–	3,0	–	3,0	V	
	15		–	4,0	–	–	4,0	–	4,0	V	
Output voltage HIGH	5	V_{OH}	4,99	–	4,99	–	–	4,95	–	V	
	10		9,99	–	9,99	–	–	9,95	–	V	3
	15		–	–	14,99	–	–	–	–	V	
Output voltage LOW	5	V_{OL}	–	0,01	–	–	0,01	–	0,05	V	
	10		–	0,01	–	–	0,01	–	0,05	V	3
	15		–	0,01	–	–	0,01	–	0,05	V	
Output current HIGH	5	$-I_{OH}$	0,36	–	0,3	–	–	0,24	–	mA	
	10		0,80	–	0,7	–	–	0,56	–	mA	4
	15		3,0	–	2,8	–	–	2,60	–	mA	
Output current LOW	5	I_{OL}	0,34	–	0,3	–	–	0,24	–	mA	
	10		1,00	–	0,9	–	–	0,72	–	mA	5
	15		4,40	–	4,0	–	–	3,20	–	mA	
Input voltage control input V_c	5	V_{IC}	–	–	0	–	5	–	–	V	
	10		–	–	0	–	10	–	–	V	6
	15		–	–	0	–	15	–	–	V	
Max. input voltage $V_{ref\,max}$ input	5	V_{IRmax}	–	–	4,5	–	4,5	–	–	V	
	10		–	–	4,5	–	9,5	–	–	V	6
	15		–	–	4,5	–	14,5	–	–	V	
Min. input voltage $V_{ref\,min}$ input	5	V_{IRmin}	–	–	0,5	–	0,5	–	–	V	
	10		–	–	0,5	–	5,5	–	–	V	6
	15		–	–	0,5	–	10,5	–	–	V	
Operating supply current	10	I_{DD}	–	–	–	750	–	–	–	μA	Fig. 3

For notes see opposite page.

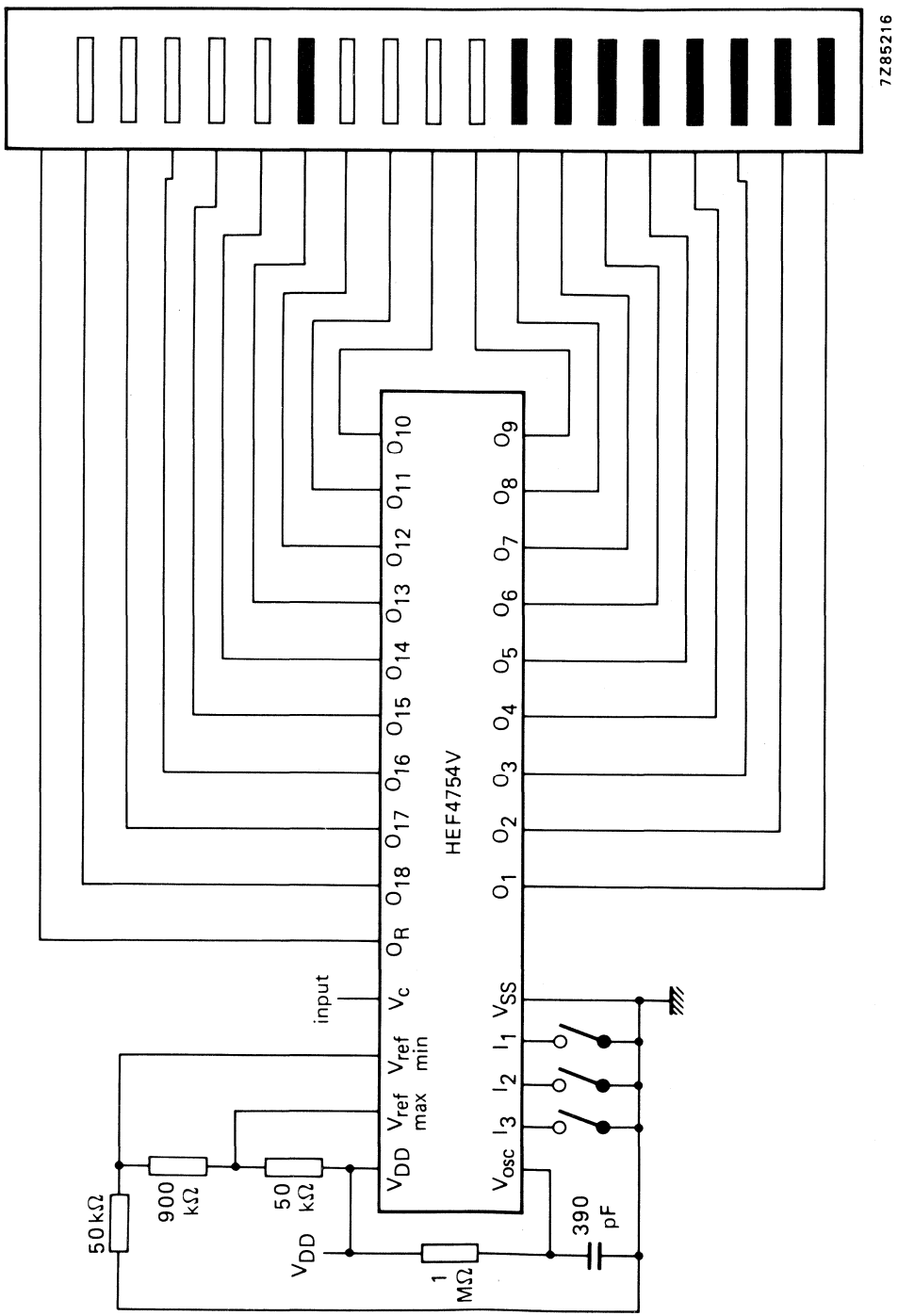


Fig. 3 Typical operating set-up.

BCD TO 7-SEGMENT LATCH/DECODER/DRIVER FOR LCDs

FEATURES

- Latch storage of BCD inputs
- Blanking inputs
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4543 are high-speed Si-gate CMOS devices and are pin compatible with "4543" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4543 are BCD to 7-segment latch/decoder/drivers for liquid crystal displays. They have four address inputs (D_0 to D_3), an active HIGH latch disable input (LD), an active HIGH blanking input (BI), an active HIGH phase input (PH) and seven buffered segment outputs (Q_a to Q_g).

The "4543" provides the function of a 4-bit storage latch and an 8-4-2-1 BCD to 7-segment decoder driver. The "4543" can invert the logic levels of the output combination. The phase (PH), blanking (BI) and latch disable (LD) inputs are used to reverse the function table phase, blank the display and store a BCD code, respectively.

For liquid crystal displays a square-wave is applied to PH and the electrical common back-plane of the display. The outputs of the "4543" are directly connected to the segments of the liquid crystal.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n LD to Q_n BI to Q_n	C_L = 15 pF V_{CC} = 5 V	29 32 20	33 31 28	ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	42	42	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4543P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT4543T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	LD	latch disable input (active HIGH)
5, 3, 2, 4	D_0 to D_3	address (data) inputs
6	PH	phase input (active HIGH)
7	BI	blanking input (active HIGH)
8	GND	ground (0 V)
9, 10, 11, 12 13, 15, 14	Q_a to Q_g	segment outputs
16	V_{CC}	positive supply voltage

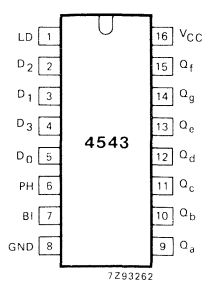


Fig. 1 Pin configuration.

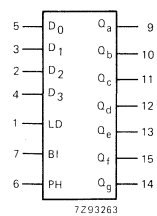


Fig. 2 Logic symbol.

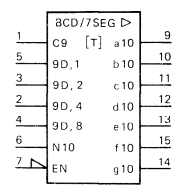


Fig. 3 IEC logic symbol.

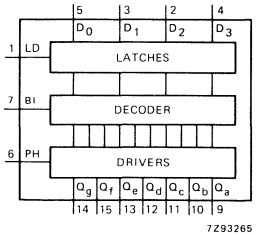


Fig. 4 Functional diagram.

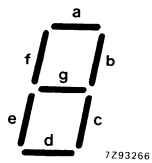


Fig. 5 Segment designation.

APPLICATIONS

- Driving LCD displays
- Driving fluorescent displays
- Driving incandescent displays
- Driving gas discharge displays

FUNCTION TABLE

INPUTS							OUTPUTS							DISPLAY
LD	BI	PH*	D_3	D_2	D_1	D_0	Q_a	Q_b	Q_c	Q_d	Q_e	Q_f	Q_g	
X	H	L	X	X	X	X	L	L	L	L	L	L	L	blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	blank
L	L	L	X	X	X	X				**				**
as above		H	as above				inverse of above							as above

* For liquid crystal displays, apply a square-wave to PH.

** Depends upon the BCD-code previously applied when LD = HIGH.

H = HIGH voltage level
L = LOW voltage level
X = don't care

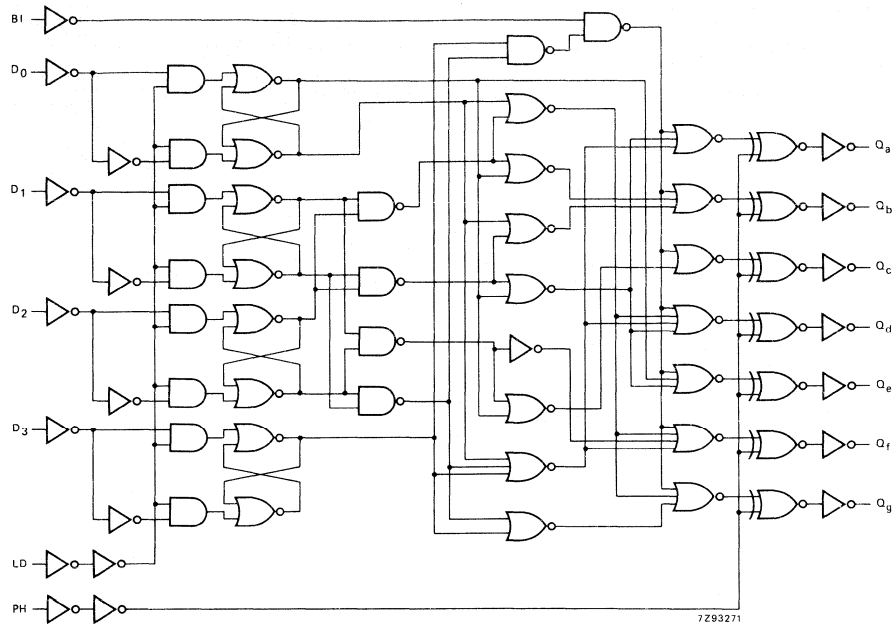


Fig. 6 Logic diagram.

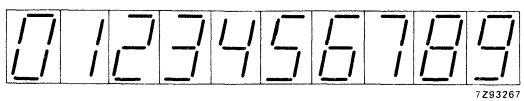


Fig. 7 Display.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
For RATINGS see chapter "HCMOS family characteristics", section "Family specifications", standard outputs.

DC CHARACTERISTICS FOR 74HC

Output capability: non-standard
I_{CC} category: MSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.2 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.8	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98 5.48	0.15 0.16		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 1.0 mA $-I_O$ = 1.3 mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 1.0 mA I_O = 1.3 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	I_O = 0

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		91 33 26	340 68 58		425 85 72		510 102 87	ns	2.0 4.5 6.0	Fig. 12
t_{PHL}/t_{PLH}	propagation delay LD to Q_n		102 37 30	370 74 63		465 93 79		555 111 94	ns	2.0 4.5 6.0	Fig. 13
t_{PHL}/t_{PLH}	propagation delay BI to Q_n		66 24 19	265 53 45		330 66 56		400 80 68	ns	2.0 4.5 6.0	Fig. 14
t_{PHL}/t_{PLH}	propagation delay PH to Q_n		55 20 16	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	
t_{THL}/t_{TLH}	output transition time		63 23 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Figs 12, 13 and 14
t_W	LD pulse width HIGH or LOW	35 7 6	11 4 3		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 13
t_{su}	set-up time D_n to LD	60 12 10	8 3 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 15
t_h	hold time D_n to LD	30 6 5	3 1 1		40 8 7		45 9 8		ns	2.0 4.5 6.0	Fig. 15

DC CHARACTERISTICS FOR 74HCT

Output capability: non-standard
I_{CC} category: MSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 1.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage		0.15	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 1.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_0, D_1, D_2	1.00
D_3	0.50
BI	0.50
LD	1.50
PH	1.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		38	80		100		120	ns	4.5	Fig. 12
t_{PHL}/t_{PLH}	propagation delay LD to Q_n		36	68		85		102	ns	4.5	Fig. 13
t_{PHL}/t_{PLH}	propagation delay BI to Q_n		32	66		83		99	ns	4.5	Fig. 14
t_{PHL}/t_{PLH}	propagation delay PH to Q_n		24	66		83		99	ns	4.5	
t_{THL}/t_{TLH}	output transition time		23	50		63		75	ns	4.5	Figs 12, 13 and 14
t_W	LD pulse width HIGH or LOW	10	4		13		15		ns	4.5	Fig. 13
t_{su}	set-up time D_n to LD	12	4		15		18		ns	4.5	Fig. 15
t_h	hold time D_n to LD	8	2		10		12		ns	4.5	Fig. 15

APPLICATION DIAGRAMS

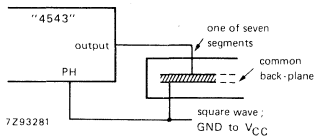


Fig. 8 Connection to liquid crystal (LCD) display readout.

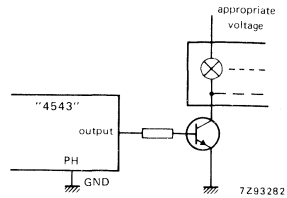


Fig. 9 Connection to incandescent display readout.

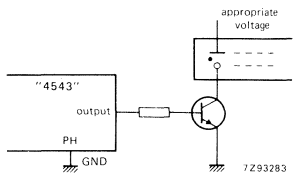


Fig. 10 Connection to gas discharge display readout.

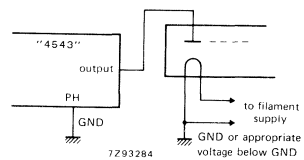


Fig. 11 Connection to fluorescent display readout.

AC WAVEFORMS

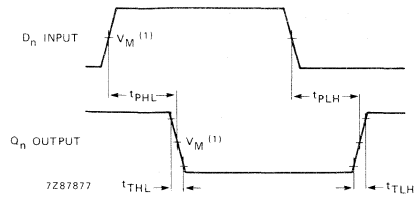


Fig. 12 Waveforms showing the address input (D_n) to output (Q_n) propagation delays and the output transition times.

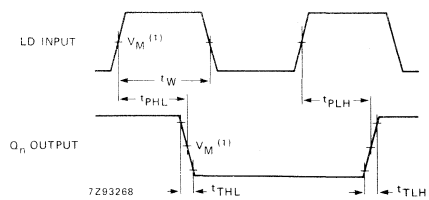


Fig. 13 Waveforms showing the latch disable input (LD) to output (Q_n) propagation delays and the output transition times.

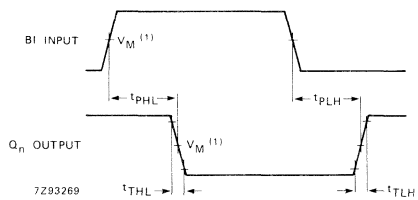


Fig. 14 Waveforms showing the blanking (BI) to output (Q_n) propagation delays and the output transition times.

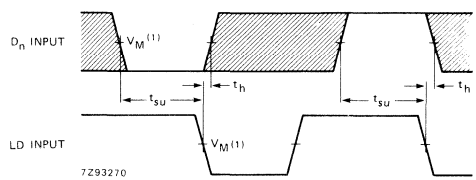


Fig. 15 Waveforms showing the address (D_n) to latch disable (LD) input set-up and hold times.

Note to Fig. 15

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

BCD TO 7-SEGMENT LATCH/DECODER/DRIVER

The HEF4543B is a BCD to 7-segment latch/decoder/driver for liquid crystal and LED displays. It has four address inputs (D_A to D_D), an active HIGH latch disable input (LD), an active HIGH blanking input (BI), an active HIGH phase input (PH) and seven buffered segment outputs (O_a to O_g).

The circuit provides the function of a 4-bit storage latch and an 8-4-2-1 BCD to 7-segment decoder/driver. It can invert the logic levels of the output combination. The phase (PH), blanking (BI) and latch disable (LD) inputs are used to reverse the function table phase, blank the display and store a BCD code, respectively.

For liquid crystal displays a square-wave is applied to PH and the electrical common back-plane of the display. The outputs of the device are directly connected to the segments of the liquid crystal.

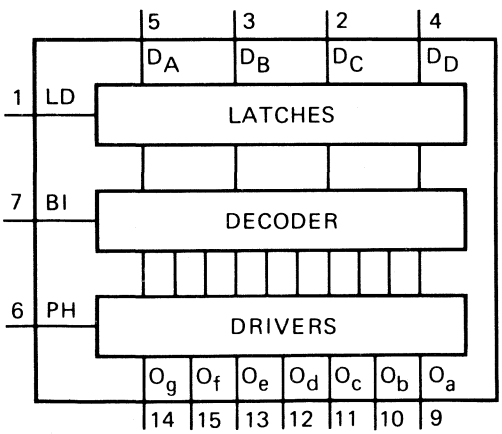


Fig. 1 Functional diagram.

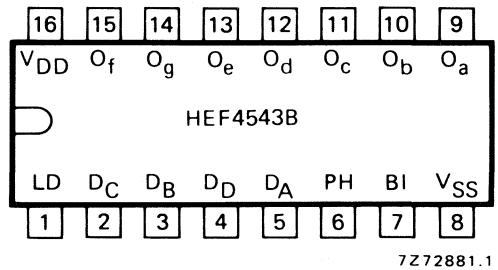


Fig. 2 Pinning diagram.

HEF4543BP : 16-lead-DIL; plastic (SOT-38Z).
HEF4543BD: 16-lead-DIL; ceramic (cerdip) (SOT-74).
HEF4543BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

D_A to D_D	address (data) inputs
PH	phase input (active HIGH)
BI	blanking input (active HIGH)
LD	latch disable input (active HIGH)
O_a to O_g	segment outputs

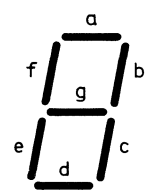


Fig. 3 Segment designation.

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

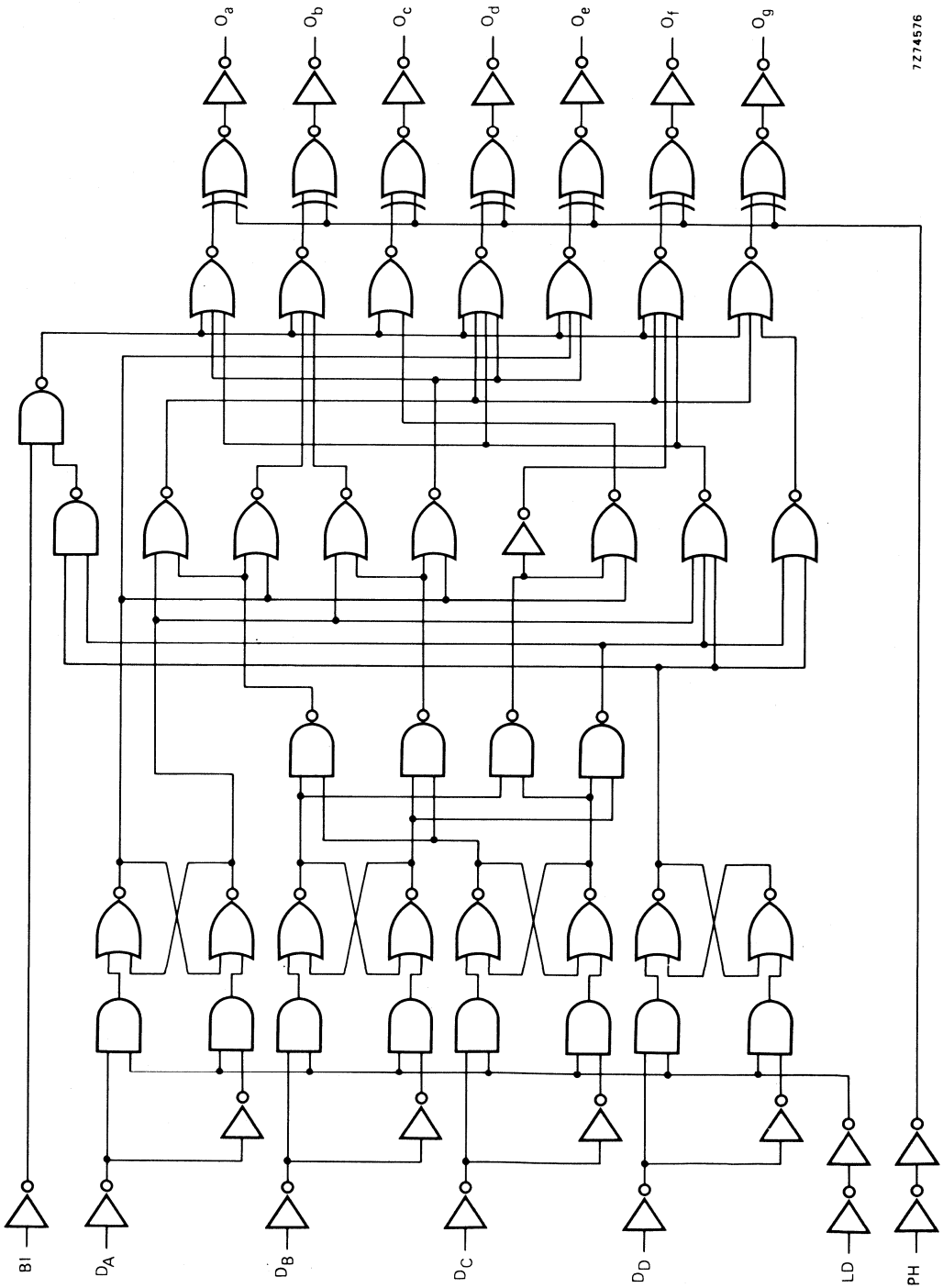


Fig. 4 Logic diagram.

FUNCTION TABLE

inputs							outputs							
LD	BI	PH *	D_D	D_C	D_B	D_A	O_a	O_b	O_c	O_d	O_e	O_f	O_g	display
X	H	L	X	X	X	X	L	L	L	L	L	L	L	blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	biank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	blank
L	L	L	X	X	X	X				* *				* *
as above		H	as above				inverse of above							as above

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

* For liquid crystal displays, apply a square-wave to PH.
For common cathode LED displays, select PH = LOW.
For common anode LED displays, select PH = HIGH.

** Depends upon the BCD-code previously applied when LD = HIGH.

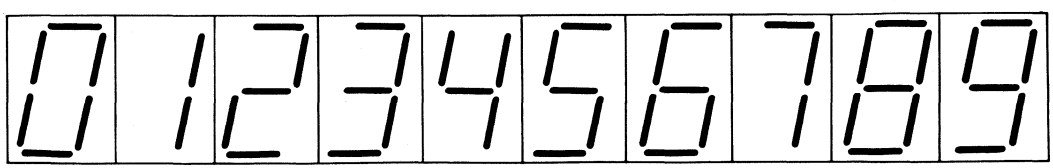


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Fig. 5 Display.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$D_n \rightarrow O_n$	5			180	360	ns	153 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		75	150	ns	64 ns + (0,23 ns/pF) C_L
	15			55	110	ns	47 ns + (0,16 ns/pF) C_L
	5			180	360	ns	153 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	150	ns	64 ns + (0,23 ns/pF) C_L
	15			55	110	ns	47 ns + (0,16 ns/pF) C_L
$LD \rightarrow O_n$	5			170	340	ns	143 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		80	160	ns	69 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
	5			190	380	ns	163 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		80	160	ns	69 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
$BI \rightarrow O_n$	5			145	290	ns	118 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
	5			125	250	ns	98 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	110	ns	54 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Minimum LD	5		60	30		ns	
pulse width; HIGH	10	t_{WLDH}	30	15		ns	
	15		20	10		ns	
Set-up time	5		40	20		ns	
$D_n \rightarrow LD$	10	t_{su}	20	5		ns	
	15		15	0		ns	
Hold time	5		0	−15		ns	
$D_n \rightarrow LD$	10	t_{hold}	15	0		ns	
	15		20	5		ns	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	2 200 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	10 400 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	33 000 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

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DATA HANDBOOK SYSTEM

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